Features

- Selectable reference inputs support either single-ended or differential or XTAL
- 8 Differential Outputs With 2 Banks
- User Configurable Output Signaling Standard for each bank: LVDS or LVPECL or HCSL
- LVCMOS reference Output up to 250MHz
- Up to 1.5GHz output frequency for differential outputs (LVDS,LVPECL)
- Ultra low additive phase jitter: < 20fs RMS (typical value in differential 156.25MHz, 12KHz to 20MHz integration range)
- Low skew between outputs within banks (< 40ps)
- Low delay from input to output (< 0.9ns)
- Pin-Controlled Configuration
- Separate Input output supply voltage for level shifting
- Spread-spectrum tolerant
- V_{CC} Core Supply: 3.3V±5% / 2.5V±5%
- V_{CCO} Output Supplies: 3.3V±5% / 2.5V±5%
  V_{CCO} can't be greater than VCC ($V_{CCO} \leqslant V_{CC}$)
- Industrial Temperature Range: –40°C to +85°C
- Package: 40-lead TQFN (6mm × 6mm)

Applications

- PCIe Gen1~Gen5
- Clock Distribution and Level Translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre Channel, SATA/SAS, SONET/SDH, CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing
- Remote Radio Units and Baseband Units

Description

The RS00308 is a 1.5 GHz 8-output differential fan out buffer intended for high-frequency, low-jitter clock/data distribution and level translation.

The input clock can be selected from two universal inputs or one crystal input. The selected input clock is distributed to two banks of 10 differential outputs and one LVCMOS output. The differential output banks can be mutually configured as LVPECL, LVDS, HCSL drivers, or disabled. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The RS00308 operates from a 3.3V/2.5V core supply and 3 independent 3.3V/2.5V output supplies.

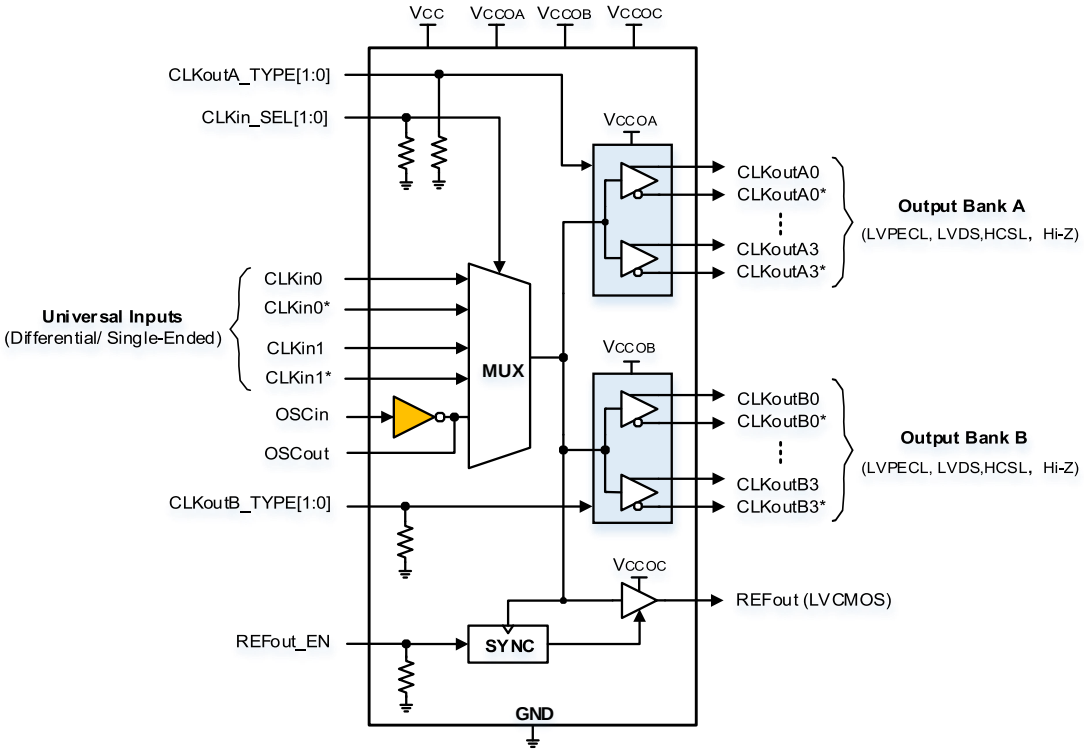
The RS00308 provides high performance, versatility, and power efficiency, making it ideal for replacing fixed-output buffer devices while increasing timing margin in the system.

Ordering Information

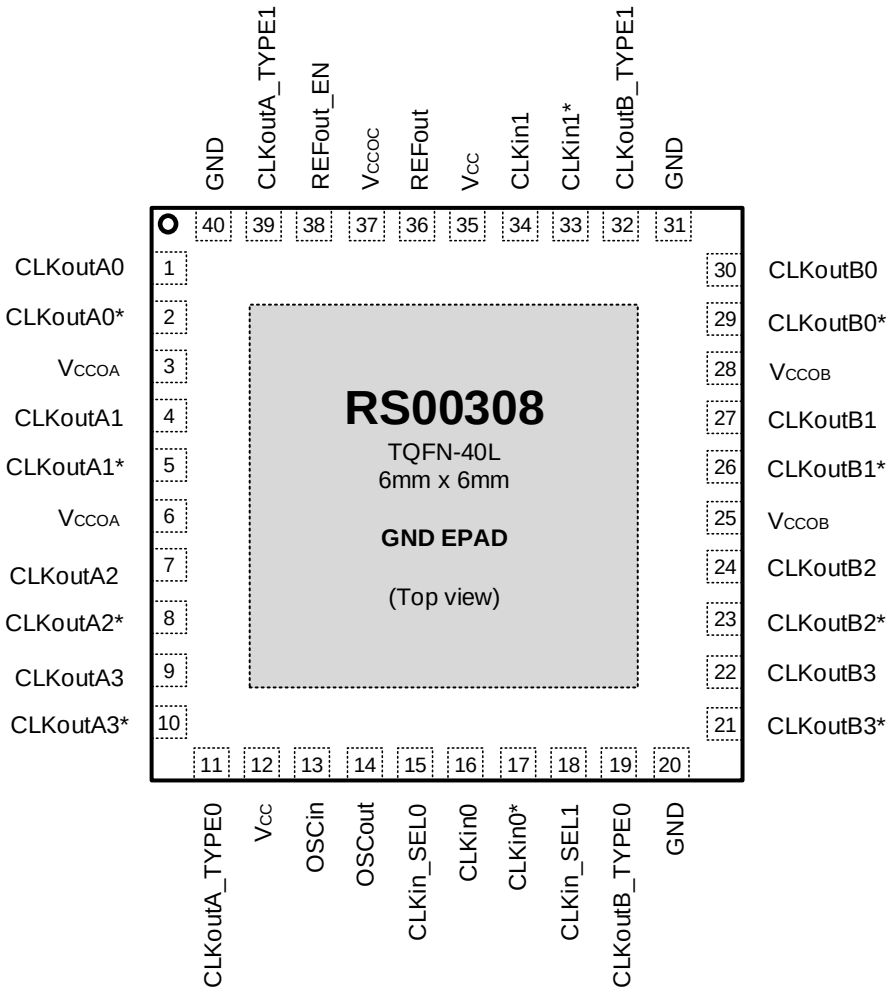
Part Number	Package	Description
RS00308ZDE	TQFN-40L	6mmx6mmx0.75mm

Notes:
[1] E = Pb-free and Green

Block Diagram



Pin Configuration



Pin	Name	Type	Description
49	EPAD	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
20,31,40	GND	GND	Ground
12, 35	V_{CC}	P	Power supply for Core and Input Buffer blocks. The V_{CC} supply operates at 3.3 V or 2.5V.
15, 18	CLKin_SEL0, CLKin_SEL1	I	Clock input selection pins.[2]
13	OSCin	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
14	OSCout	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.

Pin	Name	Type	Description
16, 17	CLKin0, CLKin0*	I	Universal clock input 0 (differential/single-ended)
33, 34	CLKin1*, CLKin1	I	Universal clock input 1 (differential/single-ended)
11, 39	CLKoutA_TYPE0, CLKoutA_TYPE1	I	Bank A and Bank B output buffer type selection pins [2]
3,6	V_{CCOA}	P	Power supply for Bank A Output buffers. V_{CCOA} operates at 3.3 V or 2.5V.
1,2	CLKoutA0, CLKoutA0*	O	Differential clock output A0. Output type set by CLKoutA_TYPE pins.
4,5	CLKoutA1, CLKoutA1*	O	Differential clock output A1. Output type set by CLKoutA_TYPE pins.
7,8	CLKoutA2, CLKoutA2*	O	Differential clock output A2. Output type set by CLKoutA_TYPE pins.
9,10	CLKoutA3, CLKoutA3*	O	Differential clock output A3. Output type set by CLKoutA_TYPE pins.
19,32	CLKoutB_TYPE0, CLKoutB_TYPE1	I	Bank B output buffer type selection pins [2]
25, 28	V_{CCOB}	P	Power supply for Bank B Output buffers. V_{CCOB} operates at 3.3 V or 2.5V.
21, 22	CLKoutB3*, CLKoutB3	O	Differential clock output B3. Output type set by CLKoutB_TYPE pins.
23, 24	CLKoutB2*, CLKoutB2	O	Differential clock output B2. Output type set by CLKoutB_TYPE pins.
26, 27	CLKoutB1*, CLKoutB1	O	Differential clock output B1. Output type set by CLKoutB_TYPE pins.
29, 30	CLKoutB0*, CLKoutB0	O	Differential clock output B0. Output type set by CLKoutB_TYPE pins.
36	REFout	O	LVCMOS reference output. Enable output by pulling REFout_EN pin high.
37	V_{CCOC}	P	Power supply for REFout buffer. V_{CCOC} operates at 3.3 V or 2.5 V.
38	REFout_EN	I	REFout enable input. Enable signal is internally synchronized to selected clock input.

Note

[1] Any unused output pins should be left floating with minimum copper length (see note in Clock Outputs), or properly terminated if connected to a transmission line, or disabled/Hi-Z if possible. See Clock Outputs for output configuration and Termination and Use of Clock Drivers for output interface and termination techniques.
[2] CMOS control input with internal pull-down resistor.

Function Table

Table 1. Input Selection

CLKin_SEL1	CLKin_SEL0	SELECTED INPUT
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin

Table 2. Differential Output Buffer Type Selection

CLKout_ TYPE1(A/B)	CLKout_ TYPE0(A/B)	CLKoutX BUFFER TYPE
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Disabled (Hi-Z)

Table 3. Reference output Enable

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

Table 4. CLKin Input vs. Output States

STATE of SELECTED CLKin	STATE of ENABLED OUTPUTS
CLKinX and CLKinX* inputs floating	Logic low
CLKinX and CLKinX* inputs shorted together	Not Supported. Output is Undefined
CLKin logic low	Logic low
CLKin logic high	Logic high

Absolute Maximum Ratings

Storage Temperature.....–65°C to +150°C
Ambient Temperature.....–40°C to +85°C
Junction Temperature..... +150°C
Supply Voltage to Ground.....–0.5V to +4.6V
Input Voltage ..... –0.5V to VCC+0.5V
Clock Output Voltage..... –0.5V to VCC+0.5V
Latch Up.....200mA
ESD, HBM..... –2000V to +2000V

Note:
Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Information

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
θJc	Junction to case thermal resistance			18.3		°C/W
θJb	Junction to Base thermal resistance			0.69		
θJA0	Junction to ambient thermal resistance	flow = 0 m/s		37.3		
θJA1	Junction to ambient thermal resistance	flow = 1 m/s		31.4		
θJA2	Junction to ambient thermal resistance	flow = 2 m/s		30.1		

Electrical Characteristics (Power Supply)

Unless otherwise specified: Vcc = 3.3V/2.5V ± 5%, Vcco = 3.3V/2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc=3.3V,Vcco=3.3V,T_A= 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.[1]

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
Power Supply						
V_{CC}	Core Supply Voltage	3.3V	3.135	3.3	3.465	V
		2.5V	2.375	2.5	2.625	
V_{CCOA} V_{CCOB} V_{CCOC}	Output Supply Voltage Range[1]	3.3V	3.135	3.3	3.465	V
		2.5V	2.375	2.5	2.625	
Current Consumption						
I_{CC_CORE}	Core Supply Current.			90	120	mA
I_{CCO_PECL}	Output Supply Current (LVPECL)	All LVPECL outputs unloaded		150	190	mA
I_{CCO_LVDS}	Output Supply Current (LVDS)	All LVDS outputs loaded		110	150	mA
I_{CCO_HCSL}	Output Supply Current (HCSL)	All HCSL outputs unloaded		80	140	mA
Temperature						
T_A	Ambient Temperature Range		-40	25	85	℃
T_B	PCB operating Temperature		-40		105	℃

Note

[1] The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

Electrical Characteristics (Inputs)

Unless otherwise specified: Vcc = 3.3V/2.5V± 5%, Vcco = 3.3V/2.5V± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc=3.3V,Vcco=3.3V,T_A= 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.[1]

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
CMOS CONTROL INPUTS (CLKin_SELn , CLKout_TYPEn , REFout_EN)						
V_{IH}	High-Level Input Voltage	VCC=3.3V	2		V_{CC}	V
		VCC=2.5V	1.7		V_{CC}	V
V_{IL}	Low-Level Input Voltage	VCC=3.3V	GND		0.4	V
		VCC=2.5V	GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = Vcc, Internal pull down			50	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0V, Internal pull down	-5	0.1		µA
CLOCK INPUTS (CLKin0/CLKin0*, CLKin1/CLKin1*)						
I_{IH}	Input High current	Input =V_{CC}			150	µA
I_{IL}	Input Low current	Input = GND	-150			µA
C_{IN}	Differential Input capacitance			3		pF
V_{IHD}	Differential Input High Voltage	CLKin driven differentially			V_{CC}+0.3	V
V_{ILD}	Differential Input Low Voltage		-0.3			V
V_{ID}	Differential Input Voltage Swing		0.15		1.3	V
V_{CMD}	Differential Input Common Mode Voltage	V_{ID} = 150mV	0.25		V_{CC}-1.2	V
		V_{ID} = 350mV	0.25		V_{CC}-1.1	V
		V_{ID} = 800mV	0.25		V_{CC}-0.9	V
ISO_{MUX}	Mux Isolation, CLKin0 to CLKin1	f_{OFFSET} > 50kHz, P_{CLKinX} = 0dBm		-89		dBc
V_{IH}	Single-Ended Input High Voltage	VCC=3.3V	2.0		V_{CC}+0.3	V
		VCC=2.5V	1.7		V_{CC}+0.3	V
V_{IL}	Single-Ended Input Low Voltage	VCC=3.3V	-0.3		0.8	V
		VCC=2.5V	-0.3		0.7	V
CRYSTAL INTERFACE (OSCin, OSCout)						
F_{CLK}	External Clock Frequency Range	OSCin driven single-ended, OSCout floating			250	MHz
F_{XTAL}	Crystal Frequency Range	Fundamental mode	10		50	MHz
ESR	Equivalent Series Resistance (ESR)				70	Ω
C_S	Shunt Capacitance				7	pF
C_L	Load Capacitance		10		18	pF
Pd	Drive Level				500	µW

Note

[1] The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

Electrical Characteristics (LVPECL)

Unless otherwise specified: Vcc = 3.3V/2.5V±5%, Vcco = 3.3V/2.5V±5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc=3.3V,Vcco=3.3V,T_A= 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.[1]

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
LVPECL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)						
f_{CLKout}	Maximum Output Frequency	V_{OD} ≥ 400mV, R_L = 100Ω differential		1.5		GHz
$Jitter_{ADD}$	Additive RMS Jitter	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns, 10kHz to 20MHz		20		fs
		CLKin: 156.25MHz, Slew rate ⩾ 3V/ns, 1MHz to 20MHz		10		fs
P_S	Phase noise f_{offset} ≥10MHz	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns		-156		dBc/Hz
t_R	Output Rise Time 20% to 80%	R_T = 150Ω to GND, R_L = 100Ω differential CL ≤ 5pF	120	150	300	ps
t_F	Output Fall Time 80% to 20%		120	150	300	ps
t_{PD_PECL}	Propagation Delay CLKin-to-LVPECL	R_T = 150Ω to GND, R_L = 100Ω differential, C_L ≤ 5pF		600		ps
$t_{SK(O)}$	Output Skew LVPECL	Skew specified between any two CLKouts with the same buffer type.		30	50	ps
$t_{SK(P)}$[2]	Part to Part Skew			80	120	ps
T_{ODC}	Duty Cycle	Frequency< 650MHz	48%		52%	
		Frequency< 1GHz	45%		55%	
		Frequency< 1.5GHz	40%		60%	
V_{OH}	Output High Voltage	TA = 25°C, DC Measurement, R_T = 50Ω to Vcco - 2V	V_{CCO}-1.4		V_{CCO}-0.9	V
V_{OL}	Output Low Voltage		V_{CCO} - 2.2		V_{CCO}-1.7	V
V_{OD}	Output Voltage Swing Single-ended	Frequency< 1GHz	500		1100	mV
		Frequency ≥ 1GHz	400		1000	mV

Note

[1] The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

[2] This parameter is guaranteed by design.

Electrical Characteristics (LVDS)

Unless otherwise specified: Vcc = 3.3V/2.5V±5%, Vcco = 3.3V/2.5V±5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc=3.3V,Vcco=3.3V,T_A= 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.[1]

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
LVDS OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)						
f_{CLKout}	Maximum Output Frequency	V_{OD} ≥ 400mV, R_L = 100Ω differential		1.5		GHz
$Jitter_{ADD}$	Additive RMS Jitter	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns, 10kHz to 20MHz		20		fs
		CLKin: 156.25MHz, Slew rate ⩾ 3V/ns, 1MHz to 20MHz		10		fs
P_S	Phase noise f_{offset} ≥10MHz	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns		-156		dBc/Hz
t_R	Output Rise Time 20% to 80%	RL = 100Ω differential, CL ⩽ 5pF	120	150	300	ps
t_F	Output Fall Time 80% to 20%		120	150	300	ps
t_{PD_LVDS}	Propagation Delay CLKin-to LVDS	R_L = 100Ω differential, C_L ≤ 5pF		600		ps
$t_{SK(O)}$	Output Skew LVDS	Skew specified between any two CLKouts with the same buffer type. R_L = 100Ω differential, C_L ≤ 5pF		15	40	ps
$t_{SK(PP)}$[2]	Part-to-Part Output Skew LVDS			80	120	ps
T_{ODC}	Duty Cycle	Frequency< 650MHz	47%		53%	
		Frequency< 1GHz	45%		55%	
		Frequency< 1.5GHz	40%		60%	
V_{OH}	Output High Voltage			1.45		V
V_{OL}	Output Low Voltage			1.05		V
V_{OS}	Output Offset Voltage	T_A = 25°C, DC Measurement, R_L = 100Ω differential		1.25		V
Δ V_{OS}	Change in V_{OS} for Complementary Output States				50	mV
V_{OD}	Output Voltage Swing	Frequency< 1GHz	300		500	mV
		Frequency≥ 1GHz	250		450	mV

Note

[1] The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

[2] This parameter is guaranteed by design.

Electrical Characteristics (HSCL)

Unless otherwise specified: Vcc = 3.3V/2.5V±5%, Vcco = 3.3V/2.5V±5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc=3.3V,Vcco=3.3V,T_A= 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.[1]

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
HSCL (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)						
f_{CLKout}	Output FrequencyRange	C_L ⩽ 5pF			250	MHz
$Jitter_{ADD_PCIe-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen2 Hi Band (5.0 GT/s)		110	310	fs (RMS)
		PCIe Gen2 Lo Band (5.0 GT/s)		10	20	
		PCIe Gen3 (8.0 GT/s)		35	60	
		PCIe Gen4 (16.0 GT/s) [3] [4]		30	60	
		PCIe Gen5 (32.0 GT/s) [3] [5]		15	25	
$Jitter_{ADD_PCIe-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS)	PCIe Gen2 (5.0 GT/s)		80	300	fs (RMS)
		PCIe Gen3 (8.0 GT/s)		50	150	
		PCIe Gen4 (16.0 GT/s) [3] [4]		40	150	
		PCIe Gen5 (32.0 GT/s) [3] [5]		25	60	
$Jitter_{ADD}$	Additive RMS Jitter	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns, 10kHz to 20MHz		20		fs
		CLKin: 156.25MHz, Slew rate ⩾ 3V/ns, 1MHz to 20MHz		10		fs
P_S	Phase noise f_{offset} ≥10MHz	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns		-156		dBc/Hz
t_R	Output Rise Time 20% to 80%	250MHz, R_L = 50Ω to GND, C_L ⩽ 5pF	300		700	ps
t_F	Output Fall Time 80% to 20%		300		700	ps
t_{PD_HSCL}	Propagation Delay CLKin-to HSCL	100MHz		900		ps
$t_{SK(O)}$	Output Skew	Skew specified between any two CLKouts with the same buffer type. Load conditions		15	40	ps
$t_{SK(PP)}$[2]	Part-to-Part Output Skew			80	120	ps
T_{ODC}	Duty Cycle	Frequency< 250MHz	48%		52%	
V_{OH}	Output High Voltage	R_T = 50Ω to GND, V_{CCO}=2.5V	500		900	mV
		R_T = 50Ω to GND, V_{CCO}=3.3V	700	800	900	mV
V_{OL}	Output Low Voltage	T_A = 25°C, DC Measurement, R_T = 50Ω to GND	-150		150	mV
V_{CROSS}	Absolute Crossing Voltage	R_L = 50Ω to GND, C_L ⩽ 5pF		460		mV
Δ V_{CROSS}	Total Variation of V_{CROSS}				140	mV

Note

[1] The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

[2] This parameter is guaranteed by design.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

Electrical Characteristics（LVCMOS）

Unless otherwise specified: Vcc = 3.3V/2.5V±5%, Vcco = 3.3V/2.5V±5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc=3.3V,Vcco=3.3V,T_A= 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.[1]

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
LVCMOS OUTPUT (REFout)						
f_{CLKout}	Output Frequency Range	Crystal Input	10		50	MHz
		Single Ended input			250	MHz
$Jitter_{ADD}$	additive jitter RMS	Crystal Input		300		fs
		Single Ended input		30		fs
P_S	Phase noise f_{offset} ≥10MHz	CLKin: 156.25MHz, Slew rate ⩾ 3V/ns		-156		dBc/Hz
t_R	Output Rise Time 20% to 80%	Uniform transmission line up to 10 inches with 50Ω characteristic impedance, R_L = 100Ω differential, C_L ⩽ 5pF		225	400	ps
t_F	Output Fall Time 80% to 20%			225	400	ps
t_{PD_CMOS}	Propagation Delay CLKin-to-LVCMOS	V_{CCO} = 3.3V ,25MHz		2200		ps
		V_{CCO} = 2.5V , 25MHz		2200		ps
t_{EN}	Output Enable Time		2		4	cycles
t_{DIS}	Output Disable Time		2		4	cycles
T_{ODC}	Duty Cycle	50% input clock duty cycle; C_L=10pF	45%		55%	
V_{OH}	Output High Voltage	V_{CCO} = 3.3V+/-5%, I_{OH} = 8mA	2.3			V
		V_{CCO} = 2.5V+/-5%, I_{OH} = 8mA	1.5			V
		V_{CCO} = 3.3V+/-5%, I_{OH} = 24mA	2.1			V
		V_{CCO} = 2.5V +/-5%, I_{OH} = 16mA	1.5			V
V_{OL}	Output Low Voltage	V_{CCO} = 3.3V +/-5%, I_{OL} = -8mA			0.5	V
		V_{CCO} = 2.5V +/-5%, I_{OL} = -8mA			0.4	V
		V_{CCO} = 3.3V +/-5%, I_{OL} = -24mA			1	V
		V_{CCO} = 2.5V +/-5%, I_{OL} = -16mA			0.8	V
R_{O_LVCMOS}	Output Impedance	V_{CCO} = 3.3V +/-5%,		17		Ω
		V_{CCO} =2.5V +/-5%,		22		Ω

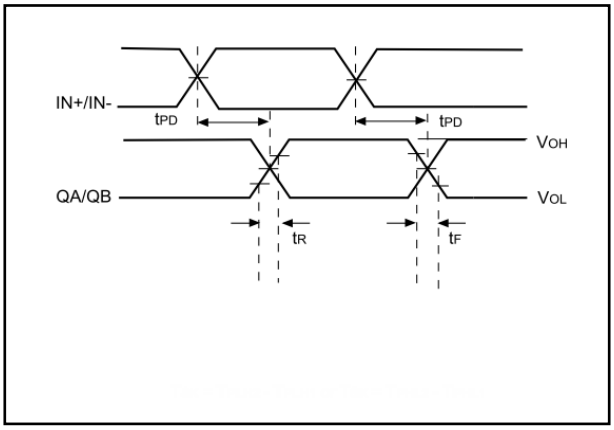
Note

[1] The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

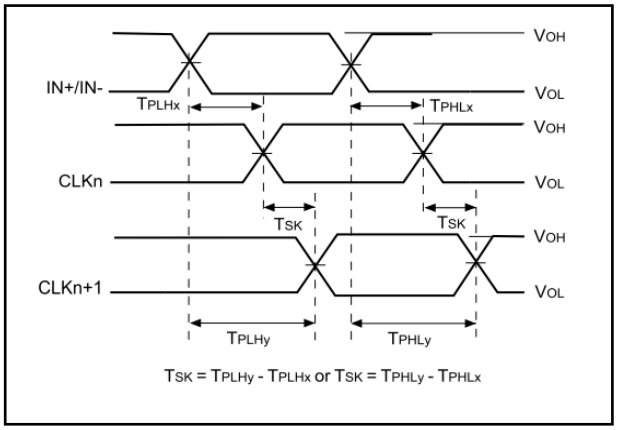
Figure of Timing Characteristics

Unless otherwise specified: Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, CLKin driven differentially, input slew rate ⩾ 3V/ns.

Propagation Delay



Output Skew



Part to Part Skew

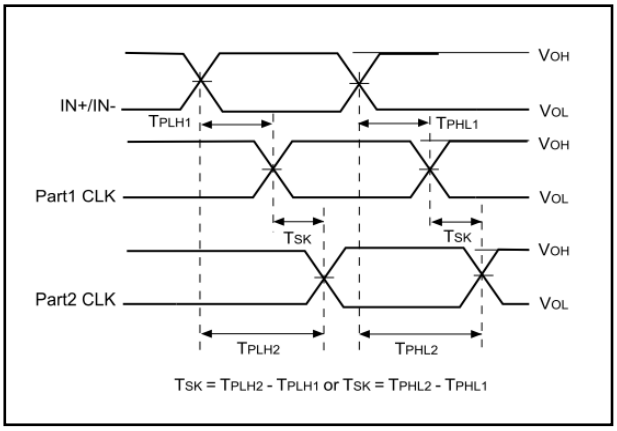
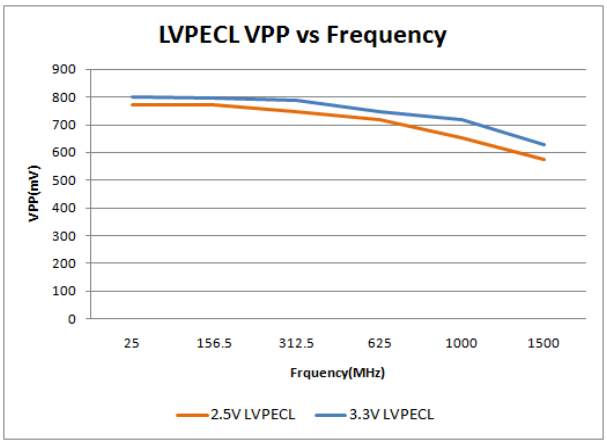


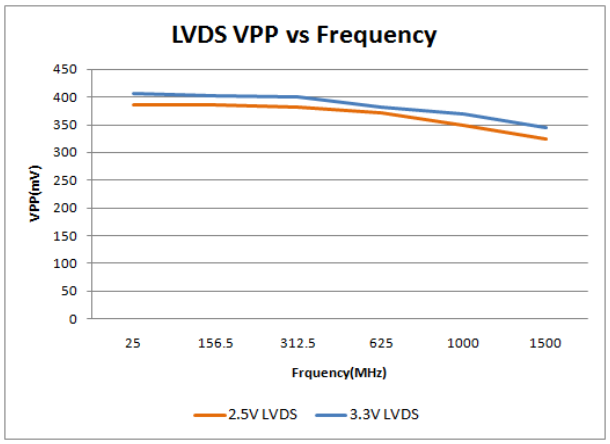
Figure of Timing Characteristics

Unless otherwise specified: Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, CLKin driven differentially, input slew rate ⩾ 3V/ns.

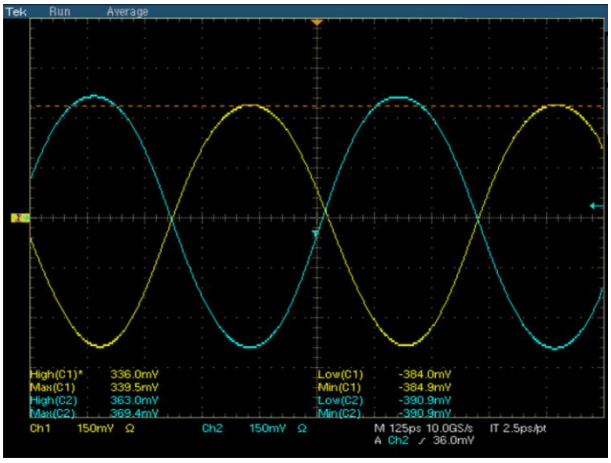
LVPECL Output Swing vs. Frequency



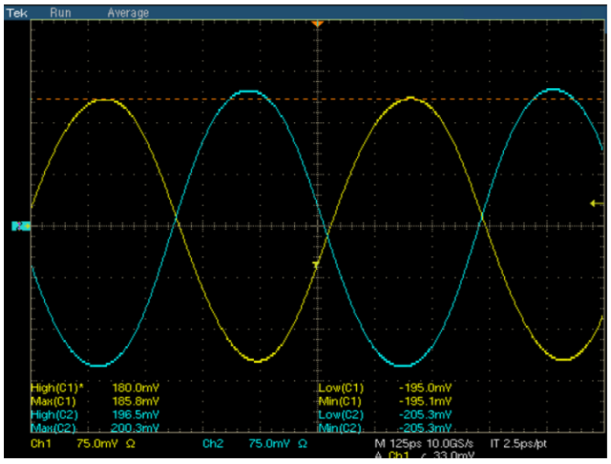
LVDS Output Swing vs. Frequency



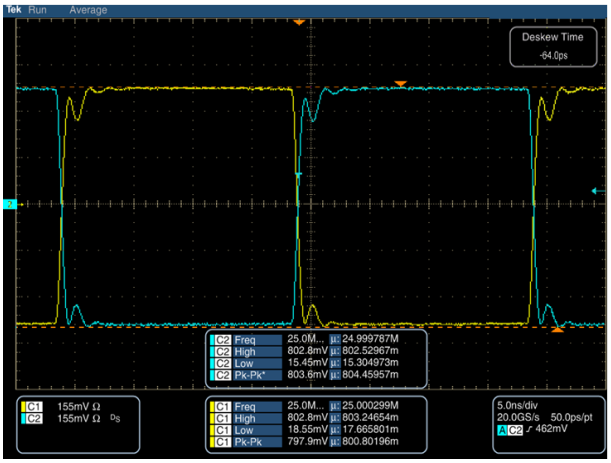
LVPECL Output Swing at 1.5GHz



LVDS Output Swing at 1.5GHz



HSCL Output Swing at 25MHz



LVCMOS Output Swing at 200MHz

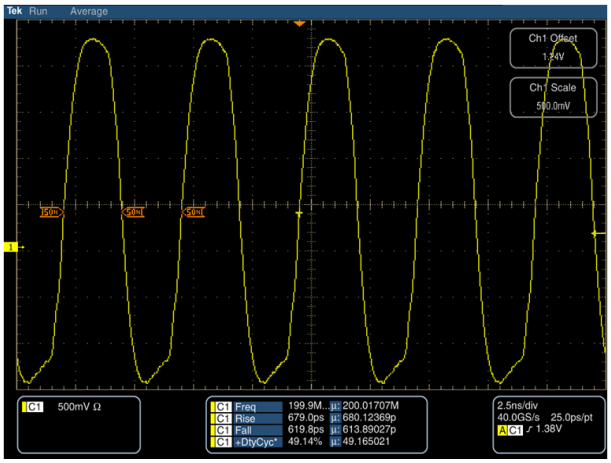


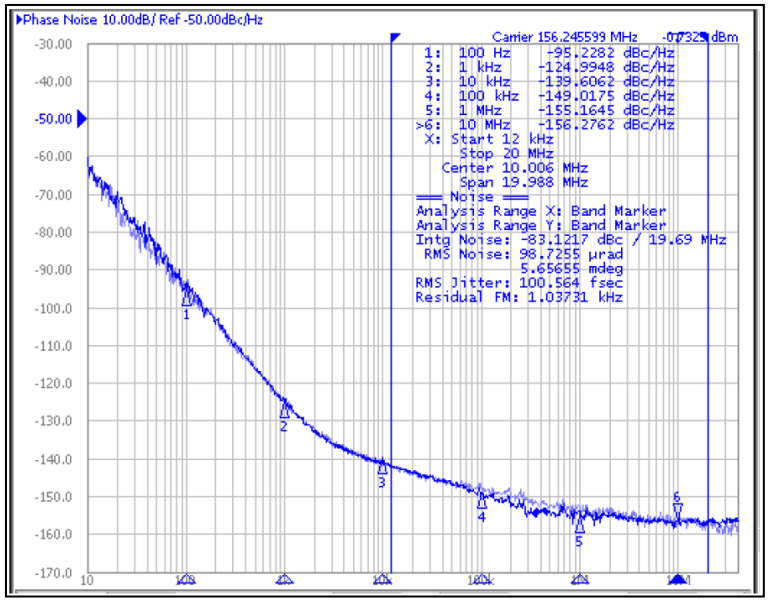
Figure of Timing Characteristics

Unless otherwise specified: Vcc = 3.3V, Vcco = 3.3V, TA = 25°C, CLKin driven differentially, input slew rate ⩾ 3V/ns.

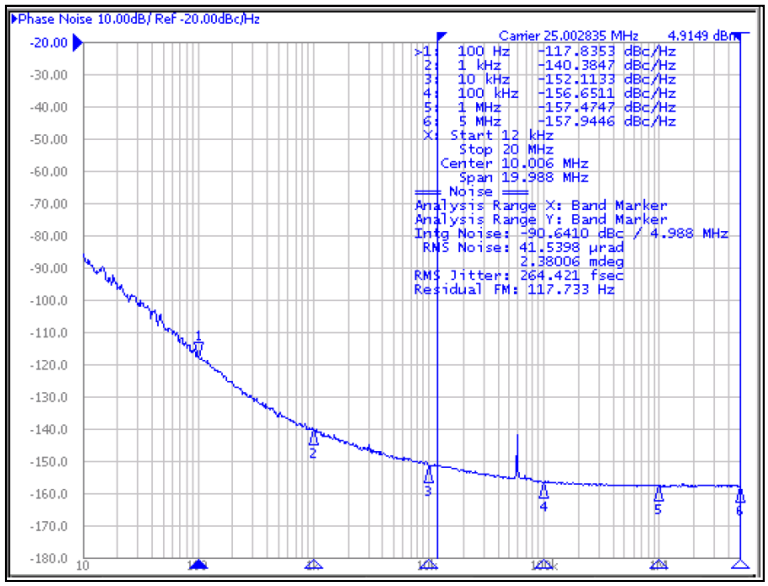
Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at 156.25MHz~27fs RMS (12kHz to 20MHz).

Additive jitter = (Output jitter^2 - Input jitter ^{2}) $^{1/2}$



Total Phase Jitter with 25MHz XTAL~264fs RMS (12kHz ~20MHz)



Feature Description

VCC and VCCO Power Supplies

The RS00308 has separate 3.3V/2.5V core supply (V_{CC}) and 3 independent 3.3V/2.5V output power supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}). Output supply operation at 2.5V enables lower power consumption and output-level compatibility with 2.5V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to its respective Vcco supply, while the output levels for LVDS and HCSL are relatively constant over the specified Vcco range.

Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator circuit will start-up and its clock will be distributed to all outputs. Alternatively, OSCin may be driven by a single-ended clock (up to 250MHz) instead of a crystal.

When OSCin is selected, the output state will be an inverted copy of the OSCin input state.

Clock Outputs

The differential output buffer type for both Bank A and B outputs are configured using the CLKout_TYPE[1:0]. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length (see note below) to minimize capacitance and potential coupling and reduce power consumption. If all differential outputs are not used, it is recommended to disable (Hi-Z) the banks to reduce power.

For best soldering practices, the minimum trace length for any unused pin should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the Vcco voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN.

The REFout_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout will be enabled within 4 cycles (t_{EN}) of the input clock after REFout_EN is toggled high. REFout will be disabled within 4 cycles (t_{DIS}) of the input clock after REFout_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1kΩ load to ground, then the output will be pulled to low when disabled.

Application Information

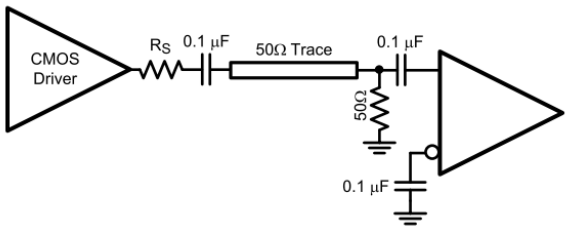
Driving the Clock Inputs

The RS00308 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept DC-coupled 3.3V/2.5V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in Electrical Characteristics. The device can accept a wide range of signals due to its wide input common mode voltage range and input voltage swing (V_{ID}) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling may also be employed to shift the input signal to within the range.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode-rejection.

While it is recommended to drive the CLKin/CLKin* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the Electrical Characteristics. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. Again, the single-ended input slew rate should be as high as possible to minimize performance degradation.

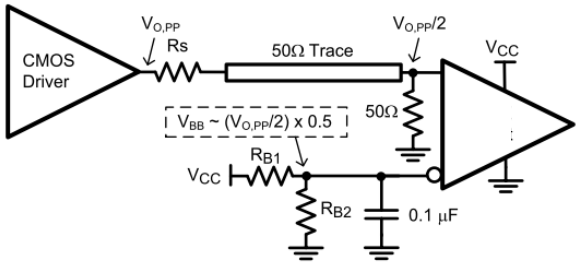
The CLKin input has an internal bias voltage of about 1.4V, so the input can be AC coupled. The output impedance of the LVCMOS driver plus Rs should be close to 50Ω to match the characteristic impedance of the transmission line and load termination.



Single-Ended LVCMOS Input, AC Coupling

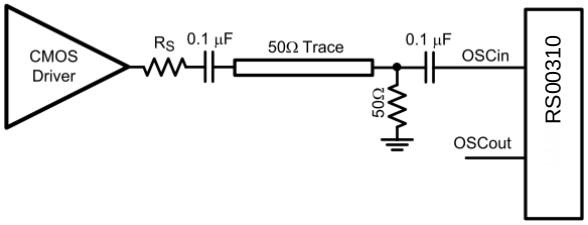
A single ended clock may also be DC coupled to CLKinX. A 50Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKinX, CLKinX* should be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage should be within the specified input common voltage range. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

If the LVCMOS driver cannot achieve sufficient swing with a DC-terminated 50Ω load at the CLKinX input, then consider connecting the 50Ω load termination to ground through a capacitor (C_{AC}). This AC termination blocks the DC load current on the driver, so the voltage swing at the input is determined by the voltage divider formed by the source (Ro + Rs) and 50Ω load resistors. The value for C_{AC} depends on the trace delay, Td, of the 50Ω transmission line, where C_{AC}>= 3*Td/50Ω.



Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing

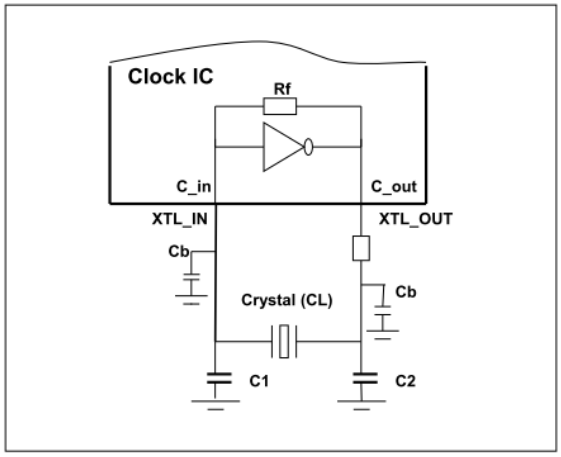
If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with a single-ended external clock. The input clock should be AC coupled to the OSCin pin, which has an internally- generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either universal input (CLKinX) since it offers higher operating frequency, better common mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.



Driving OSCin with a Single-Ended Input

Crystal Interface

The RS00308 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in bellow figure.



CL =crystal spec. loading cap.

C_in/out = (3~5pF) of IC pin cap.

Cb = PCB trace (2~4pF)

C1,C2 = load cap. of design

Rd = 50 to 100ohm drive level limit

Crystal Interface

Design guide: C1=C2=2*C_L - (Cb +C_in/out) to meet the target accuracy.(in +/- 20ppm)

Example 1: Select C_L=18pF crystal, C1=C2=2*(18pF) – (4pF+5pF)=27pF, check the datasheet of crystal.

Example 2: For higher frequency crystal (≥20MHz), can use the formula C1=C2=2*(CL-6), it can do fine tune of C1, C2 for more accurate ppm if necessary.

Termination and Use of Clock Drivers

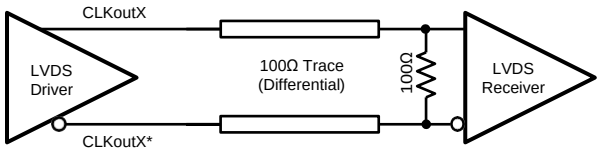
When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
  - LVDS outputs are current drivers and require a closed current loop.
  - HCSL drivers are switched current outputs and require a DC path to ground via 50Ω termination.
  - LVPECL outputs are open emitter and require a DC path to ground.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC coupled.

It is possible to drive a non-LVPECL or non-LVDS receiver with a LVDS or LVPECL driver as long as the above guidelines are followed. Check the data sheet of the receiver or input being driven to determine the best termination and coupling method to be sure the receiver is biased at the optimum DC voltage (common mode voltage).

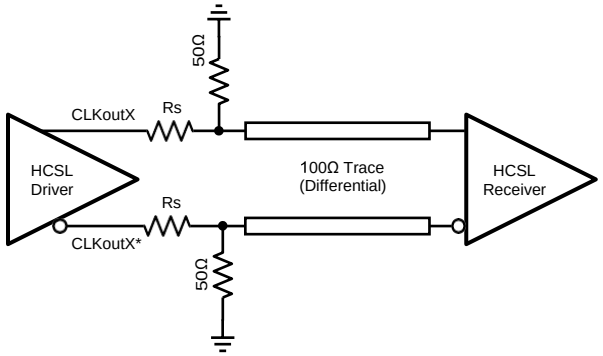
Termination for DC-Coupled Differential Operation

For DC-coupled operation of an LVDS driver, terminate with 100Ω as close as possible to the LVDS receiver as shown in the figure.



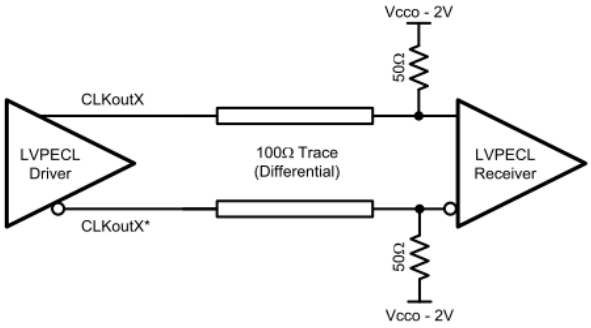
Differential LVDS Operation, DC Coupling, No Biasing by the Receiver

For DC-coupled operation of an HCSL driver, terminate with 50Ω to ground near the driver output. Series resistors, Rs, may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50Ω termination resistors.

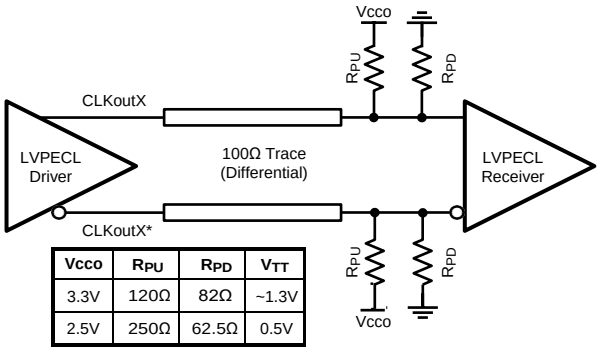


HCSL Operation, DC Coupling

For DC-coupled operation of an LVPECL driver, terminate with 50Ω to Vcco - 2V. Alternatively terminate with a Thevenin equivalent circuit for Vcco (output driver supply voltage) = 3.3V and 2.5V. In the Thevenin equivalent circuit, the resistor dividers set the output termination voltage (V_{TT}) to Vcco – 2V.



Differential LVPECL Operation, DC Coupling



Vcco	R_{PU}	R_{PD}	V_{TT}
3.3V	120Ω	82Ω	~1.3V
2.5V	250Ω	62.5Ω	0.5V

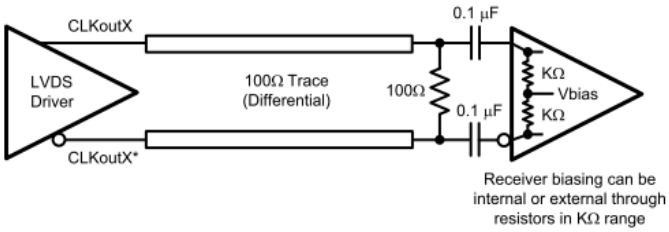
Differential LVPECL Operation, DC Coupling, Thevenin Equivalent

Termination for AC-Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common mode voltage) when driving different receiver standards. Because AC coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level.

When driving differential receivers with an LVDS driver, the signal may be AC coupled by adding DC-blocking capacitors; however the proper DC bias point needs to be established at both the driver side and the receiver side. The recommended termination scheme depends on whether the differential receiver has integrated termination resistors or not.

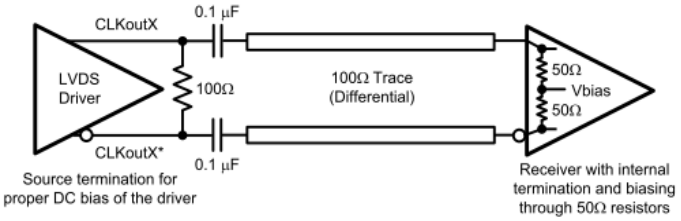
When driving a differential receiver without internal 100Ω differential termination, the AC-coupling capacitors should be placed between the load termination resistor and the receiver to allow a DC path for proper biasing of the LVDS driver. The load termination resistor and AC-coupling capacitors should be placed as close as possible to the receiver inputs to minimize stub length. The receiver can be biased internally or externally to a reference voltage within the receiver's common mode input range through resistors in the kilo-ohm range.



Differential LVDS Operation With AC Coupling to Receivers
Without Internal 100Ω Termination

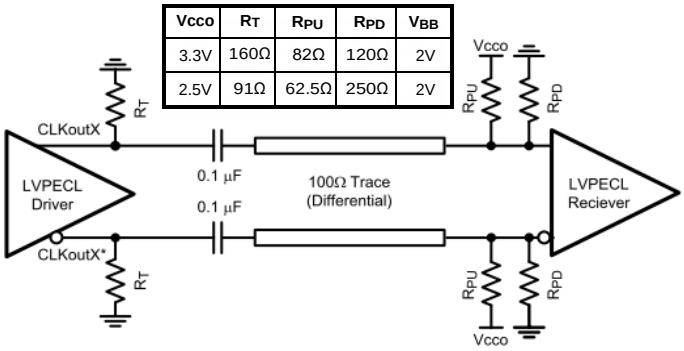
When driving a differential receiver with internal 100Ω differential termination, a source termination resistor should be placed before the AC-coupling capacitors for proper DC biasing of the driver. However, with a 100Ω resistor at the source and the load (that is, double terminated), the equivalent resistance seen by the LVDS driver is 50Ω which causes the effective signal swing at the input to be reduced by half. If a self-terminated receiver requires input swing greater than 250mVpp (differential) as well as AC coupling to its inputs, then the LVDS driver with the double-terminated arrangement may not meet the minimum input swing requirement; alternatively, the LVPECL or HCSL output driver format with AC coupling is recommended to meet the minimum input swing required by the self-terminated receiver.

When using AC coupling with LVDS outputs, there may be a startup delay observed in the clock output due to capacitor charging. The examples in bellow figure use 0.1µF capacitors, but this value may be adjusted to meet the startup requirements for the particular application.



Differential LVDS Operation With AC Coupling to Receivers
With Internal 100Ω Termination

LVPECL drivers require a DC path to ground. When AC coupling an LVPECL signal use 160Ω emitter resistors (or 91Ω for Vcco = 2.5V) close to the LVPECL driver to provide a DC path to ground. For proper receiver operation, the signal should be biased to the DC bias level (common mode voltage) specified by the receiver. The typical DC bias voltage (common mode voltage) for LVPECL receivers is 2V. Alternatively, a Thevenin equivalent circuit forms a valid termination for Vcco = 3.3V and 2.5V.

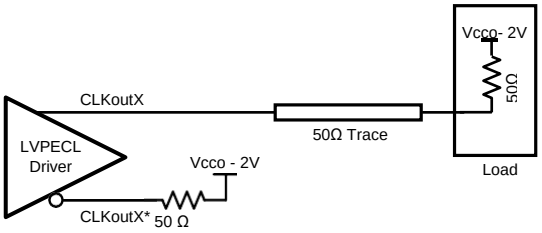


Differential LVPECL Operation, AC Coupling, Thevenin Equivalent

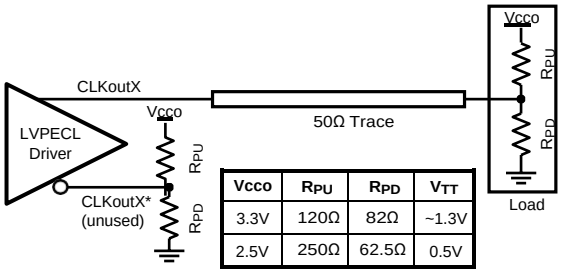
Termination for Single-Ended Operation

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal.

It is possible to use an LVPECL driver as one or two separate 800mV p-p signals. When DC coupling one of the RS00308 LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminate the unused driver. When DC coupling on of the RS00308 LVPECL drivers, the termination should be 50Ω to Vcco – 2V. The Thevenin equivalent circuit is also a valid termination for Vcco = 3.3V.



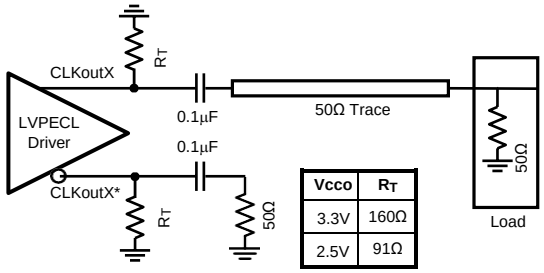
. Single-Ended LVPECL Operation, DC Coupling



Vcco	RPU	RPD	VTT
3.3V	120Ω	82Ω	~1.3V
2.5V	250Ω	62.5Ω	0.5V

Single-Ended LVPECL Operation, DC Coupling, Thevenin Equivalent

When AC coupling an LVPECL driver use a 160Ω emitter resistor (or 91Ω for Vcco = 2.5V) to provide a DC path to ground and ensure a 50Ω termination with the proper DC bias level for the receiver. The typical DC bias voltage for LVPECL receivers is 2V. If the companion driver is not used, it should be terminated with either a proper AC or DC termination. This latter example of AC coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment no DC bias point (0 VDC) is required for safe and proper operation. The internal 50Ω termination the test equipment correctly terminates the LVPECL driver being measured as shown in the figure. When using only one LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminated the unused driver.



Vcco	RT
3.3V	160Ω
2.5V	91Ω

Single-Ended LVPECL Operation, AC Coupling

Power Supply Recommendations

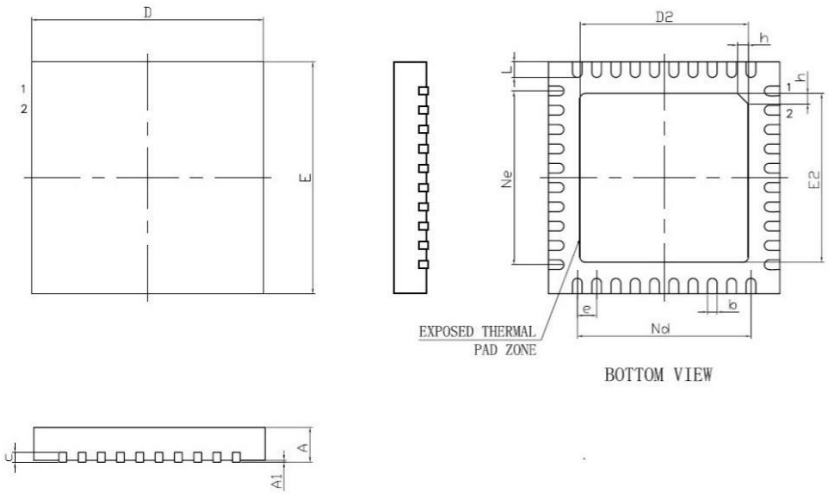
Power Supply Sequencing

When powering the Vcc and Vcco pins from separate supply rails, It is recommended that the supplies to reach their regulation point at approximately the same time while ramping up, or reach ground potential at the same time while ramping down. Using simultaneous or ratio metric power supply sequencing prevents internal current flow from Vcc to Vcco pins that could occur when Vcc is powered before Vcco.

Power Supply Bypassing

The Vcc and Vcco power supplies should have a high-frequency bypass capacitor, such as 0.1µF or 0.01µF, placed very close to each supply pin. 1µF to 10µF decoupling capacitors should also be placed nearby the device between the supply and ground planes. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		

Note:
1.All dimensions are in mm. Angels in degrees.
2.Coplanarity applies to the exposed thermal pad as well as the terminals.
3.Refer Jedec MO-220
4.Thermal pad soldering area.

TQFN6X6X0.75-0.5-40L (ZD40) POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	1. Initial release	2025/6/17
V1.1	1. Modify Pin configuration error. Pin 35 = VCC	2025/11/19
V1.2	1. Update the Pin configuration diagram outline	2026/10/30