## Features

- PCIe Gen5 additive phase jitter: 6fs RMS
- PCIe Gen6 additive phase jitter: 5fs RMS
- PCIe Gen7 additive phase jitter: 3fs RMS
- DB2000Q additive phase jitter: 15fs RMS
- 12kHz to 20MHz additive phase jitter: 40fs RMS at 156.25MHz
- Power Down Tolerant (PDT) inputs
- Flexible Startup Sequencing (FSS)
- Automatic Clock Parking (ACP) upon loss of CLKIN
- Selectable output slew rate via pin or SMBus
- 4-wire Side-Band Interface supports high-speed
- serial output enable and device daisy-chaining
- 9 selectable SMBus addresses
- SMBus write protection features
- Spread-spectrum tolerant
- 85Ω or 100Ω (-100 suffix) output impedance
- CLKIN accepts HCSL or LVDS signal levels
- -40 to +105°C, 3.3V ±10% operation

## Applications

- Cloud/High-performance Computing
- NVMe Storage
- Networking
- Accelerators

## Description

The RS2CB190xx (RS2CB19020, RS2CB19016, RS2CB19013, RS2CB19008, RS2CB19004) ultra-high performance fanout buffers support PCIe Gen6 and Gen7. They provide a Loss-Of-Signal (LOS) output for system monitoring and redundancy. The devices also incorporate Power Down Tolerant (PDT) and Flexible Startup Sequencing (FSS) features, easing system design. They can drive both source-terminated and double terminated loads, operating up to 400MHz. The family offers 4,8,13,16,20 Low-Power (LP) HCSL output pairs in 4 × 4 mm to 10 x 10 mm packages. The RS2CB190xx devices offer higher output counts in smaller packages compared to earlier buffer families. The buffers support both Common Clock (CC) and Independent Reference (IR) PCIe clock architectures.

## Ordering Information

| Part Number | Number of Outputs | Differential Output Impedance (Ω) | Package | Operation Temperature |
|---|---|---|---|---|
| RS2CB19020ZDE | 20 | 85 | TQFN 10x10X0.85-72L | -40 to +105°C |
| RS2CB19020-100ZDE | 20 | 100 | | |
| RS2CB19016ZDE | 16 | 85 | TQFN 9X9X0.85-64L | -40 to +105°C |
| RS2CB19016-100ZDE | 16 | 100 | | |
| RS2CB19013ZLE | 13 | 85 | TQFN 7X7X0.85-56L | -40 to +105°C |
| RS2CB19013-100ZLE | 13 | 100 | | |
| RS2CB19008ZLAE | 8 | 85 | TQFN 5x5x0.85-40L | -40 to +105°C |
| RS2CB19008-100ZLAE | 8 | 100 | | |
| RS2CB19004ZWAE | 4 | 85 | QFN 4x4x0.85-28L | -40 to +105°C |
| RS2CB19004-100ZWAE | 4 | 100 | | |
| RS2CB19004BZWAE | 4 | 85 | QFN 4x4x0.85-28L | -40 to +105°C |
| RS2CB19004B-100ZWAE | 4 | 100 | | |

For RS2CB19004B，the AMPLITUDE_CTRL=0.75V.

## Block Diagram

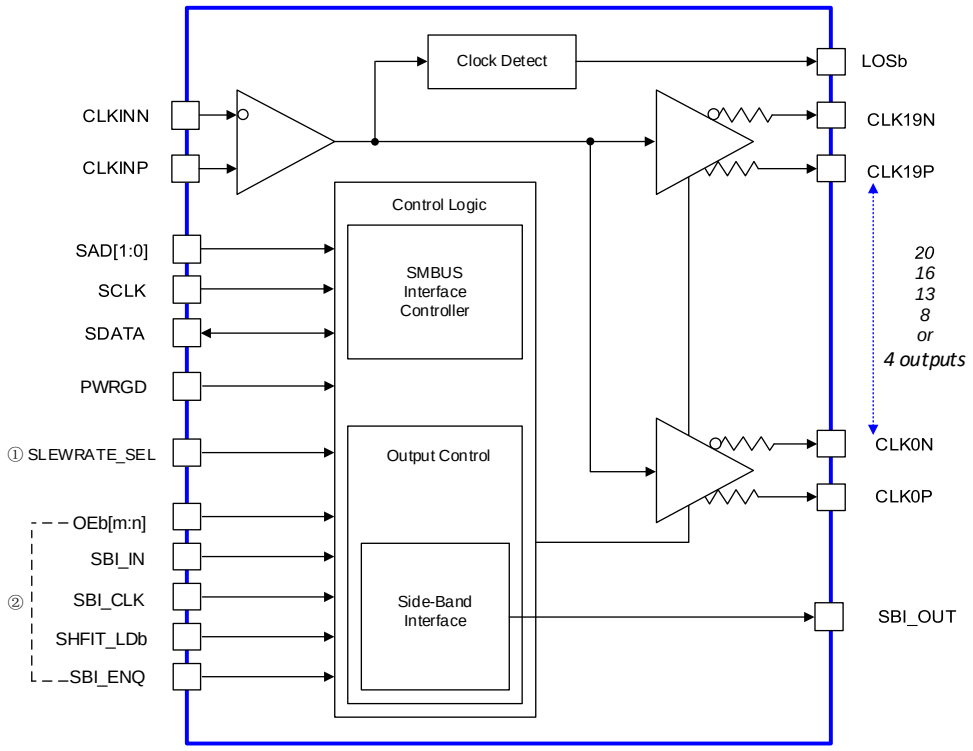



**Figure 1. RS2CB190xx Block Diagram**

1. RS2CB19016/13/08/04 only. Other devices use SMBus.
2. Some devices mux SBI with OEb pins. See specific pinouts. Devices with SBI have dedicated SBI_ENQ pin.

# 1. Pin Definition

## 1.1 Signal Types

| Term | Description |
|---|---|
| I | Input |
| O | Input |
| OD | Open Drain Output |
| I/O | Bi-Directional |
| PD | Pull-down |
| PU | Pull-up |
| Z | Tristate |
| D | Driven |
| X | Don't care |
| SE | Single ended |
| DIF | Differential |
| PWR | 3.3 V power |
| GND | Ground |
| PDT | Power Down Tolerant: These signals must tolerate being driven when the device is powered down. |

Note that some pins have both internal pull-up and pull-down resistors which bias the pins to VDD/2. Other pins are multi-mode and have an internal pull-up *or* internal pull-down depending on the mode.

## 1.2 RS2CB19020 Pin Configuration

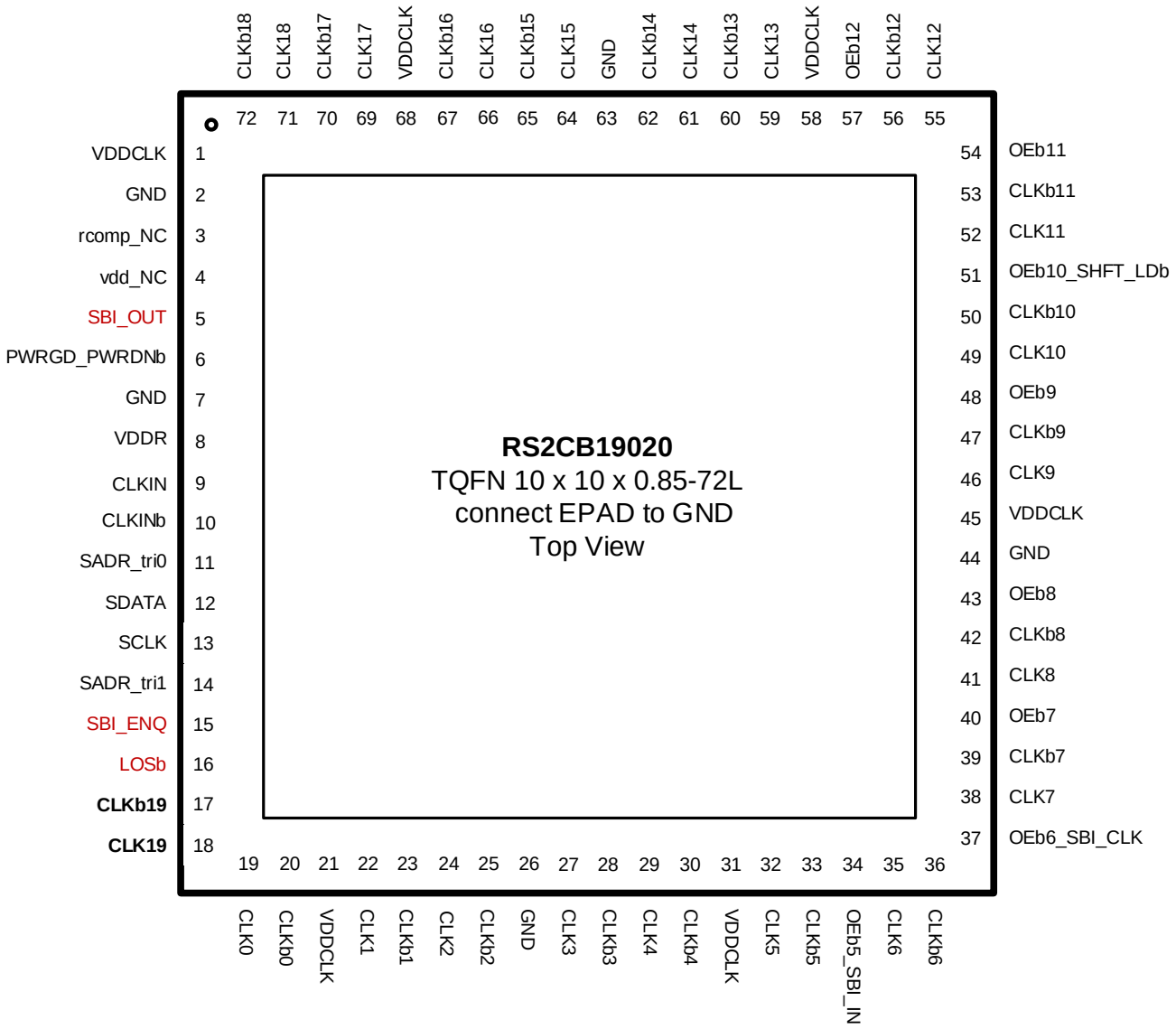



**Figure 2. RS2CB19020 TQFN-72L – Top View**

### 1.2.1 RS2CB19020 Pin Descriptions

**Table 1. RS2CB19020 Pin Descriptions**

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | VDDCLK | PWR | Power supply for clock outputs. |
| 2 | GND | GND | Ground pin. |
| 3 | rcomp_NC | NC | The DB2000Q specification calls this pin RCOMP. This pin is not connected by default. |
| 4 | vdd_NC | NC | The DB2000Q specification calls this pin VDD. This pin is not connected by default. |
| 5 | SBI_OUT | O, SE | Side-Band Interface data output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 6 | PWRGD_PWRDNb | I, SE, PU, PDT | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. |
| 7 | GND | GND | Ground pin. |
| 8 | VDDR | PWR | Power supply for clock input. |
| 9 | CLKIN | I, DIF, PDT | True clock input. |
| 10 | CLKINb | I, DIF, PDT | Complementary clock input. |
| 11 | SADR_tri0 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and refer to the tri-level input thresholds in the electrical tables. |
| 12 | SDATA | I/O, SE, OD, PDT | Data pin for SMBus interface. |
| 13 | SCLK | I, SE, PDT | Clock pin of SMBus interface. |
| 14 | SADR_tri1 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and refer to the tri-level input thresholds in the electrical tables. |
| 15 | SBI_ENQ | I, SE, PD, PDT | Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change.<br>0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins. |
| 16 | LOSb | O, OD, PDT | Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. |
| 17 | CLKb19 | O, DIF | Complementary clock output. |
| 18 | CLK19 | O, DIF | True clock output. |
| 19 | CLK0 | O, DIF | True clock output. |
| 20 | CLKb0 | O, DIF | Complementary clock output. |
| 21 | VDDCLK | PWR | Power supply for clock outputs. |
| 22 | CLK1 | O, DIF | True clock output. |
| 23 | CLKb1 | O, DIF | Complementary clock output. |
| 24 | CLK2 | O, DIF | True clock output. |
| 25 | CLKb2 | O, DIF | Complementary clock output. |
| 26 | GND | GND | Ground pin. |
| 27 | CLK3 | O, DIF | True clock output. |
| 28 | CLKb3 | O, DIF | Complementary clock output. |
| 29 | CLK4 | O, DIF | True clock output. |
| 30 | CLKb4 | O, DIF | Complementary clock output. |
| 31 | VDDCLK | PWR | Power supply for clock outputs. |
| 32 | CLK5 | O, DIF | True clock output. |
| 33 | CLKb5 | O, DIF | Complementary clock output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 34 | OEb5_SBI_IN | I, SE, PD, PDT | Active low input for enabling output 5 or the data pin for the Side-Band Interface. The function is this pin is controlled by the SBEN or SBI_ENQ pin. Refer to the Side-Band Interface (SBI) section for details.<br>OE mode:<br>0 = enable output, 1 = disable output. Side-Band mode with internal pull down: SBI shift register data input pin |
| 35 | CLK6 | O, DIF | True clock output. |
| 36 | CLKb6 | O, DIF | Complementary clock output. |
| 37 | OEb6_SBI_CLK | I, SE, PD, PDT | Active low input for enabling output 6 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBEN or SBI_ENQ pin. Refer to the Side- Band Interface (SBI) section for details.<br>OE mode:<br>0 = enable output, 1 = disable output. Side-Band mode with internal pull down:<br>Clocks data into the SBI shift register on the rising edge. |
| 38 | CLK7 | O, DIF | True clock output. |
| 39 | CLKb7 | O, DIF | Complementary clock output. |
| 40 | OEb7 | I, SE, PD, PDT | Active low input for enabling output 7. 0 = enable output, 1 = disable output. |
| 41 | CLK8 | O, DIF | True clock output. |
| 42 | CLKb8 | O, DIF | Complementary clock output. |
| 43 | OEb8 | I, SE, PD, PDT | Active low input for enabling output 8. 0 = enable output, 1 = disable output. |
| 44 | GND | GND | Ground pin. |
| 45 | VDDCLK | PWR | Power supply for clock outputs. |
| 46 | CLK9 | O, DIF | True clock output. |
| 47 | CLKb9 | O, DIF | Complementary clock output. |
| 48 | OEb9 | I, SE, PD, PDT | Active low input for enabling output 9. 0 = enable output, 1 = disable output. |
| 49 | CLK10 | O, DIF | True clock output. |
| 50 | CLKb10 | O, DIF | Complementary clock output. |
| 51 | OEb10_SHFT_LDb | I, SE, PD, PDT | Active low input for enabling output 10 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBEN or SBI_ENQ pin. Refer to the Side-Band Interface (SBI) section for details.<br>OE mode:<br>0 = enable output, 1 = disable output. Side-Band Mode with internal pull-down:<br>0 = Disable SBI shift register, 1 = Enable SBI shift register.<br>A falling edge transfers SBI shift register contents to SBI output control register. |
| 52 | CLK11 | O, DIF | True clock output. |
| 53 | CLKb11 | O, DIF | Complementary clock output. |
| 54 | OEb11 | I, SE, PD, PDT | Active low input for enabling output 11. 0 = enable output, 1 = disable output. |
| 55 | CLK12 | O, DIF | True clock output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 56 | CLKb12 | O, DIF | Complementary clock output. |
| 57 | OEb12 | I, SE, PD, PDT | Active low input for enabling output 12. 0 = enable output, 1 = disable output. |
| 58 | VDDCLK | PWR | Power supply for clock outputs. |
| 59 | CLK13 | O, DIF | True clock output. |
| 60 | CLKb13 | O, DIF | Complementary clock output. |
| 61 | CLK14 | O, DIF | True clock output. |
| 62 | CLKb14 | O, DIF | Complementary clock output. |
| 63 | GND | GND | Ground pin. |
| 64 | CLK15 | O, DIF | True clock output. |
| 65 | CLKb15 | O, DIF | Complementary clock output. |
| 66 | CLK16 | O, DIF | True clock output. |
| 67 | CLKb16 | O, DIF | Complementary clock output. |
| 68 | VDDCLK | PWR | Power supply for clock outputs. |
| 69 | CLK17 | O, DIF | True clock output. |
| 70 | CLKb17 | O, DIF | Complementary clock output. |
| 71 | CLK18 | O, DIF | True clock output. |
| 72 | CLKb18 | O, DIF | Complementary clock output. |
| 73 | EPAD | GND | Connect EPAD to Ground. |

## 1.3 RS2CB19016 Pin Assignments

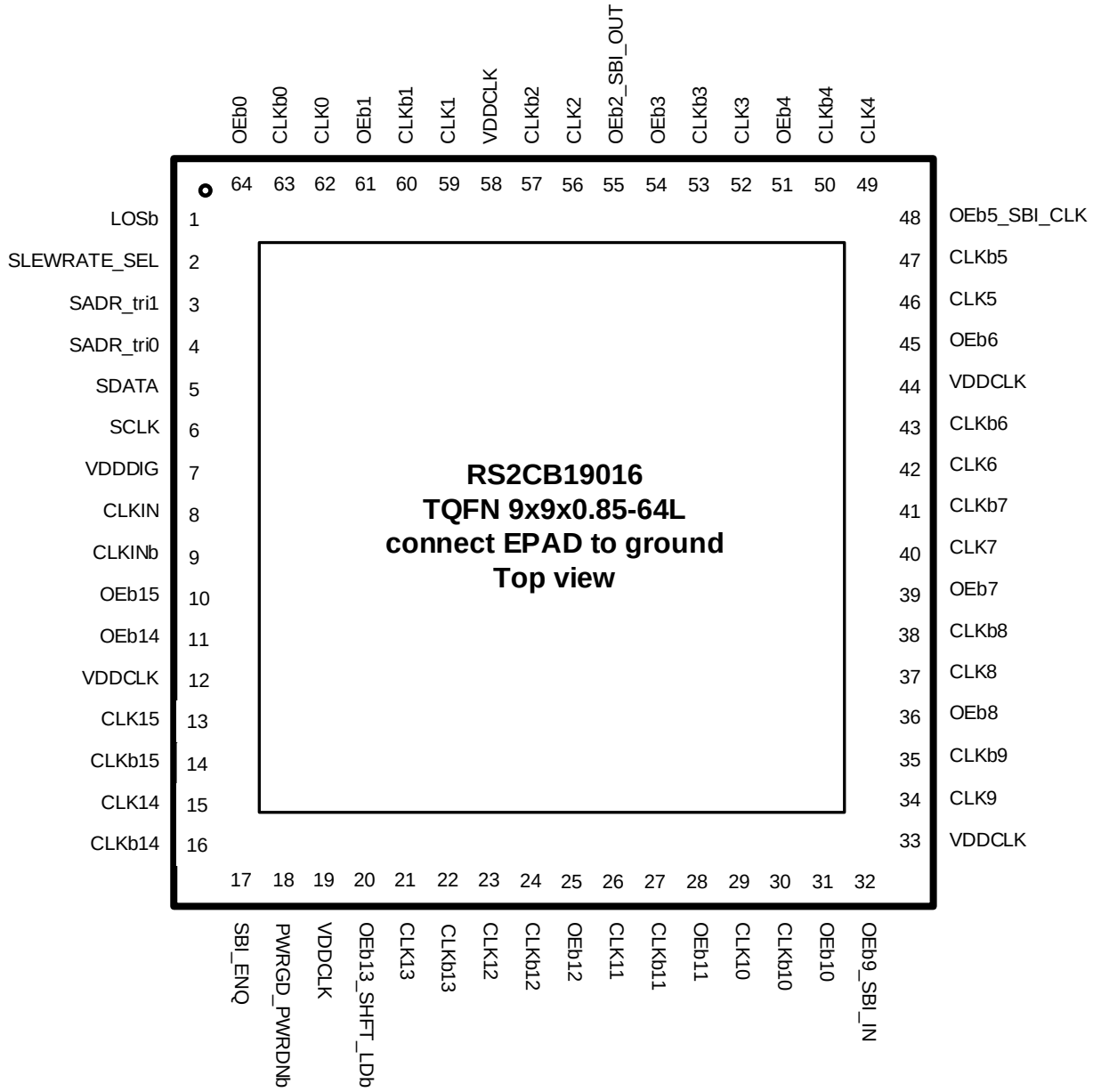



**Figure 3. RS2CB19016 TQFN-64L – Top View**

### 1.3.1 RS2CB19016 Pin Descriptions

**Table 2. RS2CB19016 Pin Descriptions**

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | LOSb | O, OD, PDT | Output indicating Loss of Input Signal. This pin is an open-drain output and requires an external pull-up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. |
| 2 | SLEWRATE_SEL | I, SE, PU, PDT | Input to select default slew rate of the outputs. 0 = Slow Slew Rate, 1 = Fast Slew Rate. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 3 | SADR_tri1 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 4 | SADR_tri0 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 5 | SDATA | I/O, SE, OD | Data pin for SMBus interface. |
| 6 | SCLK | I, SE | Clock pin of SMBus interface. |
| 7 | VDDDIG | PWR | Digital power. |
| 8 | CLKIN | I, DIF | True clock input. |
| 9 | CLKINb | I, DIF | Complementary clock input. |
| 10 | OEb15 | I, SE, PU, PDT | Active low input for enabling output 15. 0 = Enable output, 1 = Disable output. |
| 11 | OEb14 | I, SE, PU, PDT | Active low input for enabling output 14. 0 = Enable output, 1 = Disable output. |
| 12 | VDDCLK | PWR | Clock power supply. |
| 13 | CLK15 | O, DIF | True clock output. |
| 14 | CLKb15 | O, DIF | Complementary clock output. |
| 15 | CLK14 | O, DIF | True clock output. |
| 16 | CLKb14 | O, DIF | Complementary clock output. |
| 17 | SBI_ENQ | I, SE, PD, PDT | Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change.<br>0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins. |
| 18 | PWRGD_PWRDNb | I, SE, PU, PDT | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. |
| 19 | VDDCLK | PWR | Clock power supply. |
| 20 | OEb13_SHFT_LDb | I, SE, PU, PDT | Active low input for enabling output 13 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>0 = Disable SBI shift register, 1 = Enable SBI shift register.<br>A falling edge transfers SBI shift register contents to SBI output control register. |
| 21 | CLK13 | O, DIF | True clock output. |
| 22 | CLKb13 | O, DIF | Complementary clock output. |
| 23 | CLK12 | O, DIF | True clock output. |
| 24 | CLKb12 | O, DIF | Complementary clock output. |
| 25 | OEb12 | I, SE, PU, PDT | Active low input for enabling output 12. 0 = Enable output, 1 = Disable output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 26 | CLK11 | O, DIF | True clock output. |
| 27 | CLKb11 | O, DIF | Complementary clock output. |
| 28 | OEb11 | I, SE, PU, PDT | Active low input for enabling output 11. 0 = Enable output, 1 = Disable output. |
| 29 | CLK10 | O, DIF | True clock output. |
| 30 | CLKb10 | O, DIF | Complementary clock output. |
| 31 | OEb10 | I, SE, PU, PDT | Active low input for enabling output 10. 0 = Enable output, 1 = Disable output. |
| 32 | OEb9_SBI_IN | I, SE, PU, PDT | Active low input for enabling output 9 or the data pin for the Side-Band Interface. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode: SBI shift register data input pin |
| 33 | VDDCLK | PWR | Clock Power supply. |
| 34 | CLK9 | O, DIF | True clock output. |
| 35 | CLKb9 | O, DIF | Complementary clock output. |
| 36 | OEb8 | I, SE, PU, PDT | Active low input for enabling output 8. 0 = Enable output, 1 = Disable output. |
| 37 | CLK8 | O, DIF | True clock output. |
| 38 | CLKb8 | O, DIF | Complementary clock output. |
| 39 | OEb7 | I, SE, PU, PDT | Active low input for enabling output 7. 0 = Enable output, 1 = Disable output. |
| 40 | CLK7 | O, DIF | True clock output. |
| 41 | CLKb7 | O, DIF | Complementary clock output. |
| 42 | CLK6 | O, DIF | True clock output. |
| 43 | CLKb6 | O, DIF | Complementary clock output. |
| 44 | VDDCLK | PWR | Clock Power supply. |
| 45 | OEb6 | I, SE, PU, PDT | Active low input for enabling output 6. 0 = Enable output, 1 = Disable output. |
| 46 | CLK5 | O, DIF | True clock output. |
| 47 | CLKb5 | O, DIF | Complementary clock output. |
| 48 | OEb5_SBI_CLK | I, SE, PU, PDT | Active low input for enabling output 5 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode: Clocks data into the SBI on the rising edge. |
| 49 | CLK4 | O, DIF | True clock output. |
| 50 | CLKb4 | O, DIF | Complementary clock output. |
| 51 | OEb4 | I, SE, PU, PDT | Active low input for enabling output 4 0 = Enable output, 1 = Disable output. |
| 52 | CLK3 | O, DIF | True clock output. |
| 53 | CLKb3 | O, DIF | Complementary clock output. |
| 54 | OEb3 | I, SE, PU, PDT | Active low input for enabling output 3. 0 = Enable output, 1 = Disable output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 55 | OEb2_SBI_OUT | I/O, SE, PU, PDT | Active low input for enabling output 2 or the SBI shift register data output. The function is this pin is controlled by the SBI_ENQ. For more information, see Side- Band Interface (SBI). *Note: This pin is NOT PDT.*<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode: SBI shift register data output. |
| 56 | CLK2 | O, DIF | True clock output. |
| 57 | CLKb2 | O, DIF | Complementary clock output. |
| 58 | VDDCLK | PWR | Clock Power supply. |
| 59 | CLK1 | O, DIF | True clock output. |
| 60 | CLKb1 | O, DIF | Complementary clock output. |
| 61 | OEb1 | I, SE, PU, PDT | Active low input for enabling output 1. 0 = Enable output, 1 = Disable output. |
| 62 | CLK0 | O, DIF | True clock output. |
| 63 | CLKb0 | O, DIF | Complementary clock output. |
| 64 | OEb0 | I, SE, PU, PDT | Active low input for enabling output 0. 0 = Enable output, 1 = Disable output. |
| 65 | EPAD | GND | Ground pin. |

## 1.4 RS2CB19013 Pin Assignments

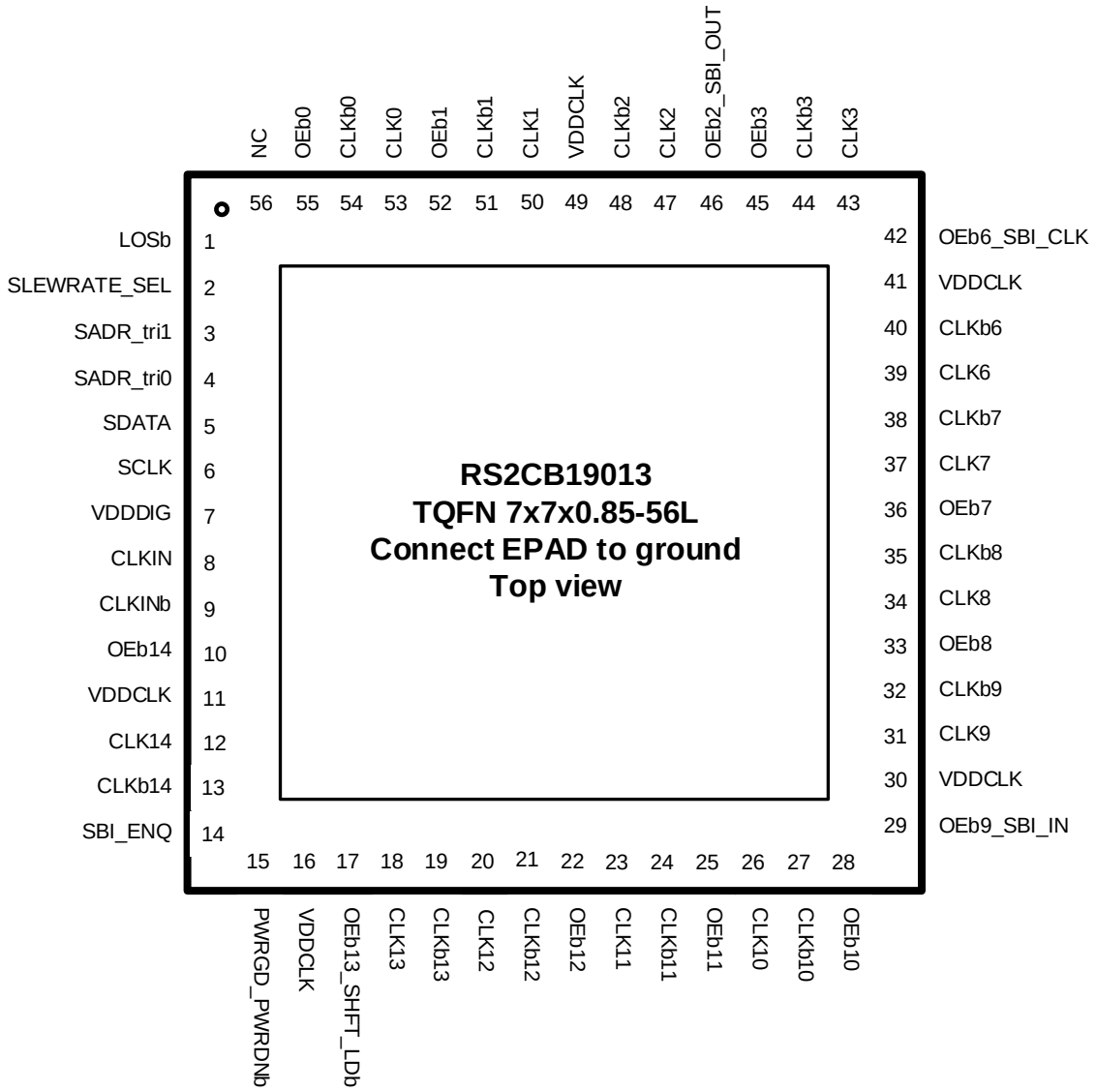



**Figure 4. RS2CB19013 TQFN-56L – Top View**

### 1.4.1 RS2CB19013 Pin Descriptions

**Table 3. RS2CB19013 Pin Descriptions**

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | LOSb | O, OD, PDT | Output indicating Loss of Input Signal. This pin is an open-drain output and requires an external pull-up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. |
| 2 | SLEWRATE_SEL | I, SE, PU, PDT | Input to select default slew rate of the outputs. 0 = Slow Slew Rate, 1 = Fast Slew Rate. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 3 | SADR_tri1 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 4 | SADR_tri0 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 5 | SDATA | I/O, SE, OD | Data pin for SMBus interface. |
| 6 | SCLK | I, SE | Clock pin of SMBus interface. |
| 7 | VDDDIG | PWR | Digital power. |
| 8 | CLKIN | I, DIF | True clock input. |
| 9 | CLKINb | I, DIF | Complementary clock input. |
| 10 | OEb14 | I, SE, PU, PDT | Active low input for enabling output 14. 0 = Enable output, 1 = Disable output. |
| 11 | VDDCLK | PWR | Clock power supply. |
| 12 | CLK14 | O, DIF | True clock output. |
| 13 | CLKb14 | O, DIF | Complementary clock output. |
| 14 | SBI_ENQ | I, SE, PD, PDT | Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change.<br>0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins. |
| 15 | PWRGD_PWRDNb | I, SE, PU, PDT | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. |
| 16 | VDDCLK | PWR | Clock power supply. |
| 17 | OEb13_SHFT_LDb | I, SE, PU, PDT | Active low input for enabling output 13 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>0 = Disable SBI shift register, 1 = Enable SBI shift register.<br>A falling edge transfers SBI shift register contents to SBI output control register. |
| 18 | CLK13 | O, DIF | True clock output. |
| 19 | CLKb13 | O, DIF | Complementary clock output. |
| 20 | CLK12 | O, DIF | True clock output. |
| 21 | CLKb12 | O, DIF | Complementary clock output. |
| 22 | OEb12 | I, SE, PU, PDT | Active low input for enabling output 12. 0 = Enable output, 1 = Disable output. |
| 23 | CLK11 | O, DIF | True clock output. |
| 24 | CLKb11 | O, DIF | Complementary clock output. |
| 25 | OEb11 | I, SE, PU, PDT | Active low input for enabling output 11. 0 = Enable output, 1 = Disable output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 26 | CLK10 | O, DIF | True clock output. |
| 27 | CLKb10 | O, DIF | Complementary clock output. |
| 28 | OEb10 | I, SE, PU, PDT | Active low input for enabling output 10. 0 = Enable output, 1 = Disable output. |
| 29 | OEb9_SBI_IN | I, SE, PU, PDT | Active low input for enabling output 9 or the data pin for the Side-Band Interface. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>SBI shift register data input pin |
| 30 | VDDCLK | PWR | Clock Power supply. |
| 31 | CLK9 | O, DIF | True clock output. |
| 32 | CLKb9 | O, DIF | Complementary clock output. |
| 33 | OEb8 | I, SE, PU, PDT | Active low input for enabling output 8. 0 = Enable output, 1 = Disable output. |
| 34 | CLK8 | O, DIF | True clock output. |
| 35 | CLKb8 | O, DIF | Complementary clock output. |
| 36 | OEb7 | I, SE, PU, PDT | Active low input for enabling output 7. 0 = Enable output, 1 = Disable output. |
| 37 | CLK7 | O, DIF | True clock output. |
| 38 | CLKb7 | O, DIF | Complementary clock output. |
| 39 | CLK6 | O, DIF | True clock output. |
| 40 | CLKb6 | O, DIF | Complementary clock output. |
| 41 | VDDCLK | PWR | Clock Power supply. |
| 42 | OEb6_SBI_CLK | I, SE, PU, PDT | Active low input for enabling output 6 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>Clocks data into the SBI on the rising edge. |
| 43 | CLK3 | O, DIF | True clock output. |
| 44 | CLKb3 | O, DIF | Complementary clock output. |
| 45 | OEb3 | I, SE, PU, PDT | Active low input for enabling output 3. 0 = Enable output, 1 = Disable output. |
| 46 | OEb2_SBI_OUT | I/O, SE, PU, PDT | Active low input for enabling output 2 or the SBI shift register data output. The function is this pin is controlled by the SBI_ENQ. For more information, see Side- Band Interface (SBI). *Note: This pin is NOT PDT.*<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>SBI shift register data output. |
| 47 | CLK2 | O, DIF | True clock output. |
| 48 | CLKb2 | O, DIF | Complementary clock output. |
| 49 | VDDCLK | PWR | Clock Power supply. |
| 50 | CLK1 | O, DIF | True clock output. |
| 51 | CLKb1 | O, DIF | Complementary clock output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 52 | OEb1 | I, SE, PU, PDT | Active low input for enabling output 1. 0 = Enable output, 1 = Disable output. |
| 53 | CLK0 | O, DIF | True clock output. |
| 54 | CLKb0 | O, DIF | Complementary clock output. |
| 55 | OEb0 | I, SE, PU, PDT | Active low input for enabling output 0. 0 = Enable output, 1 = Disable output. |
| 56 | NC | | |
| 57 | EPAD | GND | Ground pin. |

## 1.5 RS2CB19008 Pin Assignments

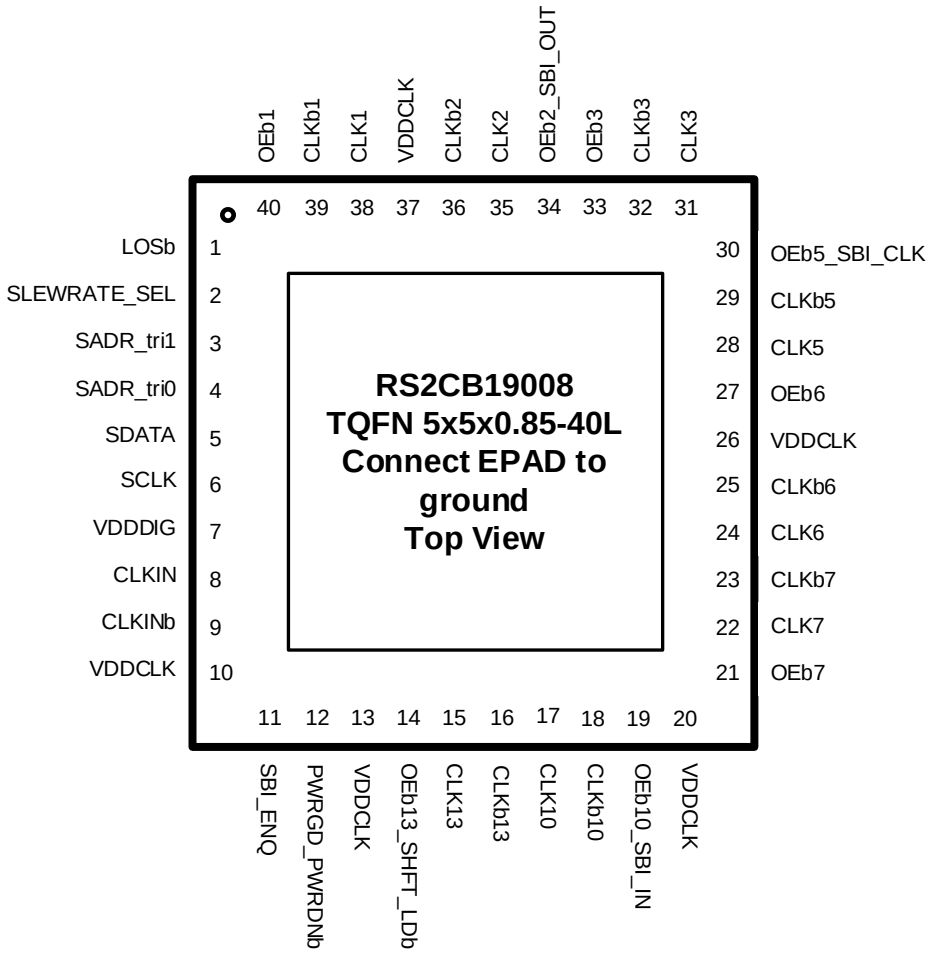



**Figure 5. RS2CB19008 TQFN-40L – Top View**

### 1.5.1 RS2CB19008 Pin Descriptions

**Table 4. RS2CB19008 Pin Descriptions**

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | LOSb | O, OD, PDT | Output indicating Loss of Input Signal. This pin is an open-drain output and requires an external pull-up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. |
| 2 | SLEWRATE_SEL | I, SE, PU, PDT | Input to select default slew rate of the outputs. 0 = Slow Slew Rate, 1 = Fast Slew Rate. |
| 3 | SADR_tri1 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 4 | SADR_tri0 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 5 | SDATA | I/O, SE, OD | Data pin for SMBus interface. |
| 6 | SCLK | I, SE | Clock pin of SMBus interface. |
| 7 | VDDDIG | PWR | Digital power. |
| 8 | CLKIN | I, DIF | True clock input. |
| 9 | CLKINb | I, DIF | Complementary clock input. |
| 10 | VDDCLK | PWR | Clock power supply. |
| 11 | SBI_ENQ | I, SE, PD, PDT | Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change.<br>0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins. |
| 12 | PWRGD_PWRDNb | I, SE, PU, PDT | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. |
| 13 | VDDCLK | PWR | Clock power supply. |
| 14 | OEb13_SHFT_LDb | I, SE, PU, PDT | Active low input for enabling output 13 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>0 = Disable SBI shift register, 1 = Enable SBI shift register.<br>A falling edge transfers SBI shift register contents to SBI output control register. |
| 15 | CLK13 | O, DIF | True clock output. |
| 16 | CLKb13 | O, DIF | Complementary clock output. |
| 17 | CLK10 | O, DIF | True clock output. |
| 18 | CLKb10 | O, DIF | Complementary clock output. |
| 19 | OEb10_SBI_IN | I, SE, PU, PDT | Active low input for enabling output 10 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode:<br>Clocks data into the SBI on the rising edge. |
| 20 | VDDCLK | PWR | Clock Power supply. |
| 21 | OEb7 | I, SE, PU, PDT | Active low input for enabling output 7. 0 = Enable output, 1 = Disable output. |
| 22 | CLK7 | O, DIF | True clock output. |
| 23 | CLKb7 | O, DIF | Complementary clock output. |
| 24 | CLK6 | O, DIF | True clock output. |
| 25 | CLKb6 | O, DIF | Complementary clock output. |
| 26 | VDDCLK | PWR | Clock Power supply. |
| 27 | OEb6 | I, SE, PU, PDT | Active low input for enabling output 6. 0 = Enable output, 1 = Disable output. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 28 | CLK5 | O, DIF | True clock output. |
| 29 | CLKb5 | O, DIF | Complementary clock output. |
| 30 | OEb5_SBI_CLK | I, SE, PU, PDT | Active low input for enabling output 5 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode: Clocks data into the SBI on the rising edge. |
| 31 | CLK3 | O, DIF | True clock output. |
| 32 | CLKb3 | O, DIF | Complementary clock output. |
| 33 | OEb3 | I, SE, PU, PDT | Active low input for enabling output 3. 0 = Enable output, 1 = Disable output. |
| 34 | OEb2_SBI_OUT | I/O, SE, PU, PDT | Active low input for enabling output 2 or the SBI shift register data output. The function is this pin is controlled by the SBI_ENQ. For more information, see Side- Band Interface (SBI). *Note: This pin is NOT PDT.*<br>OE mode:<br>0 = Enable output, 1 = Disable output. Side-Band mode: SBI shift register data output. |
| 35 | CLK2 | O, DIF | True clock output. |
| 36 | CLKb2 | O, DIF | Complementary clock output. |
| 37 | VDDCLK | PWR | Clock power supply. |
| 38 | CLK1 | O, DIF | True clock output. |
| 39 | CLKb1 | O, DIF | Complementary clock output. |
| 40 | OEb1 | I, SE, PU, PDT | Active low input for enabling output 1. 0 = Enable output, 1 = Disable output. |
| 41 | EPAD | GND | Ground pin. |

## 1.6 RS2CB19004 Pin Assignments

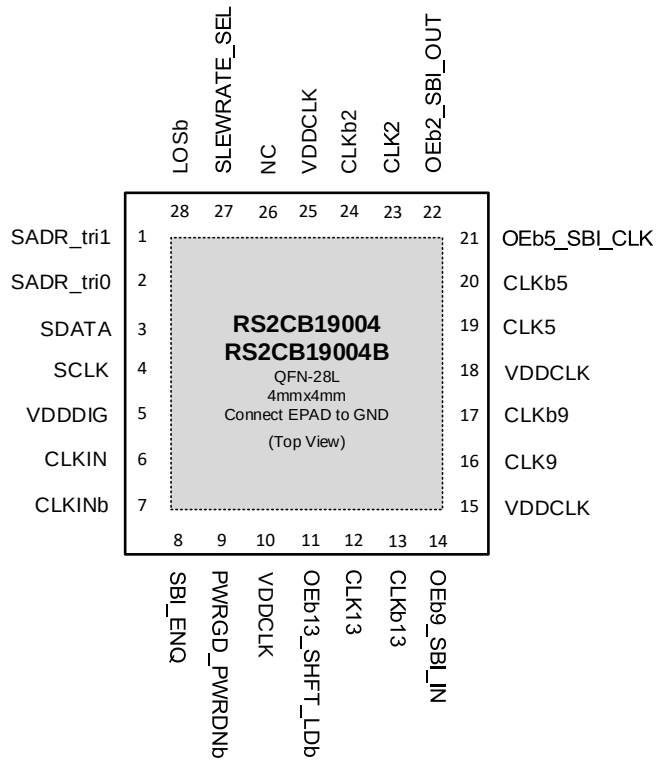



**Figure 6. RS2CB19004 TQFN-28L – Top View**

### 1.6.1 RS2CB19004 Pin Descriptions

**Table 5. RS2CB19004 Pin Descriptions**

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | SADR_tri1 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 2 | SADR_tri0 | I, SE, PD, PU | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables. |
| 3 | SDATA | I/O, SE, OD | Data pin for SMBus interface. |
| 4 | SCLK | I, SE | Clock pin of SMBus interface. |
| 5 | VDDDIG | PWR | Digital power. |
| 6 | CLKIN | I, DIF | True clock input. |
| 7 | CLKINb | I, DIF | Complementary clock input. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 8 | SBI_ENQ | I, SE, PD, PDT | Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change.<br>0 = SBI is disabled. Multiplexed pins function as output enables.<br>1 = SBI is enabled. Multiplexed pins function as SBI control pins. |
| 9 | PWRGD_PWRDNb | I, SE, PU, PDT | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. |
| 10 | VDDCLK | PWR | Clock power supply. |
| 11 | OEb13_SHFT_LDb | I, SE, PU or PD | Active low input for enabling output 13 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode with internal pull-up:<br>0 = Enable output, 1 = Disable output. Side-Band mode with internal pull-down:<br>0 = Disable SBI shift register, 1 = Enable SBI shift register. A falling edge transfers SBI shift register contents to SBI output control register. |
| 12 | CLK13 | O, DIF | True clock output. |
| 13 | CLKb13 | O, DIF | Complementary clock output. |
| 14 | OEb9_SBI_IN | I, SE, PDT, PU or PD | Active low input for enabling output 9 or the data pin for the Side-Band Interface. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>OE mode with internal pull-up:<br>0 = Enable output, 1 = Disable output.<br>Side-Band mode with internal pull-down: SBI shift register data input pin |
| 15 | VDDCLK | PWR | Clock power supply. |
| 16 | CLK9 | O, DIF | True clock output. |
| 17 | CLKb9 | O, DIF | Complementary clock output. |
| 18 | VDDCLK | PWR | Clock power supply. |
| 19 | CLK5 | O, DIF | True clock output. |
| 20 | CLKb5 | O, DIF | Complementary clock output. |
| 21 | OEb5_SBI_CLK | I, SE, PDT, PU or PD | Active low input for enabling output 5 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).OE mode with internal pull-up:<br>0 = Enable output, 1 = Disable output.<br>Side-Band mode with internal pull-down:Clocks data into the SBI on the rising edge. |

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 22 | OEb2_SBI_OUT | I/O, SE | Active low input for enabling output 2 or the SBI shift register data output. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI).<br>Note: This pin is NOT PDT.<br>OE mode with internal pull-up:<br>0 = Enable output, 1 = Disable output.<br>Side-Band mode:<br>SBI shift register data output. |
| 23 | CLK2 | O, DIF | True clock output. |
| 24 | CLKb2 | O, DIF | Complementary clock output. |
| 25 | VDDCLK | PWR | Clock power supply. |
| 26 | NC | NC | No connect. |
| 27 | SLEWRATE_SEL | I, SE, PU, PDT | Input to select default slew rate of the outputs.<br>0 = Slow Slew Rate, 1 = Fast Slew Rate. |
| 28 | LOSb | O, OD, PDT | Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. |
| 29 | EPAD | GND | Connect to ground. |

# 1. Specifications

## 1.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | MIN | MAX | Unit |
|---|---|---|---|---|---|
| $V_{DDx}$ | Supply Voltage with respect to Ground | Any VDD pin | -0.5 | 3.9 | V |
| $V_{IN}$ | Input Voltage | [1] | -0.5 | 3.9 | V |
| $V_{IN}$ | Input Voltage | [2] | -0.5 | $V_{DDx}$ + 0.3 | V |
| $I_{IN}$ | Input Current | All SE inputs and CLKIN [2] | - | ±50 | mA |
| $I_{OUT}$ | Output Current – Continuous | CLK | - | 30 | mA |
| | | SDATA, SBI_OUT | - | 25 | mA |
| | Output Current – Surge | CLK | - | 60 | mA |
| | | SDATA, SBI_OUT | - | 50 | mA |
| $T_J$ | Maximum Junction Temperature | - | - | 150 | °C |
| $T_S$ | Storage Temperature | Storage Temperature | -65 | 150 | °C |

1. Pins designated Power Down Tolerant (PDT) in the pin description tables.
2. Pins not designated Power Down Tolerant (PDT) in the pin description tables.

## 1.2 ESD Ratings

| Symbol | Parameter | Condition | Rating | Unit |
|---|---|---|---|---|
| ESD | HBM | JESD22-A114 (JS-001) Classification | 6000 | V |
| | CDM | JESD22-C101 Classification | 1000 | V |

## 1.3 Recommended Operation Conditions

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $T_J$ | Maximum Junction Temperature | - | - | - | 125 | °C |
| $T_A$ | Ambient Operating Temperature | - | -40 | 25 | 105 | °C |
| $V_{DDx}$ | Supply Voltage with respect to Ground | Any VDD pin, 3.3V ±10% supply. | 2.97 | 3.3 | 3.63 | V |
| $t_{PU}$ | Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | - | 0.05 | - | 5 | ms |

## 1.4 Thermal Information

| Package [1] | Symbol | Condition | TYP Value (°C/W) |
|---|---|---|---|
| TQFN 10x10X0.85-72L | θJc | Junction to Case | 16.9 |
| | θJb | Junction to Base | 2.7 |
| | θJA0 | Junction to Air, still air | 26.4 |
| | θJA1 | Junction to Air, 1 m/s air flow | 22.7 |
| | θJA3 | Junction to Air, 3 m/s air flow | 20.6 |
| | θJA5 | Junction to Air, 5 m/s air flow | 19.8 |
| TQFN 9X9X0.85-64L | θJc | Junction to Case | 24.6 |
| | θJb | Junction to Base | 2.7 |
| | θJA0 | Junction to Air, still air | 26.8 |
| | θJA1 | Junction to Air, 1 m/s air flow | 22.9 |
| | θJA3 | Junction to Air, 3 m/s air flow | 21.5 |
| | θJA5 | Junction to Air, 5 m/s air flow | 20.7 |
| TQFN 7X7X0.85-56L | θJc | Junction to Case | 26.6 |
| | θJb | Junction to Base | 3.4 |
| | θJA0 | Junction to Air, still air | 26.9 |
| | θJA1 | Junction to Air, 1 m/s air flow | 23.4 |
| | θJA3 | Junction to Air, 3 m/s air flow | 21.9 |
| | θJA5 | Junction to Air, 5 m/s air flow | 21 |
| TQFN 5x5x0.85-40L | θJc | Junction to Case | 37 |
| | θJb | Junction to Base | 4.8 |
| | θJA0 | Junction to Air, still air | 33.1 |
| | θJA1 | Junction to Air, 1 m/s air flow | 29.6 |
| | θJA3 | Junction to Air, 3 m/s air flow | 28 |
| | θJA5 | Junction to Air, 5 m/s air flow | 27.1 |
| TQFN 4x4x0.85-28L | θJc | Junction to Case | 45.3 |
| | θJb | Junction to Base | 2.2 |
| | θJA0 | Junction to Air, still air | 36.3 |
| | θJA1 | Junction to Air, 1 m/s air flow | 32.7 |
| | θJA3 | Junction to Air, 3 m/s air flow | 31.0 |
| | θJA5 | Junction to Air, 5 m/s air flow | 30.0 |

1. ePad soldered to board.

## 1.5 Electrical Characteristics

### 1.5.1 Phase Jitter

**Table 5. PCIe Refclk Phase Jitter - Normal Conditions [1][2][3][9]**

| Symbol | Parameter | Condition | TYP | MAX | Specification Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1-CC}$ | Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5% | PCIe Gen1 (2.5 GT/s) | 500 | 600 | 86000 | fs p-p |
| $t_{jphPCIeG2-CC}$ | | PCIe Gen2 Hi Band (5.0 GT/s) | 50 | 60 | 3,100 | fs RMS |
| | | PCIe Gen2 Lo Band (5.0 GT/s) | 10 | 20 | 3,000 | |
| $t_{jphPCIeG3-CC}$ | | PCIe Gen3 (8.0 GT/s) | 15 | 25 | 1,000 | |
| $t_{jphPCIeG4-CC}$ | | PCIe Gen4 (16.0 GT/s) [3] [4] | 15 | 25 | 500 | |
| $t_{jphPCIeG5-CC}$ | | PCIe Gen5 (32.0 GT/s) [3] [5] | 6 | 8 | 150 | |
| $t_{jphPCIeG6-CC}$ | | PCIe Gen6 (64.0 GT/s) [3] [6] | 5 | 6 | 100 | |
| $T_{jphPCIeG7-CC}$ | | PCIe Gen7 (128.0 GT/s) [3] [7] | 3 | 4 | 67 | |
| $t_{jphPCIeG2-IR}$ | Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC ≤ -0.3% | PCIe Gen2 (5.0 GT/s) | 40 | 50 | [8] | fs RMS |
| $t_{jphPCIeG3-IR}$ | | PCIe Gen3 (8.0 GT/s) | 15 | 25 | | |
| $t_{jphPCIeG4-IR}$ | | PCIe Gen4 (16.0 GT/s) | 15 | 25 | | |
| $t_{jphPCIeG5-IR}$ | | PCIe Gen5 (32.0 GT/s) | 5 | 6 | | |
| $t_{jphPCIeG6-IR}$ | | PCIe Gen6 (64.0 GT/s) | 4 | 5 | | |
| $t_{jphPCIeG7-IR}$ | | PCIe Gen7 (128.0 GT/s) | 3 | 4 | | |

1. The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 6.0, Revision 1.0*. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
9. The *PCI Express Base Specification 6.0, Revision 1.0* provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.
10. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns

**Table 6. Non-PCIe Refclk Phase Jitter [1][2][3]**

| Symbol | Parameter | Condition | TYP | MAX | Specification Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphDB2000Q}$ | Additive Phase Jitter - normal conditions [4] | 100MHz, Intel-supplied filter [3] | 15 | 18 | 80 [5] | fs RMS |
| $t_{jph12k-20M}$ | | 156.25MHz (12kHz to 20MHz) | 40 | 48 | N/A | |

1. See Test Loads for test configuration.
2. SMA100B used as signal source.
3. The RS2CB19xxx devices meet all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
4. Differential input swing = 1,600mV and input slew rate = 3.5V/ns.
5. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.

## 1.5.2 Output Frequencies, Startup Time, and LOS Timing

**Table 7. Output Frequencies, Startup Time, and LOS Timing**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $f_{OP}$ | Operating Frequency | Automatic Clock Parking (ACP) Circuit disabled | 1 | - | 400 | MHz |
| | | Automatic Clock Parking (ACP) Circuit enabled | 25 | - | 400 | |
| $t_{STARTUP}$ | Start-up Time | [1] | - | 1.2 | 3 | ms |
| $t_{STARTUP}$ | Start-up Time | [2] | - | 0.3 | 1 | ms |
| $t_{LATOEb}$ | OEb latency | OEb assertion/de-assertion CLK start/stop latency. Input clock must be running. | 4 | 5 | 10 | clks |
| $t_{LOSAssert}$ | LOS Assert Time | Time from disappearance of input clock to LOS assert. [3][4] | - | 123 | 200 | ns |
| $t_{LOSDeassert}$ | LOS De-assert Time | Time from appearance of input clock to LOS de-assert. [3][5] | - | 6 | 9 | clks |

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. PWRGD_PWRDNb tied to VDD in this case.
2. VDD stable, measured from de-assertion of PWRGD_PWRDNb.
3. The clock detect circuit does not qualify the accuracy of the input clock. The first input clock must appear to release the power on reset and enable the LOS circuit at power up.
4. PWRGD_PWRDNb high. The Automatic Clock Parking (ACP) circuit - if enabled - will park the outputs in a low/low state within this time. See Byte4, bit 4 LOSb_ACP_ENABLE.
5. PWRGD_PWRDNb high. The device will drive the outputs to a high/low state within this time and then begin clocking the outputs.

### 1.5.3 RS2CB19020 CLK Output AC/DC Characteristics

The tables in this section apply to the RS2CB19020.

**Table 8. RS2CB19020 85Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe [1]**

| Symbol | Parameter | Conditions | MIN | TYP | MAX | Specification Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{MAX}$ | Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4] | Across all settings in this table at 100MHz. | - | - | 1100 | 1150 | mV |
| $V_{MIN}$ | Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5] | | -160 | - | - | -300 | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 800mV. | 660 | 805 | 980 | - | |
| $V_{LOW}$ | Voltage Low [3] | | -90 | 30 | 150 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 800mV, scope averaging off. | 280 | 405 | 540 | 250 to 550 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | - | 20 | 100 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 800mV, Fast slew rate, scope averaging on. | 2.0 | 2.9 | 4.0 | 2 to 5 | V/ns |
| | | $V_{HIGH}$ set to 800mV, Slow slew rate, scope averaging on. | 1.6 | 2.4 | 3.4 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3] [11] | $V_{HIGH}$ set to 800mV. Fast slew rate. | - | 8 | 19 | 20 | % |
| | | $V_{HIGH}$ set to 800mV. Slow slew rate. | - | 10 | 24 | N/A | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 900mV. | 700 | 890 | 1080 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -110 | 30 | 160 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] [6][7] | $V_{HIGH}$ set to 900mV, scope averaging off. | 270 | 450 | 580 | 250 to 600 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3] [6][8] | | - | 30 | 110 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 900mV, Fast slew rate, scope averaging on. | 2.2 | 3 | 4.8 | 2 to 5 | V/ns |
| | | $V_{HIGH}$ set to 900mV, Slow slew rate, scope averaging on. | 1.6 | 2.6 | 3.4 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Fast slew rate. | - | 5 | 19 | 20 | % |
| | | $V_{HIGH}$ set to 900mV. Slow slew rate. | - | 8 | 26 | N/A | |
| $t_{DC}$ | Output Duty Cycle [9] | $V_T$ = 0V differential. 50% duty cycle input. | 48 | 50 | 52 | 45 to 55 | % |

1. Standard high impedance load with $C_L$ = 2pF. See Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.

6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 9. RS2CB19020 100Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe Apps [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Specification Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{MAX}$ | Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4] | Across all settings in this table at 100MHz. | - | - | 1050 | 1150 | mV |
| $V_{MIN}$ | Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5] | | -150 | - | - | -300 | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 800mV. | 710 | 815 | 915 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -35 | 20 | 75 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 800mV, scope averaging off. | 285 | 410 | 500 | 250 to 550 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | -25 | 35 | 105 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 800mV, Fast slew rate, scope averaging on. | 2.1 | 3 | 3.7 | 2 to 4 | V/ns |
| | | $V_{HIGH}$ set to 800mV, Slow slew rate, scope averaging on. | 1.6 | 2.6 | 3.4 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 800mV. Fast slew rate. | - | 4 | 16 | 20 | % |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 800mV. Slow slew rate. | - | 3.5 | 15.5 | 20 | % |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 900mV. | 802 | 907 | 1012 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -38 | 21 | 80 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 900mV, scope averaging off. | 320 | 450 | 540 | 300 to 600 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | -35 | 40 | 115 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 900mV, Fast slew rate, scope averaging on. | 2.1 | 3.0 | 3.9 | 2 to 4 | V/ns |
| | | $V_{HIGH}$ set to 900mV, Slow slew rate, scope averaging on. | 1.6 | 2.8 | 3.4 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Fast slew rate. | - | 5 | 19.7 | 20 | % |

**Table 9. RS2CB19020 100Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe Apps [1] (Cont.)**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Specification Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Slow slew rate. | - | 4.9 | 19.5 | 20 | % |
| $t_{DC}$ | Output Duty Cycle [9] | $V_T$ = 0V differential. | 48 | 50 | 52 | 45 to 55 | % |

1. Standard high impedance load with $C_L$= 2pF. For more information, see Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant **x86** processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 10. RS2CB19020 85Ω CLK AC/DC Characteristics - Non-PCIe, Source-Terminated Loads [1]**

| Symbol | Parameter | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 25MHz, 156.25MHz, 312.5MHz. | 630 | 800 | 1003 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -150 | 15 | 160 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 230 | 395 | 570 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | - | 50 | 140 | |
| $t_R$ | Rise Time [2]<br>$V_T$ = 20% to 80% of swing | | 135 | 480 | 780 | ps |
| $t_F$ | Fall Time [2]<br>$V_T$ = 20% to 80% of swing | | 155 | 425 | 748 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 25MHz, 156.25MHz, 312.5MHz. | 700 | 890 | 1100 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -155 | 30 | 195 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 260 | 430 | 640 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | - | 40 | 165 | |
| $t_R$ | Rise Time [2]<br>$V_T$ = 20% to 80% of swing | | 160 | 500 | 870 | ps |
| $t_F$ | Fall Time [2]<br>$V_T$ = 20% to 80% of swing | | 150 | 430 | 765 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 47 | 50 | 52 | % |

1. Standard high impedance load with $C_L$ = 2pF. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.

4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

**Table 11. RS2CB19020 85Ω CLK AC/DC Characteristics - Non-PCIe, Double-Terminated Loads [1]**

| Symbol | Parameter | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 25MHz, 156.25MHz, 312.5MHz (amplitude is reduced by ~50% due to double termination). | 370 | 430 | 475 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -30 | 11 | 60 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 150 | 215 | 245 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | - | 8 | 40 | |
| $t_R$ | Rise Time [2] $V_T$ = 20% to 80% of swing | | 205 | 320 | 570 | ps |
| $t_F$ | Fall Time [2] $V_T$ = 20% to 80% of swing | | 120 | 300 | 450 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz (amplitude is reduced by ~50% due to double termination). | 385 | 490 | 555 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -30 | 12 | 60 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 170 | 220 | 265 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | - | 8 | 45 | |
| $t_R$ | Rise Time [2] $V_T$ = 20% to 80% of swing | | 215 | 330 | 610 | ps |
| $t_F$ | Fall Time [2] $V_T$ = 20% to 80% of swing | | 140 | 310 | 400 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 49 | 50 | 51 | % |

1. Both Tx and Rx are terminated (double-terminated) with $C_L$ = 2pF. This reduces amplitude by 50%. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

**Table 12. RS2CB19020 100Ω CLK AC/DC Characteristics - Non-PCIe Apps, Source-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz) | 700 | 795 | 910 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -70 | 30 | 120 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 252 | 375 | 495 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | 0 | 35 | 135 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 205 | 320 | 590 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 145 | 315 | 585 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz) | 750 | 885 | 1020 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -80 | 20 | 145 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 260 | 400 | 545 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | 0 | 45 | 145 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_R$ | Rise Time [2]<br>VT = 20% to 80% of swing | | 200 | 390 | 610 | ps |
| $t_F$ | Fall Time [2]<br>VT = 20% to 80% of swing | | 120 | 325 | 595 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 48 | 50 | 52 | % |

1. Standard high impedance load with $C_L$= 2pF. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

**Table 13. RS2CB19020 100Ω CLK AC/DC Characteristics–Non-PCIe Apps, Double-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz) | 360 | 395 | 430 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -25 | 8 | 45 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 150 | 185 | 215 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | -12 | 10 | 30 | |
| $t_R$ | Rise Time [2]<br>VT = 20% to 80% of swing | | 150 | 310 | 557 | ps |
| $t_F$ | Fall Time [2]<br>VT = 20% to 80% of swing | | 110 | 260 | 380 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz) | 380 | 480 | 560 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -30 | 10 | 50 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 165 | 220 | 280 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | -18 | 10 | 30 | |
| $t_R$ | Rise Time [2]<br>VT = 20% to 80% of swing | | 170 | 320 | 610 | ps |
| $t_F$ | Fall Time [2]<br>VT = 20% to 80% of swing | | 130 | 305 | 400 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 48 | 50 | 52 | % |

1. Both Tx and Rx are terminated (double-terminated) with $C_L$= 2pF. This reduces amplitude by 50%. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

### 1.5.4 RS2CB190xx CLK Output AC/DC Characteristics

The tables in the section apply to the RS2CB19016, RS2CB19013, RS2CB19008，RS2CB19004.

**Table 14. RS2CB19016/13/08/04 85Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe Applications [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Specification Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{MAX}$ | Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4] | Across all settings in this table at 100MHz. | - | 870 | 968 | 1150 | mV |
| $V_{MIN}$ | Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5] | | -45 | 2 | 36 | -300 | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 800mV. | 710 | 795 | 869 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -45 | 31 | 108 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 800mV, scope averaging off. | 280 | 406 | 535 | 250 to 550 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | -32 | 30 | 136 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 800mV, Fast slew rate, scope averaging on. | 2.1 | 3.2 | 4.6 | 2 to 5 | V/ns |
| | | $V_{HIGH}$ set to 800mV, Slow slew rate, scope averaging on. | 1.6 | 2.3 | 3.2 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 800mV. Fast slew rate. | - | 5 | 20 | 25 | % |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 800mV. Slow slew rate. | - | 7 | 24 | 28 | % |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 900mV. | 750 | 880 | 960 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -44 | 32 | 112 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 900mV, scope averaging off. | 312 | 441 | 567 | 300 to 600 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | -45 | 33 | 140 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 900mV, Fast slew rate, scope averaging on. | 2.1 | 3.4 | 4.9 | 2 to 5 | V/ns |
| | | $V_{HIGH}$ set to 900mV, Slow slew rate, scope averaging on. | 1.6 | 2.4 | 3.3 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Fast slew rate. | - | 5 | 20 | 25 | % |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Slow slew rate. | - | 7 | 24 | 28 | % |
| $t_{DC}$ | Output Duty Cycle [9] | $V_T$ = 0V differential. | 48 | 50 | 52 | 45 to 55 | % |

1. Standard high impedance load with $C_L$= 2pF. For more information, see Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.

5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 25% of the slowest edge rate.

**Table 15. RS2CB19016/13/08/04 100Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe Apps [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Specification Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{MAX}$ | Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4] | Across all settings in this table at 100MHz. | 844 | 930 | 1017 | 1150 | mV |
| $V_{MIN}$ | Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5] | | -51 | 7 | 65 | -300 | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 800mV. | 713 | 816 | 918 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -35 | 22 | 78 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 800mV, scope averaging off. | 296 | 420 | 540 | 250 to 550 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | -28 | 39 | 106 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 800mV, Fast slew rate, scope averaging on. | 2.1 | 2.9 | 3.7 | 2 to 4 | V/ns |
| | | $V_{HIGH}$ set to 800mV, Slow slew rate, scope averaging on. | 1.6 | 2.4 | 3.2 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 800mV. Fast slew rate. | - | 3.6 | 15.6 | 20 | % |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 800mV. Slow slew rate. | - | 3.5 | 15.5 | 20 | % |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 900mV. | 802 | 907 | 1012 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -38 | 21 | 80 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 900mV, scope averaging off. | 326 | 454 | 560 | 300 to 600 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | -31 | 40 | 111 | 140 | |
| dv/dt | Slew Rate [9][10] | $V_{HIGH}$ set to 900mV, Fast slew rate, scope averaging on. | 2.1 | 3.0 | 4.0 | 2 to 4 | V/ns |
| | | $V_{HIGH}$ set to 900mV, Slow slew rate, scope averaging on. | 1.7 | 2.6 | 3.4 | 1.5 to 3.5 | |
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Fast slew rate. | - | 4.8 | 19.7 | 20 | % |

**Table 15. RS2CB19016/13/08/04 100Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe Apps [1] (Cont.)**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Specification Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta T_{R/F}$ | Rise/Fall Matching [3][11] | $V_{HIGH}$ set to 900mV. Slow slew rate. | - | 4.9 | 19.4 | 20 | % |
| $t_{DC}$ | Output Duty Cycle [9] | $V_T$ = 0V differential. | 48 | 50 | 52 | 45 o 55 | % |

1. Standard high impedance load with $C_L$= 2pF. For more information, see Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant **x86** processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 16. RS2CB19016/13/08/04 85Ω CLK AC/DC Characteristics - Non-PCIe Apps, Source-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz) | 695 | 811 | 950 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -52 | 30 | 108 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 283 | 431 | 582 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | 0 | 35 | 168 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 93 | 334 | 543 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 103 | 293 | 539 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz) | 744 | 901 | 1084 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -51 | 27 | 102 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 234 | 446 | 656 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | 0 | 35 | 168 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 65 | 386 | 683 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 82 | 302 | 565 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 48 | 50 | 52 | % |

1. Standard high impedance load with $C_L$= 2pF. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

**Table 17. RS2CB19016/13/08/04 85Ω CLK AC/DC Characteristics - Non-PCIe Apps, Double-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz) | 385 | 431 | 475 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -22 | 12 | 46 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 164 | 205 | 245 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | -19 | 10 | 40 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 185 | 396 | 615 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 185 | 253 | 355 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz) | 430 | 479 | 526 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -26 | 12 | 49 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 179 | 223 | 260 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | -24 | 10 | 45 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 259 | 456 | 670 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 197 | 256 | 345 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 48 | 49.8 | 52 | % |

1. Both Tx and Rx are terminated (double-terminated) with $C_L$ = 2pF. This reduces amplitude by 50%. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

**Table 18. RS2CB19016/13/08/04 100Ω CLK AC/DC Characteristics - Non-PCIe Apps, Source-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz) | 702 | 808 | 914 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -73 | 34 | 118 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 256 | 376 | 496 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | 0 | 37 | 133 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 217 | 376 | 467 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 140 | 365 | 576 | ps |
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz) | 756 | 890 | 1024 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -85 | 31 | 147 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 269 | 405 | 541 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | 0 | 47 | 144 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 222 | 412 | 610 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 127 | 368 | 591 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 48.2 | 48.9 | 52.1 | % |

1. Standard high impedance load with $C_L$= 2pF. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

**Table 19. RS2CB19016/13/08/04 100Ω CLK AC/DC Characteristics–Non-PCIe Apps, Double-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz) | 365 | 398 | 435 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -20 | 10 | 43 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 152 | 186 | 216 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | -14 | 7 | 29 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 237 | 409 | 634 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 174 | 260 | 380 | ps |

**Table 19. RS2CB19016/13/08/04 100Ω CLK AC/DC Characteristics–Non-PCIe Apps, Double-Terminated Loads [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $V_{HIGH}$ = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz) | 405 | 442 | 485 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -22 | 12 | 45 | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 167 | 201 | 232 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | -14 | 8 | 30 | |
| $t_R$ | Rise Time [2] VT = 20% to 80% of swing | | 280 | 467 | 695 | ps |
| $t_F$ | Fall Time [2] VT = 20% to 80% of swing | | 180 | 263 | 385 | ps |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings in this table, $V_T$ = 0V. | 48 | 50 | 52 | % |

1. Both Tx and Rx are terminated (double-terminated) with $C_L$ = 2pF. This reduces amplitude by 50%. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

## 1.5.5 Output-to-Output and Input-to-Output Skew

**Table 20. RS2CB19020 Output-to-Output and Input-to-Output Skew [1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $t_{SK}$ | Output-to-Output Skew [2] | Any two outputs, all outputs at fast slew rate. | - | 38 | 50 | ps |
| | | Any two outputs, all outputs at slow slew rate. | - | 40 | 60 | ps |
| $t_{PD}$ | Input-to-Output Delay Double-Terminated [3] | Clock in to any output, all outputs at fast slew rate. | 1.1 | 1.2 | 1.4 | ns |
| | | Clock in to any output, all outputs at slow slew rate. | 1.2 | 1.4 | 1.6 | ns |
| $t_{PD}$ | Input-to-Output Delay Source-Terminated [3] | Clock in to any output, all outputs at fast slew rate. | 1.2 | 1.4 | 1.6 | ns |
| | | Clock in to any output, all outputs at slow slew rate. | 1.4 | 1.5 | 1.8 | ns |
| $\Delta t_{PD}$ | Input-to-Output Delay Variation [3] | A single device, over temperature *and voltage*. | - | 1.4 | 2 | ps/°C |

1. For more information, see Test Loads.
2. This parameter is defined in accordance with JEDEC Standard 65.
3. Defined as the time between to output rising edge and the input rising edge that caused it.

**Table 21. RS2CB19016/13/08/04 Output-to-Output and Input-to-Output Skew[1]**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $t_{SK}$ | Output-to-Output Skew [2] | Any two outputs, all outputs at fast slew rate. | - | 37 | 50 | ps |
| | | Any two outputs, all outputs at slow slew rate. | - | 39 | 60 | ps |
| $t_{PD}$ | Input-to-Output Delay Double-Terminated [3] | Clock in to any output, all outputs at fast slew rate. | 1.1 | 1.4 | 1.6 | ns |
| | | Clock in to any output, all outputs at slow slew rate. | 1.2 | 1.5 | 1.8 | ns |
| $t_{PD}$ | Input-to-Output Delay Source-Terminated [3] | Clock in to any output, all outputs at fast slew rate. | 1.2 | 1.4 | 1.7 | ns |
| | | Clock in to any output, all outputs at slow slew rate. | 1.3 | 1.5 | 1.8 | ns |
| $\Delta t_{PD}$ | Input-to-Output Delay Variation [3] | A single device, over temperature *and voltage*. | - | 1.5 | 1.8 | ps/°C |

1. For more information, see Test Loads.
2. This parameter is defined in accordance with JEDEC Standard 65.
3. Defined as the time between to output rising edge and the input rising edge that caused it.

## 1.5.6 I/O Signals

**Table 22. I/O Electrical Characteristics**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage [1][2] | Single-ended inputs, unless otherwise listed. | 2 | - | VDD + 0.3 | V |
| $V_{IL}$ | Input Low Voltage [1][2] | | -0.3 | - | 0.8 | V |
| $V_{IH}$ | Input High Voltage | SADR_tri[1:0]. | 2.4 | - | VDD+0.3 | V |
| $V_{IM}$ | Input Mid Voltage | | 1.2 | - | 1.8 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | - | 0.8 | V |
| $V_{OH}$ | Output High Voltage [2] | SBI_OUT, IOH = -2mA | 2.4 | 3.2 | VDD + 0.3 | V |
| $V_{OL}$ | Output Low Voltage [2] | SBI_OUT, IOL = 2mA | - | 0.1 | 0.4 | V |
| $I_{IH}$ | Input Leakage Current High, $V_{IN}$ = VDD | CLKIN (RS2CB19020) | - | - | 70 | µA |
| | | CLKINb (RS2CB19020) | - | - | 70 | |
| | | CLKIN (RS2CB19016/13/08/04) | - | - | 70 | |
| | | CLKINb (RS2CB19016/13/08/04) | - | - | 70 | |
| | | Single-ended inputs, unless otherwise listed. | 25 | - | 35 | |
| | | PWRGD_PWRDNb | -1 | - | 5 | |
| | | SADR_tri[1:0] | 25 | - | 35 | |

**Table 23. I/O Electrical Characteristics (Cont.)**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current Low, $V_{IN}$ = 0V | CLKIN (RS2CB19020) | -12 | - | -6 | µA |
| | | CLKINb (RS2CB19020) | -3 | - | +3 | |
| | | CLKIN (RS2CB19016/13/08/04) | -3 | - | +3 | |
| | | CLKINb (RS2CB19016/13/08/04) | -12 | - | -6 | |
| | | Single-ended inputs, unless otherwise listed. | -3 | - | +3 | |
| | | PWRGD_PWRDNb | -35 | - | -20 | |
| | | SADR_tri[1:0] | -35 | - | -20 | |
| Rp | PD_CLKIN | Value of internal pull-down resistor to ground (CLKIN) | - | 53 | - | kΩ |
| | PU_CLKINb | Value of internal pull-up resistor to 0.5V (CLKINb). | - | 57 | - | |
| | Pull-up/Pull-down Resistor | Single-ended inputs. | - | 125 | - | |
| Zo | Output Impedance | SBI_OUT pin. | - | 50 | - | Ω |
| | | CLK outputs, RS2CB190xx (single-ended value). | - | 41 | - | Ω |
| | | CLK outputs, RS2CB190xx-**100** (single-ended value). | - | 48 | - | Ω |

1. For SCLK and SDATA, see the SMBus Electrical Characteristics table.
2. These values are compliant with JESD8C.01.

### 1.5.7 Power Supply Current

**Table 24. Power Supply Current [1][2][3] (Cont.)**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19020 | 85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 155 | 175 | mA |
| | | 85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 190 | 205 | |
| | | 85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 160 | 180 | |
| | | 85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 200 | 220 | |
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19016 | 85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 154 | 175 | mA |
| | | 85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 210 | 231 | |
| | | 85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 270 | 291 | |
| | | 85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 336 | 357 | |
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19013 | 85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 110 | 131 | mA |
| | | 85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 174 | 194 | |
| | | 85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 215 | 236 | |
| | | 85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 276 | 297 | |

**Table 24. Power Supply Current [1][2][3] (Cont.)**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19008 | 85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 72 | 92 | mA |
| | | 85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 116 | 137 | |
| | | 85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 126 | 146 | |
| | | 85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 183 | 203 | |
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19004 | 85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 39 | 59 | mA |
| | | 85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 60 | 80 | |
| | | 85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 79 | 100 | |
| | | 85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 102 | 122 | |
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19016-100 | 100Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 151 | 172 | mA |
| | | 100Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 187 | 208 | |
| | | 100Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 265 | 285 | |
| | | 100Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 303 | 323 | |
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19013-100 | 100Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 97 | 117 | mA |
| | | 100Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 160 | 180 | |
| | | 100Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 194 | 214 | |
| | | 100Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 257 | 278 | |

**Table 24. Power Supply Current [1][2][3] (Cont.)**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19008-100 | 100Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 70 | 90 | mA |
| | | 100Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 106 | 126 | |
| | | 100Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 121 | 142 | |
| | | 100Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 169 | 190 | |
| $I_{DDCLK}$ | $V_{DDCLK}$ Operating Current – RS2CB19004-100 | 100Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 38 | 59 | mA |
| | | 100Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1. | - | 59 | 79 | |
| | | 100Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 74 | 94 | |
| | | 100Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1. | - | 97 | 118 | |
| $I_{DDDIG}$ | $V_{DDDIG}$ Operating Current | PWRGD_PWRDNb = 1, RS2CB19016/13/08/04 | - | 0.6 | 1.3 | mA |
| $I_{DDR}$ | $V_{DDR}$ Operating Current – RS2CB19020 | 85Ω impedance, fast slew rate, at 100MHz. PWRGD_PWRDNb = 1. | - | 35 | 40 | mA |
| | | 85Ω impedance, fast slew rate, at maximum output frequency. PWRGD_PWRDNb = 1. | - | 90 | 100 | mA |
| $I_{DDCLK_PD}$ | $V_{DDCLK}$ Power-down Current | PWRGD_PWRDNb = 0, RS2CB19016/13/08/04 | - | 0.6 | 1.3 | mA |
| | | PWRGD_PWRDNb = 0, RS2CB19020 | - | 0.25 | 0.5 | mA |
| $I_{DDDIG_PD}$ | $V_{DDDIG}$ Power-down Current | PWRGD_PWRDNb = 0, RS2CB19016/13/08/04 | - | 3.1 | 5.0 | mA |
| $I_{DDR_PD}$ | $V_{DDR}$ Power-down Current | PWRGD_PWRDNb = 0, RS2CB19020 | - | 4.8 | 6 | mA |

1. For more information, see Test Loads.
2. Output voltage set to 800mV. Slew rate has negligible effect on current consumption, so only fast is listed.
3. Total operating current is obtained by adding IDDCLK + IDDDIG, or IDDCLK + IDDR for a particular device and operating mode. Power down current is obtained by adding IDDCLK_PD + IDDDIG_PD, or IDDCLK_PD + IDDR_PD for a particular device.

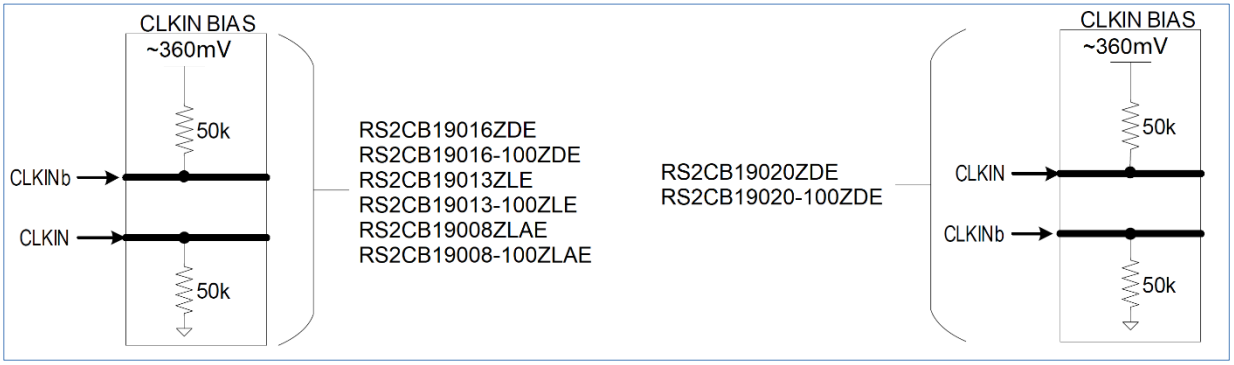
### 1.5.8 CLKIN AC/DC Characteristics

**Table 25. CLKIN AC/DC Characteristic**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{CROSS}$ | Input Crossover Voltage | - | 100 | - | 1400 | mV |
| $V_{SWING}$ | Input Swing | Differential value. | 200 | - | - | mV |
| dv/dt | Input Slew Rate | Measured differentially. [2] | 0.6 | - | - | V/ns |

1. For values required for performance, see the Phase Jitter tables.
2. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

**Figure 6. Clock Input Bias Network**




### 1.5.9 SMBus Electrical Characteristics

**Table 26. SMBus DC Electrical Characteristics [1]**

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level Input Voltage for SMBCLK and SMBDAT | - | 0.8 VDD | - | - | V |
| $V_{IL}$ | Low-level Input Voltage for SMBCLK and SMBDAT | - | - | - | 0.3 VDD | |
| $V_{HYS}$ | Hysteresis of Schmitt Trigger Inputs | - | 0.05 VDD | - | - | |
| $V_{OL}$ | Low-level Output Voltage for SMBCLK and SMBDAT | $I_{OL}$ = 4mA | - | 0.28 | 0.4 | |
| $I_{IN}$ | Input Leakage Current per Pin | - | [2] | - | [2] | µA |
| $C_B$ | Capacitive Load for Each Bus Line | - | - | - | 400 | pF |

1. $V_{OH}$ is governed by the $V_{PUP}$, the voltage rail to which the pull-up resistors are connected.
2. For more information, see I/O Electrical Characteristics.

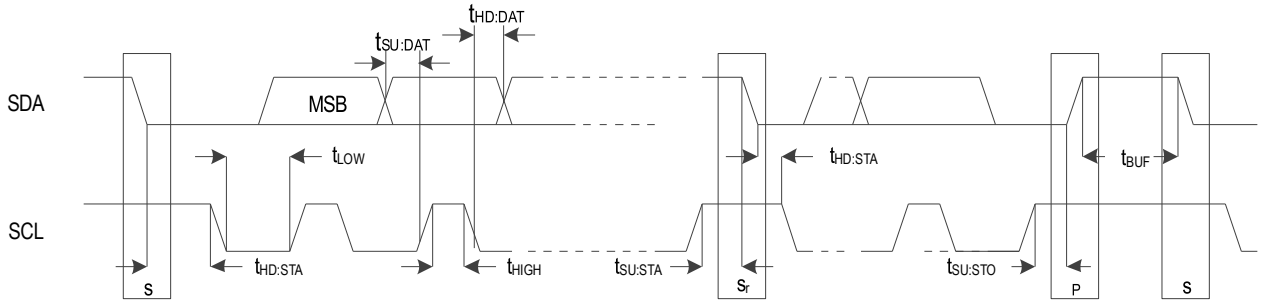



**Figure 7. SMBus Slave Timing**

**Table 27. SMBus AC Electrical Characteristics**

| Symbol | Parameter | Condition | 100kHz | | 400kHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{SMB}$ | SMBus Operating Frequency | [1] | 10 | 100 | 10 | 400 | kHz |
| $t_{BUF}$ | Bus free time between STOP and START Condition | - | 4.7 | - | 1.3 | - | µs |
| $t_{HD:STA}$ | Hold Time after (REPEATED) START Condition | [2] | 4 | - | 0.6 | - | µs |
| $t_{SU:STA}$ | REPEATED START Condition Setup Time | - | 4.7 | - | 0.6 | - | µs |
| $t_{SU:STO}$ | STOP Condition Setup Time | - | 4 | - | 0.6 | - | µs |
| $t_{HD:DAT}$ | Data Hold Time | [3] | 300 | - | 300 | - | ns |
| $t_{SU:DAT}$ | Data Setup Time | - | 250 | - | 100 | - | ns |
| $t_{TIMEOUT}$ | Detect SCL_SCLK Low Timeout | [4] | 25 | 35 | 25 | 35 | ms |
| $t_{TIMEOUT}$ | Detect SDA_nCS Low Timeout | [5] | 25 | 35 | 25 | 35 | ms |
| $t_{LOW}$ | Clock Low Period | - | 4.7 | - | 1.3 | - | µs |
| $t_{HIGH}$ | Clock High Period | [6] | 4 | 50 | 0.6 | 50 | µs |
| $t_{LOW:SEXT}$ | Cumulative Clock Low Extend Time - Slave | [7] | N/A | | N/A | | ms |
| $t_{LOW:MEXT}$ | Cumulative Clock Low Extend Time - Master | [8] | N/A | | N/A | | ms |
| $t_F$ | Clock/Data Fall Time | [9] | - | 300 | - | 300 | ns |
| $t_R$ | Clock/Data Rise Time | [9] | - | 1000 | - | 300 | ns |
| $t_{SPIKE}$ | Noise Spike Suppression Time | [10] | - | – | 0 | 50 | ns |

1. Power must be applied and PWRGD_PWRDNb must be a 1 for the SMBus to be active.
2. A master should not drive the clock at a frequency below the minimum $f_{SMB}$. Further, the operating clock frequency should not be reduced below the minimum value of fSMB due to periodic clock extending by slave devices as defined in Section 5.3.3 of System Management Bus (SMBus) Specification, Version 3.1, dated 19 Mar 2018. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW:SEXT}$ and $t_{LOW:MEXT}$ limits. For example, if the SMBCLK is high for $t_{HIGH,MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB,MIN} – t_{HIGH,MAX}$. This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100 µs in a non-periodic way.
3. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the VIH,MIN of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
4. Slave devices may have caused other slave devices to hold SDA low. This is the maximum time that a device can hold SMBDAT low after the master raises SMBCLK after the last bit of a transaction. A slave device may detect how long SDA is held low and release SDA after the time out period.
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT,MAX}$ or longer.
6. The device has the option of detecting a timeout if the SMBDATA pin is also low for this time.
7. $t_{HIGH,MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.
8. tLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a slave device or another master will also extend the clock causing the combined clock low time to be greater than tLOW:MEXT on a given byte. This parameter is measured with a full speed slave device as the sole target of the master.
9. The rise and fall time measurement limits are defined as follows:
   Rise Time Limits: ($V_{IL:MAX}$ - 0.15 V) to ($V_{IH:MIN}$ + 0.15 V)
   Fall Time Limits: ($V_{IH:MIN}$ + 0.15 V) to ($V_{IL:MAX}$ - 0.15 V)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

### 1.5.10 Side-Band Interface

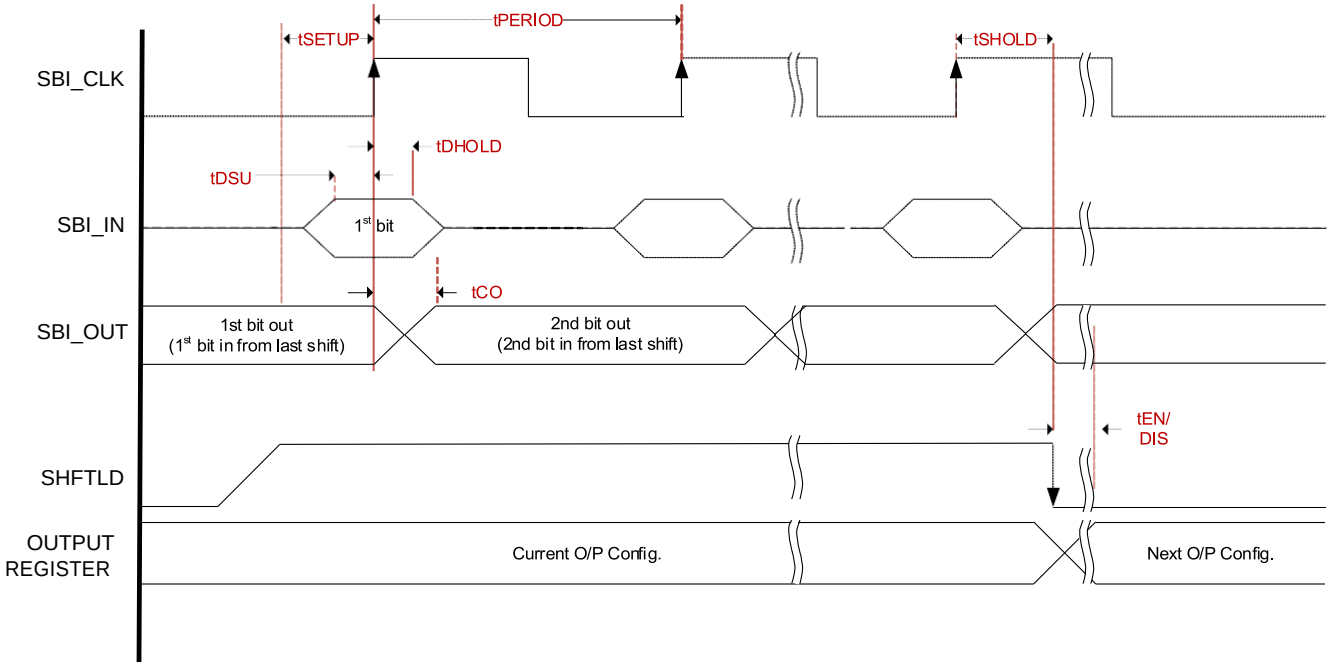



**Figure 8. Side-Band Interface Timing**

Figure 8 is the timing diagram and Table 28 provides the electrical characteristics for the Side-Band Interface. The SBI supports clock rates up to 25MHz.

**Table 28. Electrical Characteristics – Side-Band Interface**

| Symbol | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $t_{PERIOD}$ | Clock Period | Clock period. | 40 | - | - | ns |
| $t_{SETUP}$ | SHFT Setup Time to Clock | SHFT_LDB high to SBI_CLK rising edge. | 10 | - | - | ns |
| $t_{DSU}$ | SBI_IN Setup Time | SBI_IN setup to SBI_CLK rising edge. | 5 | - | - | ns |
| $t_{DHOLD}$ | SBI_IN Hold Time | SBI_IN hold after SBI_CLK rising edge. | 2 | - | - | ns |
| $t_{CO}$ | SBI_CLK to SBI_OUT | SBI_CLK rising edge to SBI_OUT valid. | 2 | - | - | ns |
| $t_{SHOLD}$ | SHFT Hold Time | SHFT_LDB hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LDB falling edge). | 10 | - | - | ns |
| $t_{EN/DIS}$ | Enable/Disable Time | Delay from SHFT_LDB falling edge to next output configuration taking effect.[1] | 4 | - | 12 | clocks |
| $t_{SLEW}$ | Slew Rate | SBI_CLK (between 20% and 80%).[2] | 0.7 | - | 6 | V/ns |

1. Refers to the output clock.
2. Control input must be monotonic from 20% to 80% of input swing.

# 3. Test Loads

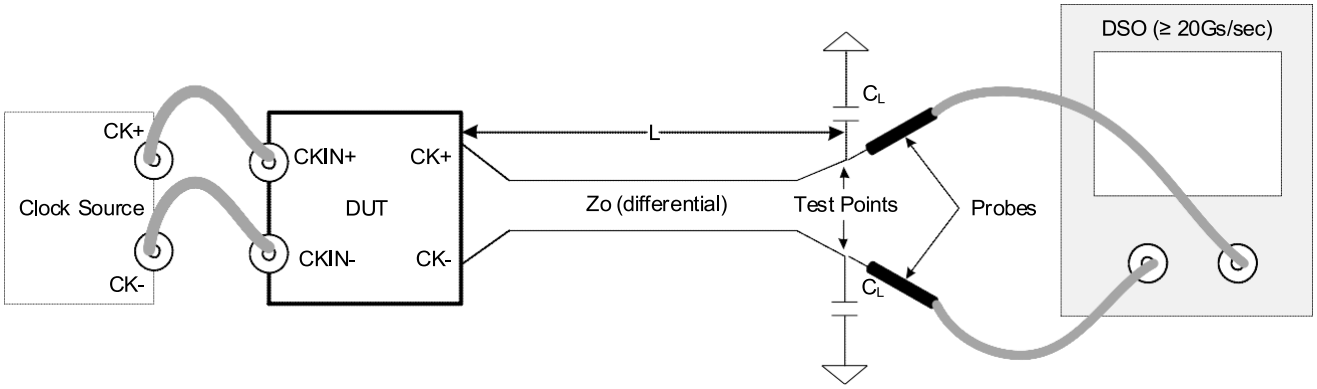



**Figure 9. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)**

**Table 29. Parameters for AC/DC Test Load (Standard PCIe Source-Terminated)**

| Device | Clock Source | Rs (ohms) | Zo (ohms) | L (cm) | $C_L$ (pF) |
|---|---|---|---|---|---|
| RS2CB19xxx | SMA100B | Internal | 85 | 25.4 | 2 |
| RS2CB19xxx-100 | SMA100B | Internal | 100 | 25.4 | 2 |

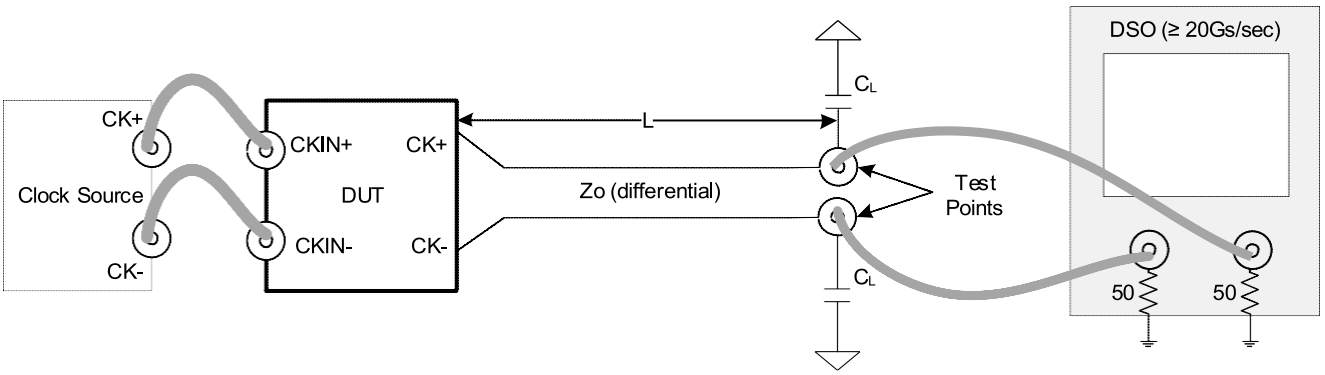



**Figure 10. AC/DC Test Load for Differential Outputs (Double-Terminated)**

**Table 30. Parameters for AC/DC Test Load (Double-Terminated)**

| Device | Clock Source | Rs (ohms) | Zo (ohms) | L (cm) | $C_L$ (pF) |
|---|---|---|---|---|---|
| RS2CB19xxx | SMA100B | Internal | 85 | 25.4 | 2 |
| RS2CB19xxx-100 | SMA100B | Internal | 100 | 25.4 | 2 |

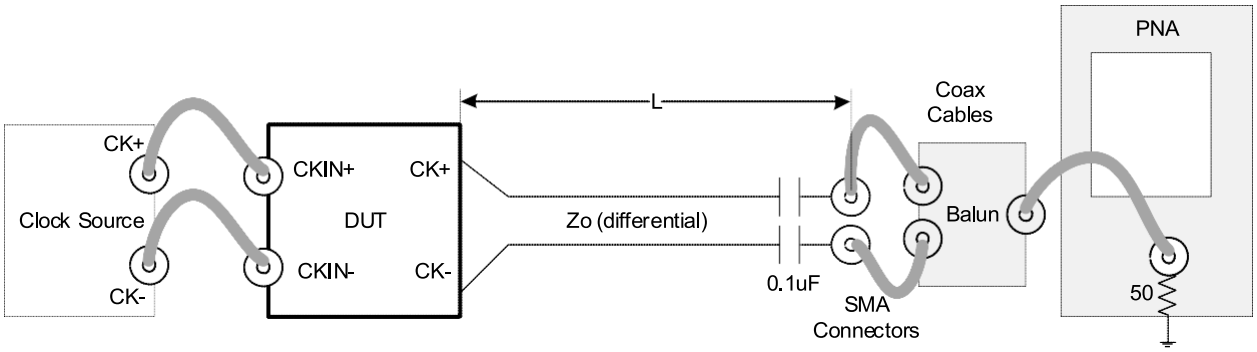



**Figure 11. Test Load for PCIe Phase Jitter Measurements**

**Table 31. Parameters for PCIe Gen5 Jitter Measurement**

| Device | Clock Source | Rs (ohms) | Zo (ohms) | L (cm) [1] | $C_L$ (pF) |
|---|---|---|---|---|---|
| RS2CB19xxx | SMA100B | Internal | 85 | 25.4 | 2 |
| RS2CB19xxx-**100** | SMA100B | Internal | 100 | 25.4 | 2 |

1. PCIe Gen6 specifies L = 0cm for 32 and 64 GT/s. L = 25.4cm is more conservative.

# 4. SMBus Interface

## 4.1 Write Sequence

- Controller (host) sends a start bit
- Controller (host) sends the write address
- RS2CB190xx clock will **acknowledge**
- Controller (host) sends the beginning byte Location= N
- RS2CB190xx clock will **acknowledge**
- Controller (host) sends the byte count = X
- RS2CB190xx clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- RS2CB190xx clock will **acknowledge** each byte one at a time
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **RS2CB190xx (Slave/Receiver)** |
| T | start bit | | |
| Slave Address | | | |
| WR | Write | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stop bit | | |

## 4.2 Read Sequence

- Controller (host) will send a start bit
- Controller (host) sends the write address
- RS2CB190xx clock will **acknowledge**
- Controller (host) sends the beginning byte Location= N
- RS2CB190xx clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- RS2CB190xx clock will **acknowledge**
- RS2CB190xx clock will send the data byte count = X
- RS2CB190xx clock sends Byte **N+X-1**
- RS2CB190xx clock sends **Byte L through Byte X (if X(H) was written to Byte 7)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **RS2CB190xx (Slave/Receiver)** |
| T | start bit | | |
| Slave Address | | | |
| WR | Write | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat start | | |
| Slave Address | | | |
| RD | Read | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not | | |
| P | stop bit | | |

## 4.3 SMBus Bit Types

| Bit Description | Definition |
|---|---|
| RO | Read-only |
| RW | Read-write |
| RW1C | Read/Write '1' to clear |
| RESERVED | Undefined do not write |

## 4.4 Write Lock Functionality

| WRITE_LOCK | WRITE_LOCK RW1C | SMBus Write Protect |
|---|---|---|
| 0 | 0 | No |
| 0 | 1 | Yes |
| 1 | 0 | Yes |
| 1 | 1 | Yes |

## 4.5 SMBus Address Decode

| Address Selection | | Binary Value | | | | | | | | Hex Value |
|---|---|---|---|---|---|---|---|---|---|---|
| SADR_tri1 | SADR_tri0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Rd/Wrt | |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | D8 |
| | M | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA |
| | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | DE |
| M | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2 |
| | M | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4 |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CA |
| | M | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC |
| | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | CE |

## 4.6 RS2CB19020 SMBus Registers

**Table 32. RS2CB19020 SMBus Registers**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 0 | OUTPUT_ENABLE_2 | RESERVED | [7] | RW | 0 | RESERVED | 0 = output is disabled (low/low)<br>1 = output is enabled |
| | | CLK19_EN | [6] | RW | 1 | Output Enable for CLK19 | |
| | | CLK18_EN | [5] | RW | 1 | Output Enable for CLK18 | |
| | | CLK17_EN | [4] | RW | 1 | Output Enable for CLK17 | |
| | | CLK16_EN | [3] | RW | 1 | Output Enable for CLK16 | |
| | | RESERVED | [2:0] | RW | 0 | RESERVED | |
| 1 | OUTPUT_ENABLE_0 | CLK7_EN | [7] | RW | 1 | Output Enable for CLK7 | 0 = output is disabled (low/low)<br>1 = output is enabled |
| | | CLK6_EN | [6] | RW | 1 | Output Enable for CLK6 | |
| | | CLK5_EN | [5] | RW | 1 | Output Enable for CLK5 | |
| | | CLK4_EN | [4] | RW | 1 | Output Enable for CLK4 | |
| | | CLK3_EN | [3] | RW | 1 | Output Enable for CLK3 | |
| | | CLK2_EN | [2] | RW | 1 | Output Enable for CLK2 | |
| | | CLK1_EN | [1] | RW | 1 | Output Enable for CLK1 | |
| | | CLK0_EN | [0] | RW | 1 | Output Enable for CLK0 | |
| 2 | OUTPUT_ENABLE_1 | CLK15_EN | [7] | RW | 1 | Output Enable for CLK15 | 0 = output is disabled (low/low)<br>1 = output is enabled |
| | | CLK14_EN | [6] | RW | 1 | Output Enable for CLK14 | |
| | | CLK13_EN | [5] | RW | 1 | Output Enable for CLK13 | |
| | | CLK12_EN | [4] | RW | 1 | Output Enable for CLK12 | |
| | | CLK11_EN | [3] | RW | 1 | Output Enable for CLK11 | |
| | | CLK10_EN | [2] | RW | 1 | Output Enable for CLK10 | |
| | | CLK9_EN | [1] | RW | 1 | Output Enable for CLK9 | |
| | | CLK8_EN | [0] | RW | 1 | Output Enable for CLK8 | |
| 3 | OEb_PIN_READBACK | RB_OEb_12 | [7] | RO | 1'bX | Status of OEb12 | 0 = pin low<br>1 = pin high |
| | | RB_OEb_11 | [6] | RO | 1'bX | Status of OEb11 | |
| | | RB_OEb_10 [1] | [5] | RO | 1'bX | Status of OEb10 | |
| | | RB_OEb_9 | [4] | RO | 1'bX | Status of OEb9 | |
| | | RB_OEb_8 | [3] | RO | 1'bX | Status of OEb8 | |
| | | RB_OEb_7 | [2] | RO | 1'bX | Status of OEb7 | |
| | | RB_OEb_6 [1] | [1] | RO | 1'bX | Status of OEb6 | |
| | | RB_OEb_5 [1] | [0] | RO | 1'bX | Status of OEb5 | |
| 4 | SBEN_RDBK_ ACP_CONFIG | RESERVED | [7:5] | RW | 1'b111 | RESERVED | - |
| | | ACP_ENABLE | [4] | RW | 1 | Enable Automatic Clock Parking to low/low when LOS event is detected | 0 = disable ACP<br>1 = enable ACP |
| | | RESERVED | [3:1] | RW | 1'b110 | RESERVED | - |
| | | RB_SBI_ENQ | [0] | RO | 1'bX | Status of SBI_ENQ | 0 = pin low<br>1 = pin |

**Table 32. RS2CB19020 SMBus Registers (Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 5 | VENDOR_REVISION_ID | RID | [7:4] | RO | 0x0 | REVISION ID, A revision is 0000 | - |
| | | VID | [3:0] | RO | 0x1 | VENDOR ID | - |
| 6 | DEVICE_ID | DEVICE_ID | [7:0] | RO | 0xC8 | Device ID | - |
| 7 | BYTE_COUNT | RESERVED | [7:5] | RW | 0x0 | RESERVED | - |
| | | BC | [4:0] | RW | 0x7 | Writing to this register configures how many bytes will be read back in a block read | - |
| 8 | OEb_Configuration_A | CFGA_OEb12 | [7] | RW | 1 | Controls CLK12 | 0 = OEb does not control output<br>1 = OEb controls output |
| | | CFGA_OEb11 | [6] | RW | 1 | Controls CLK11 | |
| | | CFGA_OEb10 | [5] | RW | 1 | Controls CLK10 when SBI_ENQ = 0 | |
| | | CFGA_OEb9 | [4] | RW | 1 | Controls CLK9 | |
| | | CFGA_OEb8 | [3] | RW | 1 | Controls CLK8 | |
| | | CFGA_OEb7 | [2] | RW | 1 | Controls CLK7 | |
| | | CFGA_OEb6 | [1] | RW | 1 | Controls CLK6 when SBI_ENQ = 0 | |
| | | CFGA_OEb5 | [0] | RW | 1 | Controls CLK5 when SBI_ENQ = 0 | |
| 9 | OEb_Configuration_B | CFGB_OEb12 | [7] | RW | 0 | Controls CLK13 | 0 = OEb does not control output<br>1 = OEb controls output |
| | | CFGB_OEb11 | [6] | RW | 0 | Controls CLK14 | |
| | | CFGB_OEb10 | [5] | RW | 0 | Controls CLK15 when SBI_ENQ = 0 | |
| | | CFGB_OEb9 | [4] | RW | 0 | Controls CLK0 | |
| | | CFGB_OEb8 | [3] | RW | 0 | Controls CLK1 | |
| | | CFGB_OEb7 | [2] | RW | 0 | Controls CLK2 | |
| | | CFGB_OEb6 | [1] | RW | 0 | Controls CLK3 when SBI_ENQ = 0 | |
| | | CFGB_OEb5 | [0] | RW | 0 | Controls CLK4 when SBI_ENQ = 0 | |
| 10 | OEb_Configuration_C _ AMP_Control_ | CFGC_OEb12 | [7] | RW | 0 | Controls CLK16 | 0 = OEb does not control output<br>1 = OEb controls output |
| | | CFGC_OEb11 | [6] | RW | 0 | Controls CLK17 | |
| | | CFGC_OEb10 | [5 | RW | 0 | Controls CLK18 when SBI_EN = 0 | |
| | | CFGC_OEb9 | [4] | RW | 0 | Controls CLK19 | |
| | | AMPLITUDE_CTRL | [3:0] | RW | 0x7 | Global Differential output Control<br>0.625V~1V<br>25mV/step<br>Default = 0.8V | - |

**Table 32. RS2CB19020 SMBus Registers (Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 11 | OUTPUT_SLEW _ RATE_0 | CLK7_SLEWRATE | [7] | RW | 1 | CLK7 Slewrate Control | 0 = low slew rate<br>1 = high slew rate |
| | | CLK6_SLEWRATE | [6] | RW | 1 | CLK6 Slewrate Control | |
| | | CLK5_SLEWRATE | [5] | RW | 1 | CLK5 Slewrate Control | |
| | | CLK4_SLEWRATE | [4] | RW | 1 | CLK4 Slewrate Control | |
| | | CLK3_SLEWRATE | [3] | RW | 1 | CLK3 Slewrate Control | |
| | | CLK2_SLEWRATE | [2] | RW | 1 | CLK2 Slewrate Control | |
| | | CLK1_SLEWRATE | [1] | RW | 1 | CLK1 Slewrate Control | |
| | | CLK0_SLEWRATE | [0] | RW | 1 | CLK0 Slewrate Control | |
| 12 | OUTPUT_SLEW _ RATE_1 | CLK15_SLEWRATE | [7] | RW | 1 | CLK15 Slewrate Control | 0 = low slew rate<br>1 = high slew rate |
| | | CLK14_SLEWRATE | [6] | RW | 1 | CLK14 Slewrate Control | |
| | | CLK13_SLEWRATE | [5] | RW | 1 | CLK13 Slewrate Control | |
| | | CLK12_SLEWRATE | [4] | RW | 1 | CLK12 Slewrate Control | |
| | | CLK11_SLEWRATE | [3] | RW | 1 | CLK11 Slewrate Control | |
| | | CLK10_SLEWRATE | [2] | RW | 1 | CLK10 Slewrate Control | |
| | | CLK9_SLEWRATE | [1] | RW | 1 | CLK9 Slewrate Control | |
| | | CLK8_SLEWRATE | [0] | RW | 1 | CLK8 Slewrate Control | |
| 13 | OUTPUT_SLEW _ RATE_2 | RESERVED | [7:4] | RW | 0b1111 | RESERVED | 0 = low slew rate<br>1 = high slew rate |
| | | CLK19_SLEWRATE | [3] | RW | 1 | CLK19 Slewrate Control | |
| | | CLK18_SLEWRATE | [2] | RW | 1 | CLK18 Slewrate Control | |
| | | CLK17_SLEWRATE | [1] | RW | 1 | CLK17 Slewrate Control | |
| | | CLK16_SLEWRATE | [0] | RW | 1 | CLK16 Slewrate Control | |
| 14 - 20 | RESERVED | - | - | - | - | RESERVED | - |

**Table 32. RS2CB19020 SMBus Registers (Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 21 | PD_RESTORE_LOSb | AC_IN | [7] | RW | 0 | Enable receiver bias when CLKIN is AC coupled, | 0 = DC coupled input<br>1 = AC coupled input |
| | | Rx_TERM | [6] | RW | 0 | Enable termination resistors on CLKIN | 0 = input termination R is disabled<br>1 = input termination R is enabled |
| | | RESERVED | [5] | RW | 1'b1 | RESERVED | - |
| | | CLK Acquired | [4] | RO | 1'bX | A clock was acquired | 1 = clock acquired |
| | | PD_RESTOREb | [3] | RW | 1 | Save Configuration in Power Down | 0 = Config Cleared<br>1 = Config Saved |
| | | SDATA_TIMEOUT_EN | [2] | RW | 1 | Enable SMB SDATA time out monitoring | 0 = disable SDATA time out<br>1 = enable SDATA time out |
| | | RESERVED | [1] | RO | 1'bX | - | - |
| | | LOSb_RB | [0] | RO | 1'bX | Real time read back of loss detect block output | 0 = LOS event detected<br>1 = NO LOS event detected. |
| 22 | SBI_MASK_0 [2] | MASK7 | [7] | RW | 0 | Masks off Side-band Disable for CLK7 | 0 = SBI may disable the output<br>1 = SBI cannot disable the output |
| | | MASK6 | [6] | RW | 0 | Masks off Side-band Disable for CLK6 | |
| | | MASK5 | [5] | RW | 0 | Masks off Side-band Disable for CLK5 | |
| | | MASK4 | [4] | RW | 0 | Masks off Side-band Disable for CLK4 | |
| | | MASK3 | [3] | RW | 0 | Masks off Side-band Disable for CLK3 | |
| | | MASK2 | [2] | RW | 0 | Masks off Side-band Disable for CLK2 | |
| | | MASK1 | [1] | RW | 0 | Masks off Side-band Disable for CLK1 | |
| | | MASK0 | [0] | RW | 0 | Masks off Side-band Disable for CLK0 | |

**Table 32. RS2CB19020 SMBus Registers (Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 23 | SBI_MASK_1 [2] | MASK15 | [7] | RW | 0 | Masks off Side-band Disable for CLK15 | 0 = SBI may disable the output<br>1 = SBI cannot disable the output |
| | | MASK14 | [6] | RW | 0 | Masks off Side-band Disable for CLK14 | |
| | | MASK13 | [5] | RW | 0 | Masks off Side-band Disable for CLK13 | |
| | | MASK12 | [4] | RW | 0 | Masks off Side-band Disable for CLK12 | |
| | | MASK11 | [3] | RW | 0 | Masks off Side-band Disable for CLK11 | |
| | | MASK10 | [2] | RW | 0 | Masks off Side-band Disable for CLK10 | |
| | | MASK9 | [1] | RW | 0 | Masks off Side-band Disable for CLK9 | |
| | | MASK8 | [0] | RW | 0 | Masks off Side-band Disable for CLK8 | |
| 24 | SBI_MASK_2 [2] | RESERVED | [7] | RW | 0 | RESERVED | 0 = SBI may disable the output<br>1 = SBI cannot disable the output |
| | | RESERVED | [6] | RW | 0 | RESERVED | |
| | | RESERVED | [5] | RW | 0 | RESERVED | |
| | | RESERVED | [4] | RW | 0 | RESERVED | |
| | | MASK19 | [3] | RW | 0 | Masks off Side-band Disable for CLK19 | |
| | | MASK18 | [2] | RW | 0 | Masks off Side-band Disable for CLK18 | |
| | | MASK17 | [1] | RW | 0 | Masks off Side-band Disable for CLK17 | |
| | | MASK16 | [0] | RW | 0 | Masks off Side-band Disable for CLK16 | |
| 25–32 | RESERVED | RESERVED | [7:0] | RW | 0xXX | RESERVED | - |

**Table 32. RS2CB19020 SMBus Registers (Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 33 | SBI_READBACK_0 [2] | SBI_CLK7 | [7] | RO | 1'bX | Readback of Side-band Disable for CLK7 | 0 = bit low<br>1 = bit high |
| | | SBI_CLK6 | [6] | RO | 1'bX | Readback of Side-band Disable for CLK6 | |
| | | SBI_CLK5 | [5] | RO | 1'bX | Readback of Side-band Disable for CLK5 | |
| | | SBI_CLK4 | [4] | RO | 1'bX | Readback of Side-band Disable for CLK4 | |
| | | SBI_CLK3 | [3] | RO | 1'bX | Readback of Side-band Disable for CLK3 | |
| | | SBI_CLK2 | [2] | RO | 1'bX | Readback of Side-band Disable for CLK2 | |
| | | SBI_CLK1 | [1] | RO | 1'bX | Readback of Side-band Disable for CLK1 | |
| | | SBI_CLK0 | [0] | RO | 1'bX | Readback of Side-band Disable for CLK0 | |
| 34 | SBI_READBACK_1 [2] | SBI_CLK15 | [7] | RO | 1'bX | Readback of Side-band Disable for CLK15 | 0 = bit low<br>1 = bit high |
| | | SBI_CLK14 | [6] | RO | 1'bX | Readback of Side-band Disable for CLK14 | |
| | | SBI_CLK13 | [5] | RO | 1'bX | Readback of Side-band Disable for CLK13 | |
| | | SBI_CLK12 | [4] | RO | 1'bX | Readback of Side-band Disable for CLK12 | |
| | | SBI_CLK11 | [3] | RO | 1'bX | Readback of Side-band Disable for CLK11 | |
| | | SBI_CLK10 | [2] | RO | 1'bX | Readback of Side-band Disable for CLK10 | |
| | | SBI_CLK9 | [1] | RO | 1'bX | Readback of Side-band Disable for CLK9 | |
| | | SBI_CLK8 | [0] | RO | 1'bX | Readback of Side-band Disable for CLK8 | |
| 35 | SBI_READBACK_2 [2] | RESERVED | [7:4] | RO | 1'bXXX | RESERVED | 0 = bit low<br>1 = bit high |
| | | SBI_CLK19 | [3] | RO | 1'bX | Readback of Side-band Disable for CLK19 | |
| | | SBI_CLK18 | [2] | RO | 1'bX | Readback of Side-band Disable for CLK18 | |
| | | SBI_CLK17 | [1] | RO | 1'bX | Readback of Side-band Disable for CLK17 | |
| | | SBI_CLK16 | [0] | RO | 1'bX | Readback of Side-band Disable for CLK16 | |
| 36-37 | RESERVED | RESERVED | [7:0] | RW | 0xXX | RESERVED | RESERVED |

**Table 32. RS2CB19020 SMBus Registers (Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 38 | WRITE_LOCK_NCLEAR | RESERVED | [7:1] | RW | 0x0 | RESERVED | - |
| | | WRITE_LOCK | [0] | RW | 0 | Non-clearable SMBus Write Lock bit. Once written to '1', the SMBus control registers cannot be written to. This bit can only be cleared by cycling power. | 0 = SMBus not locked for writing by this bit. See WRITE_LOCK_ R<br>W1C bit.<br>1 = SMBus locked for writing |
| 39 | WRITE_LOCK_CLEAR _ LOS_EVENT | RESERVED | [7:2] | RW1C | 1'b111000 | - | - |
| | | LOS_EVT | [1] | RW1C | 0 | LOS Event Status<br>When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it. | 0 = No LOS event detected<br>1 = LOS event detected. |
| | | WRITE_LOCK_RW1C | [0] | RW1C | 0 | Clearable SMBus Write Lock bit.<br>When written to one, other SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to it. | 0 = SMBus not locked for writing by this bit. See WRITE_LOCK bit.<br>1 = SMBus locked for writing |

1. Register is only valid when the Side-Band Interface is not enabled (SBI_ENQ = 0).
2. Register only valid when the Side-Band Interface is enabled (SBI_ENQ = 1).

## 4.7 RS2CB19016/13/08/04 SMBus Registers

**Table 33. RS2CB19016/13/08/04 SMBus Registers**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 0 | OUTPUT_ENABLE_0 | [7] | CLK7_EN | RW | 1 | Output Enable Bit for CLK7 | 0 = output is disabled (low/low)<br>1 = output is enabled |
| | | [6] | CLK6_EN | RW | 1 | Output Enable Bit for CLK6 | |
| | | [5] | CLK5_EN | RW | 1 | Output Enable Bit for CLK5 | |
| | | [4] | CLK4_EN | RW | 1 | Output Enable Bit for CLK4 | |
| | | [3] | CLK3_EN | RW | 1 | Output Enable Bit for CLK3 | |
| | | [2] | CLK2_EN | RW | 1 | Output Enable Bit for CLK2 | |
| | | [1] | CLK1_EN | RW | 1 | Output Enable Bit for CLK1 | |
| | | [0] | CLK0_EN | RW | 1 | Output Enable Bit for CLK0 | |

**Table 33. RS2CB19016/13/08/04 SMBus Registers(Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 1 | OUTPUT_ENABLE_1 | [7] | CLK15_EN | RW | 1 | Output Enable Bit for CLK15 | 0 = output is disabled (low/low)<br>1 = output is enabled |
| | | [6] | CLK14_EN | RW | 1 | Output Enable Bit for CLK14 | |
| | | [5] | CLK13_EN | RW | 1 | Output Enable Bit for CLK13 | |
| | | [4] | CLK12_EN | RW | 1 | Output Enable Bit for CLK12 | |
| | | [3] | CLK11_EN | RW | 1 | Output Enable Bit for CLK11 | |
| | | [2] | CLK10_EN | RW | 1 | Output Enable Bit for CLK10 | |
| | | [1] | CLK9_EN | RW | 1 | Output Enable Bit for CLK9 | |
| | | [0] | CLK8_EN | RW | 1 | Output Enable Bit for CLK8 | |
| 2 | OEb_PIN_READBACK_0 | [7] | OE7b_Readback | RO | pin | Status of OE7b pin | 0 = OEb pin low<br>1 = OEb Pin high |
| | | [6] | OE6b_Readback | RO | pin | Status of OE6b pin | |
| | | [5] | OE5b_Readback | RO | pin | Status of OE5b pin | |
| | | [4] | OE4b_Readback | RO | pin | Status of OE4b pin | |
| | | [3] | OE3b_Readback | RO | pin | Status of OE3b pin | |
| | | [2] | OE2b_Readback | RO | pin | Status of OE2b pin | |
| | | [1] | OE1b_Readback | RO | pin | Status of OE1b pin | |
| | | [0] | OE0b_Readback | RO | pin | Status of OE0b pin | |
| 3 | OEb_PIN_READBACK_1 | [7] | OE15b_Readback | RO | pin | Status of OE15b pin | 0 = OEb pin low<br>1 = OEb Pin high |
| | | [6] | OE14b_Readback | RO | pin | Status of OE14b pin | |
| | | [5] | OE13b_Readback | RO | pin | Status of OE13b pin | |
| | | [4] | OE12b_Readback | RO | pin | Status of OE12b pin | |
| | | [3] | OE11b_Readback | RO | pin | Status of OE11b pin | |
| | | [2] | OE10b_Readback | RO | pin | Status of OE10b pin | |
| | | [1] | OE9b_Readback | RO | pin | Status of OE9b pin | |
| | | [0] | OE8b_Readback | RO | pin | Status of OE8b pin | |
| 4 | SBEN_RDBK_ LOS_CONFIG | [7:5] | RESERVED | - | - | - | - |
| | | [4] | LOSb_ACP_ENABLE | RW | 1 | Enable input loss detect to park outputs low/low | 0 = disable,<br>1 = enable |
| | | [3:2] | RESERVED | - | - | - | - |
| | | [1] | RESERVED | - | - | - | - |
| | | [0] | RB_SBI_EN | RO | pin | Status of SBI_EN | 0 = pin low<br>1 = pin high |
| 5 | VENDOR_REVISION_ ID | [7:4] | RID | RO | 0x0 | REVISION ID, A rev is 0000 | - |
| | | [3:0] | VID | RO | 0x1 | VENDOR ID | - |

**Table 33. RS2CB19016/13/08/04 SMBus Registers(Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 6 | DEVICE_ID | [7:0] | DEVICE_ID | RO | | Device ID:<br>RS2CB19016 = 0h10<br>RS2CB19013 = 0h0D<br>RS2CB19008 = 0h08<br>RS2CB19004 = 0h04<br>RS2CB19016-100 = 0h90<br>RS2CB19013-100 = 0h8D<br>RS2CB19008-100 = 0h88<br>RS2CB19004-100 = 0h84 | - |
| 7 | BYTE_COUNT | [7:5] | RESERVED | - | - | - | - |
| | | [4:0] | BC | RW | 0x7 | Writing to this register configures how many bytes will be read back in a block read. | - |
| 8 | SBI_MASK_0<br>(Register only functional and/or valid when SBEN = 1) | [7] | MASK7 | RW | 0 | Masks off Side-band Disable for CLK7 | 0 = SBI may disable the output<br>1 = SBI cannot disable the output |
| | | [6] | MASK6 | RW | 0 | Masks off Side-band Disable for CLK6 | |
| | | [5] | MASK5 | RW | 0 | Masks off Side-band Disable for CLK5 | |
| | | [4] | MASK4 | RW | 0 | Masks off Side-band Disable for CLK4 | |
| | | [3] | MASK3 | RW | 0 | Masks off Side-band Disable for CLK3 | |
| | | [2] | MASK2 | RW | 0 | Masks off Side-band Disable for CLK2 | |
| | | [1] | MASK1 | RW | 0 | Masks off Side-band Disable for CLK1 | |
| | | [0] | MASK0 | RW | 0 | Masks off Side-band Disable for CLK0 | |
| 9 | SBI_MASK_1<br>(Register only functional and/or valid when SBEN = 1) | [7] | MASK15 | RW | 0 | Masks off Side-band Disable for CLK15 | 0 = SBI may disable the output<br>1 = SBI cannot disable the output |
| | | [6] | MASK14 | RW | 0 | Masks off Side-band Disable for CLK14 | |
| | | [5] | MASK13 | RW | 0 | Masks off Side-band Disable for CLK13 | |
| | | [4] | MASK12 | RW | 0 | Masks off Side-band Disable for CLK12 | |
| | | [3] | MASK11 | RW | 0 | Masks off Side-band Disable for CLK11 | |
| | | [2] | MASK10 | RW | 0 | Masks off Side-band Disable for CLK10 | |
| | | [1] | MASK9 | RW | 0 | Masks off Side-band Disable for CLK9 | |
| | | [0] | MASK8 | RW | 0 | Masks off Side-band Disable for CLK8 | |
| 10 | RESERVED | [7:0] | Reserved | - | - | - | - |

**Table 33. RS2CB19016/13/08/04 SMBus Registers(Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 11 | SBI_READBACK_0 (Register only functional and/or valid when SBEN = 1) | [7] | SBI_CLK7 | RO | X | Readback of Side-band Disable for CLK7 | 0 = bit low<br>1 = bit high |
| | | [6] | SBI_CLK6 | RO | X | Readback of Side-band Disable for CLK6 | |
| | | [5] | SBI_CLK5 | RO | X | Readback of Side-band Disable for CLK5 | |
| | | [4] | SBI_CLK4 | RO | X | Readback of Side-band Disable for CLK4 | |
| | | [3] | SBI_CLK3 | RO | X | Readback of Side-band Disable for CLK3 | |
| | | [2] | SBI_CLK2 | RO | X | Readback of Side-band Disable for CLK2 | |
| | | [1] | SBI_CLK1 | RO | X | Readback of Side-band Disable for CLK1 | |
| | | [0] | SBI_CLK0 | RO | X | Readback of Side-band Disable for CLK0 | |
| 12 | SBI_READBACK_1 (Register only functional and/or valid when SBEN = 1) | [7] | SBI_CLK15 | RO | X | Readback of Side-band Disable for CLK15 | 0 = bit low<br>1 = bit high |
| | | [6] | SBI_CLK14 | RO | X | Readback of Side-band Disable for CLK14 | |
| | | [5] | SBI_CLK13 | RO | X | Readback of Side-band Disable for CLK13 | |
| | | [4] | SBI_CLK12 | RO | X | Readback of Side-band Disable for CLK12 | |
| | | [3] | SBI_CLK11 | RO | X | Readback of Side-band Disable for CLK11 | |
| | | [2] | SBI_CLK10 | RO | X | Readback of Side-band Disable for CLK10 | |
| | | [1] | SBI_CLK9 | RO | X | Readback of Side-band Disable for CLK9 | |
| | | [0] | SBI_CLK8 | RO | X | Readback of Side-band Disable for CLK8 | |
| 13–16 | RESERVED | [7:0] | Reserved | - | - | - | - |
| 17 | LPHCSL_AMP_CTRL | [7:4] | Global Amplitude Control | RW | 0x7 | 0.625V~1V in 25mV steps. | Default = 0.8V |
| | | [3:0] | Reserved | - | - | - | - |

**Table 33. RS2CB19016/13/08/04 SMBus Registers(Cont.)**

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 18 | PD_RESTORE_LOSb _ ENABLE | [7] | AC_IN | RW | 0 | Enable receiver self bias when input clock is AC coupled, | 0 = DC coupled input<br>1 = AC coupled input |
| | | [6] | Rx_TERM | RW | 0 | Enable termination resistor on CLKIN/CLKINb | 0 = input termination is disabled<br>1 =input termination is enabled |
| | | [5:4] | Reserved | - | - | - | - |
| | | [3] | PD_RESTOREb | RW | 1 | Save Configuration in Power Down | 0 = Config Cleared<br>1 = Config Saved |
| | | [2:1] | Reserved | - | - | - | - |
| | | [0] | LOSb_Readback | RO | X | real time read back of loss detect block output | 0 = LOS event detected<br>1 = NO LOS event detected. |
| 19 | RESERVED | [7:0] | Reserved | - | - | - | - |
| 20 | OUTPUT_SLEW_ RATE_0 | [7] | CLK7_SLEWRATE | RW | 1 | CLK7 Slew Rate Control | 0 = low slew rate<br>1 = high slew rate |
| | | [6] | CLK6_SLEWRATE | RW | 1 | CLK6 Slew Rate Control | |
| | | [5] | CLK5_SLEWRATE | RW | 1 | CLK5 Slew Rate Control | |
| | | [4] | CLK4_SLEWRATE | RW | 1 | CLK4 Slew Rate Control | |
| | | [3] | CLK3_SLEWRATE | RW | 1 | CLK3 Slew Rate Control | |
| | | [2] | CLK2_SLEWRATE | RW | 1 | CLK2 Slew Rate Control | |
| | | [1] | CLK1_SLEWRATE | RW | 1 | CLK1 Slew Rate Control | |
| | | [0] | CLK0_SLEWRATE | RW | 1 | CLK0 Slew Rate Control | |
| 21 | OUTPUT_SLEW_ RATE_1 | [7] | CLK15_SLEWRATE | RW | 1 | CLK15 Slewrate Control | 0 = low slew rate<br>1 = high slew rate |
| | | [6] | CLK14_SLEWRATE | RW | 1 | CLK14 Slewrate Control | |
| | | [5] | CLK13_SLEWRATE | RW | 1 | CLK13 Slewrate Control | |
| | | [4] | CLK12_SLEWRATE | RW | 1 | CLK12 Slewrate Control | |
| | | [3] | CLK11_SLEWRATE | RW | 1 | CLK11 Slewrate Control | |
| | | [2] | CLK10_SLEWRATE | RW | 1 | CLK10 Slewrate Control | |
| | | [1] | CLK9_SLEWRATE | RW | 1 | CLK9 Slewrate Control | |
| | | [0] | CLK8_SLEWRATE | RW | 1 | CLK8 Slewrate Control | |
| 23–37 | Reserved | [7:0] | Reserved | - | - | - | - |
| | | [7:1] | Reserved | RW | 0 | reserved | - |

| Byte | Register | Name | Bit | Type | Default | Description | Definition |
|---|---|---|---|---|---|---|---|
| 38 | WRITE_LOCK _ NOCLEAR | [0] | WRITE_LOCK | RW | 0 | Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by cycling power. | 0 = SMBus not locked for writing by this bit. See WRITE_LOCK _RW1C bit.<br>1 = SMBus locked for writing |
| 39 | WRITE_LOCK_ CLEAR_LOS_EVEN T | [7:2] | Reserved | - | - | - | - |
| | | [1] | LOS_EVT | R/ W 1C | 0 | LOS Event Status<br>When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it. | 0 = No LOS event detected<br>1 = LOS event detected. |
| | | [0] | WRITE_LOCK_RW1C | R/ W 1C | 0 | Clearable SMBus Write Lock bit.<br>When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to it. | 0 = SMBus not locked for writing by this bit. See WRITE_LOCK bit.<br>1 = SMBus locked for writing |

# 5. Applications Information

## 5.1 Inputs, Outputs, and Output Control

### 5.1.1 Recommendations for Unused Inputs and Outputs

#### 5.1.1.1 Unused Differential CLKIN Inputs

The CLKIN/CLKINb inputs of the RS2CB19016/13/08/04 devices have internal bias networks that protect the devices from a floating input clock condition. For RS2CB19020 multiplexers that use only one input clock, the unused input can be left open. It is recommended that no trace be attached to unused CLKIN pins.

#### 5.1.1.2 Unused Single-ended Control Inputs

The single-ended control pins have internal pull-up and/or internal pull-down resistors and do not require external resistors. They can be left floating if the default pin state is the desired state. If external resistors are needed to change the pin state or are desired for design robustness, 10kohm is the recommended value.

#### 5.1.1.3 Unused Differential CLK Outputs

All unused CLK outputs can be left floating. RSM recommends that no trace be attached to unused CLK outputs. While not required (but is highly recommended), the best design practice is to disable unused CLK outputs.

#### 5.1.1.4 Unused SMBus Clock and Data Pins

If the SMBus interface is not used, the clock and data pins must be pulled high with an external resistor. The two pins can share a resistor if there is no possibility of using the SMBus interface for debug purposes. If the interface may be used for debug, separate resistors should be used. 10kohm is the recommended value.

### 5.1.2 Differential CLKIN Configurations

The RS2CB19xxx clock input supports four configurations:

- Direct connection to HCSL-level inputs
- Direct connection to LVDS-level inputs with *external* termination resistor
- Internal self-bias circuit for applications that *externally* AC-couple the input clock
  - This feature is enabled by the **AC_IN** bit.
- Internal pull-down resistors (Rp) to terminate the clock input at the receiver.
  - This feature is enabled by the **Rx_TERM** bit.

Devices with multiple input clocks have individual AC_IN and Rx_TERM configuration bits for each input. The internal input clock terminations prevent reflections and are useful for non-PCIe applications, where the frequency and transmission line length vary from the 100MHz PCIe standard.

Figure 12 through Figure 15 illustrate the above items.

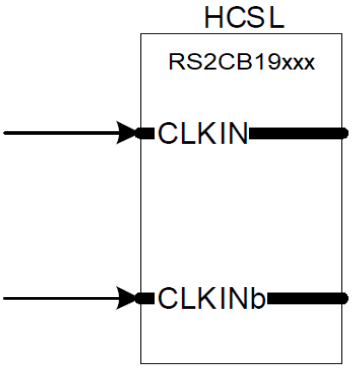



Figure 12. HCSL Input Levels (PCI-e Standard)

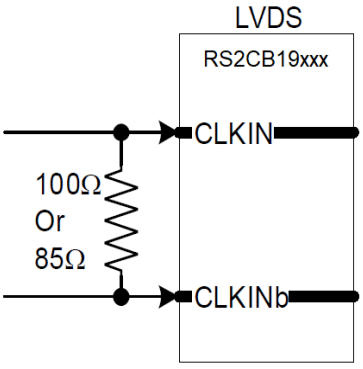



Figure 13. LVDS Input Levels

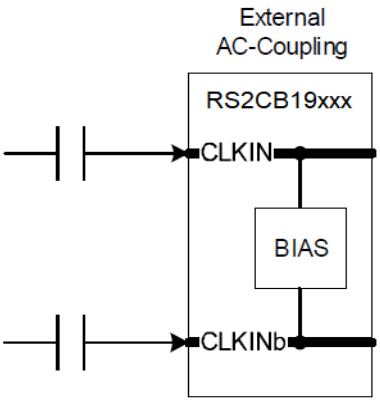



Figure 14. External AC-Coupling

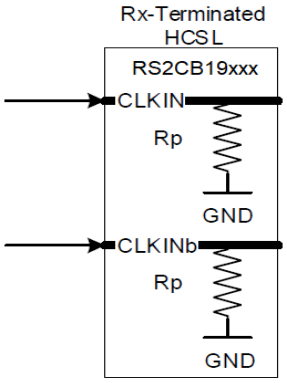



Figure 15. Receiver Termination

## 5.1.3 Differential CLK Output Configurations

### 5.1.3.1 Direct-Coupled HCSL Loads

The RS2CB19xxx LP-HCSL clock outputs have internal source terminations and directly drive industry-standard HCSL-level inputs with no external components. They support both 85ohm and 100ohm differential impedances. The clock outputs can also drive receiver-terminated HCSL loads. The combination of source termination and receiver termination results in a double-terminated load. When double-terminated, the clock output swing will be half of the source-terminated values.

### 5.1.3.2 AC-Coupled non-HCSL Loads

The RS2CB19xxx clock output can directly drive AC-coupling capacitors without any termination components. The clock input side of the AC-coupling capacitor may require an input-dependent bias network (BN). For examples of terminating the RS2CB19xxx clock outputs to other logic families such as LVDS, LVPECL, or CML.

Figure 16 to Figure 18 show the various clock output configurations.

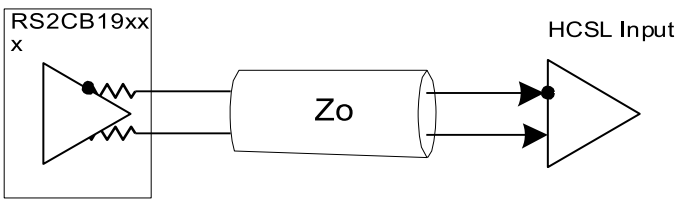



Figure 16. Direct-Coupled Source-Terminated HCSL

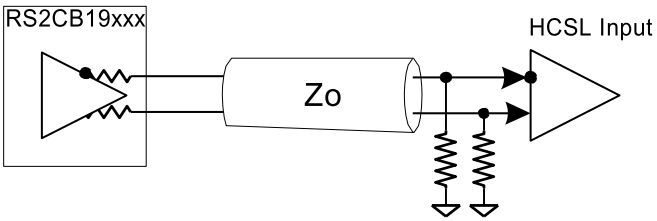



**Figure 17. Direct-Coupled Double-Terminated HCSL**

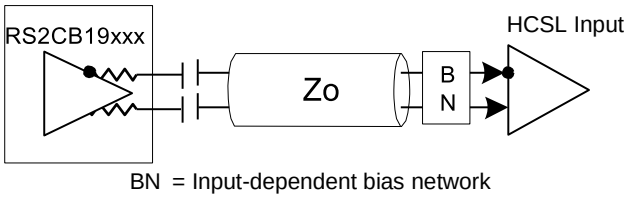



**Figure 18. AC-Coupled**

## 5.2 Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the RS2CB19xxx may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the RS2CB19xxx before it has received power.

## 5.3 Flexible Startup Sequence

RS2CB19xxx support Flexible Startup Sequencing (FSS). FSS allows application of CLKIN at different times in the system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table 34 shows the supported sequences; that is, the RS2CB19xxx can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

**Table 34. Flexible Startup Sequences**

| VDD | PWRGD_PWRDN | CLKIN/CLKINb |
|---|---|---|
| Not present | X | Running |
| | | Floating |
| | | Low/Low |
| Present | 0 or 1 | Running |
| | | Floating |
| | | Low/Low |

## 5.4 Loss of Signal and Automatic Clock Parking

The RS2CB190xx buffers and multiplexers have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOSb pin (the “b” suffix indicates “bar”, or active-low) and sets the LOS_EVT bit in the SMBus register space. There are two slightly different LOSb pin behaviors at power up. Figure 19 shows the LOSb de-assertion timing for the 8, 13, 16 and 20-output buffers. CLKIN is represented differentially in Figure 19 and Figure 20.

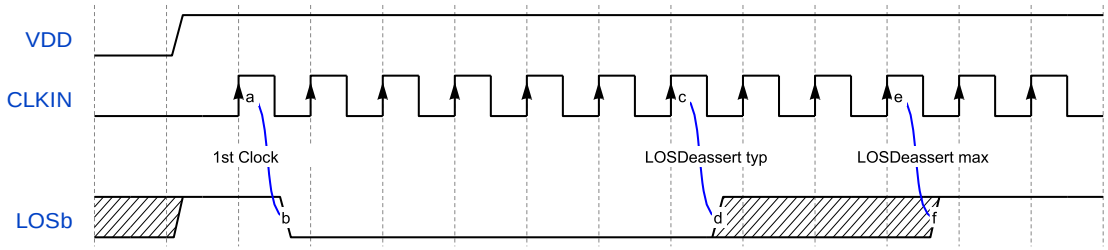



**Figure 19. LOSb De-assert Timing, RS2CB19008, RS2CB19013, RS2CB19016**

*Note*: The LOS circuit on the RS2CB19016/13/08/04 output buffers requires a CLKIN edge to release the LOSb pin after power up. So, the LOSb pin will be high until the first clock edge after power up.

Figure 20 shows the LOSb de-assertion timing for RS2CB19020.

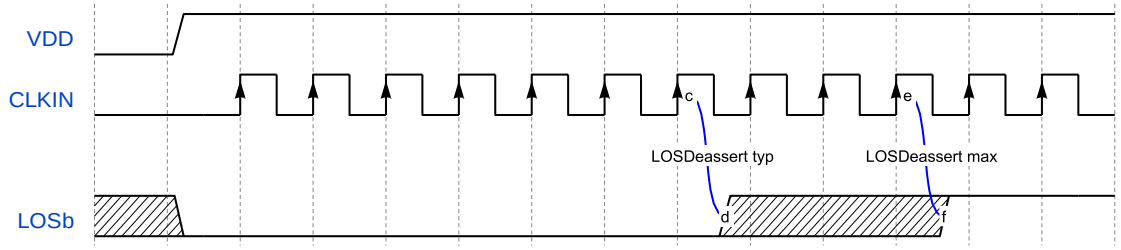



**Figure 20. LOSb De-assert Timing RS2CB19020 Devices**

*Note:* The LOSb pin monitors the *selected input clock* in the RS2CB19020 multiplexers.

The following diagram shows the LOSb assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event. For exact timing, see Electrical Characteristics.

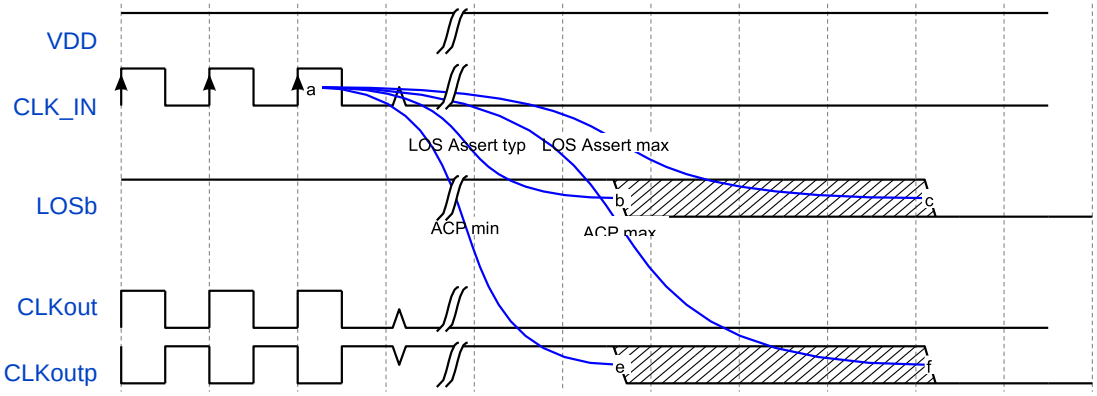



**Figure 21. LOSb Assert Timing**

## 5.5 Output Enable Control

The RS2CB19xxx buffer family provides three mechanisms to enable or disable clock outputs. All three mechanisms start and stop the output clocks in a synchronous, glitch-free manner. A clock output is enabled only when all three mechanisms indicate “enabled.” The following sections describe the three mechanisms.

### 5.5.1 SMBus Output Enable Bits

The RS2CB19xxx family has a traditional SMBus output enable bit for each output. The power-up default is 1, or enabled. Changing this bit to a 0 disables the output to a low/low state. The transitions between the enable and disable states are glitch-free in both directions.

*Note*: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

### 5.5.2 Output Enable (OEb) Pins

The OEb (Note: the “b” suffix indicates “bar”, or active-low) pins on the RS2CB19xxx family provide flexible CLKREQb functionality for PCIe slots and/or banked OE control for ‘motherboard-down’ devices (depending on the device). If the OEb pin is low the controlled output is enabled. If the OEb pin is high, the controlled output is disabled to a low/low state. All OEb pins enable and disable the controlled outputs in a glitch-free, synchronous manner.

*Note*: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

The RS2CB19020 each have 8 OEb pins. Some of the pins are muxed with SBI functions.

The RS2CB19020 OEb pins may be configured to control up to 2 outputs. Details are provided in Table 35.

**Table 35. RS2CB19020 OEb Mapping[1]**

| Pin Name | SBI_ENQ Pin | Default Pin Function | Optional Pin Function |
|---|---|---|---|
| OEb12 | X | CLK12 OEb | CLK13 OEb |
| OEb11 | X | CLK11 OEb | CLK14 OEb |
| OEb10_SHFT_LDb | 0 (Disabled) | CLK10 OEb | CLK15 OEb |
| | 1 (Enabled) | SHFT_LDb | N/A |
| OEb9 | X | CLK9 OEb | CLK0 OEb |
| OEb8 | X | CLK8 OEb | CLK1 OEb |
| OEb7 | X | CLK7 OEb | CLK2 OEb |
| OEb6_SBI_CLK | 0 (Disabled) | CLK6 OEb | CLK3 OEb |
| | 1 (Enabled) | SBI_CLK | N/A |
| OEb5_SBI_IN | 0 (Disabled) | CLK5 OEb | CLK4 OEb |
| | 1 (Enabled) | SBI_IN | N/A |

1. See the OEb_ASSIGNMENT registers in Table 32.

The RS2CB19016/13/08/04 devices (16, 13, 8 and 4 outputs respectively) provide a dedicated OEb pin for each output, and therefore do not have OEb_ASSIGNMENT registers. Note that four OEb pins are used for the SBI interface when SBI_ENQ = 1 (for more information, see Table 35).

**Table 36. RS2CB19016, RS2CB19013, RS2CB19008,RS2CB19004 Buffer OEb Mapping**

| Pin Name | SBI_ENQ Pin | RS2CB19016 Pin Function | RS2CB19013 Pin Function | RS2CB19008 Pin Function | RS2CB19004 Pin Function |
|---|---|---|---|---|---|
| OEb0 | X | CLK0 OEb | CLK0 OEb | - | - |
| OEb1 | X | CLK1 OEb | CLK1 OEb | CLK1 OEb | - |
| OEb2_SBI_OUT | 0 (Disabled) | CLK2 OEb | CLK2 OEb | CLK2 OEb | CLK2 OEb |
| | 1 (Enabled) | SBI_OUT | SBI_OUT | SBI_OUT | SBI_OUT |
| OEb3 | X | CLK3 OEb | CLK3 OEb | CLK3 OEb | - |
| OEb4 | X | CLK4 OEb | - | - | - |
| OEb5_SBI_CLK | 0 (Disabled) | CLK5 OEb | - | CLK5 OEb | CLK5 OEb |
| | 1 (Enabled) | SBI_CLK | - | SBI_CLK | SBI_CLK |
| OEb6 | X | CLK6 OEb | - | CLK6 OEb | - |
| OEb6_SBI_CLK | 0 (Disabled) | - | CLK6 OEb | - | - |
| | 1 (Enabled) | - | SBI_CLK | - | - |
| OEb7 | X | CLK7 OEb | CLK7 OEb | CLK7 OEb | - |
| OEb8 | X | CLK8 OEb | CLK8 OEb | - | - |
| OEb9_SBI_IN | 0 (Disabled) | CLK9 OEb | CLK9 OEb | - | CLK9 OEb |
| | 1 (Enabled) | SBI_IN | SBI_IN | - | SBI_IN |
| OEb10 | X | CLK10 OEb | CLK10 OEb | - | - |
| OEb10_SBI_IN | 0 (Disabled) | - | - | CLK10 OEb | - |
| | 1 (Enabled) | - | - | SBI_IN | - |
| OEb11 | X | CLK11 OEb | CLK11 OEb | - | - |
| OEb12 | X | CLK12 OEb | CLK12 OEb | - | - |
| OEb13_SHFT_LDb | 0 (Disabled) | CLK13 OEb | CLK13 OEb | CLK13 OEb | CLK13 OEb |
| | 1 (Enabled) | SHFT_LDb | SHFT_LDb | SHFT_LDb | SHFT_LDb |
| OEb14 | X | CLK14 OEb | CLK14 OEb | - | - |
| OEb15 | X | CLK15 OEb | - | - | - |

### 5.5.3 Side-Band Interface (SBI)

SMBus output enable bits and OEb pins are the traditional methods for enabling and disabling clocks. The 2-wire SMBus interface can enable or disable all clock outputs in a device. This pin efficiency is its advantage. The SMBus interface's main drawback is that it is a relatively slow physical interface, whose software is one of several routines running on an often overtaxed micro-controller. OEb pins are real-time and are ideally dedicated to an individual clock output. As buffers grow in output count, dedicated OEb pins become problematic for two reasons. First, the clock buffer pin count becomes much larger than it otherwise would be, resulting in a larger package. Second, unless the OEb pins are used for CLKREQ# functionality, the number of pins that need to be controlled outgrows the GPIO pins of an FPGA or micro-controller.

A third output enable/disable mechanism, the Side-Band Interface (SBI), addresses these issues. The SBI is a simple 3-wire (4-wire if the SBI_OUT pin is used) interface that can control all outputs across multiple devices. The SBI is only slightly less pin efficient than the SMBus, and is much more pin efficient than a dedicated OEb pins per output. It is protocol-free, hardware-oriented and runs at speeds up to 25MHz, much faster than SMBus.

Another SBI advantage is that it is active after power is applied and before PWRGD is asserted. External logic can disable specific outputs before PWRGD is asserted, and can then dynamically adjust the output run state during device operation. The SBI can make the adjustments much more rapidly than SMBus.

The RS2CB19xxx 4-wire SBI interface consists of the SBI_IN, SBI_CLK, SHFT_LDb, and SBI_OUT pins. The RS2CB19xxx SBI is enabled by strapping the SBI_ENQ pin to 1. When enabled, various OEb pins become the SBI interface. The exact pins that are multiplexed vary with device (for more information, see Table 36).

The SBI_ENQ pin strap takes effect as soon as power is applied and is not dependent on the assertion of PWRGD_PWRDNb to 1. Because of this, the SBI_ENQ must be static and cannot change once power is applied. If SBI_ENQ is 0 when power is applied, the SBI is disabled and has no impact on enabling or disabling outputs.

The SBI consists of a shift register, an SMBus readback register (of the shift register contents), and an SMBus MASK register. The SBI shifts a bit stream containing the enable/disable pattern into the shift register. A 1 enables an output and a 0 disables an output. All shift-register bits default to 1 at power up, indicating an enabled state. This means that the SBI can be used to disable outputs at power up because the default is enabled.

The SBI has its own SBI_CLK and does not need a running CLKIN to shift in an enable/disable pattern. This provides utmost flexibility for setting output run state before the SMBus becomes active or before the CLKIN is applied. When the SBI indicates enabled, the standard SMBus output enable bits and OEb pins can control the outputs.

The SBI feeds common output enable/disable synchronization logic ensuring glitch-free enable and disable of outputs. Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

If the application does not use the SBI, the SBI_ENQ pin can be tied to 0, and the entire SBI has no impact on enabling or disabling clock outputs.

The SBI Mask registers allow the user to block the disable function of the SBI via the SMBus. The SBI Mask registers default to 0 at power-up, allowing the SBI shift register bits to disable their respective output. After asserting the PWRGD_PWRDNb pin high, the SMBus is active and the SBI mask registers can be configured via SMBus to mask off (block) the SBI disable function. In other words, setting and SBI Mask bit to 1 forces the SBI to always indicate "enable" for the respective output. This allows the user to prevent the SBI from accidentally turning off a critical output.

The RS2CB190xx clock buffers provide the ability to read back the SBI shift register contents via the SMBus. The SMBus readback values update on each falling edge of SHFT_LDb. Note: The SBI shift register can only be read using the SMBus; the SMBus *cannot* be used to load it.

#### 5.5.4.1 Using the SBI

Using the RS2CB19020 as an example, we see the SBI shift order follows the order of the SMBus enable bits. in Byte [2:0] as shown in Figure 22. The first bit shifted in would be the output enable/disable bit for the CLK19, which is in Byte 0 bit 6. The last bit shifted in would be the output enable/disable for CLK0, which is in Byte 1, bit 0.

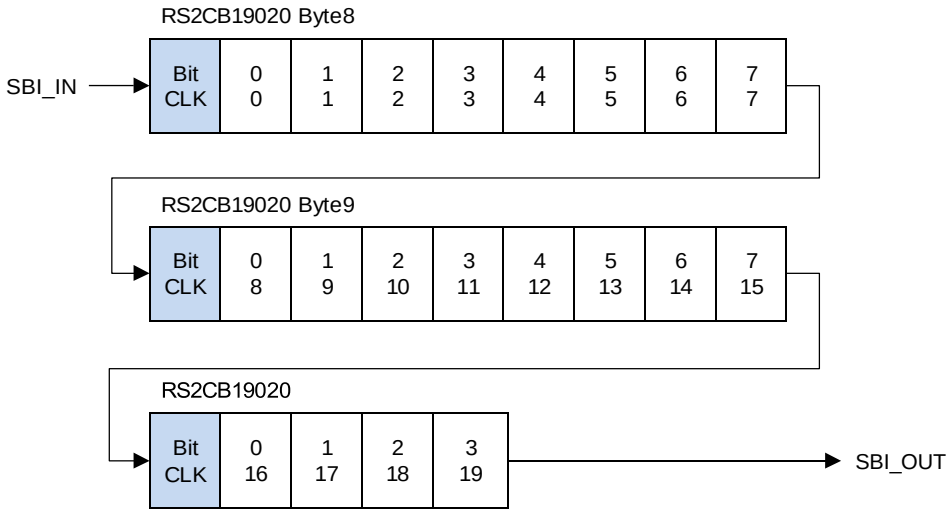



**Figure 22. RS2CB19020 Side-Band Shift Order**

Figure 23 through Figure 25 show the Side-Band Shift order for the RS2CB19016, RS2CB19013, RS2CB19008. Notice that the Side-Band Shift Count is equal to the number of outputs in each device.

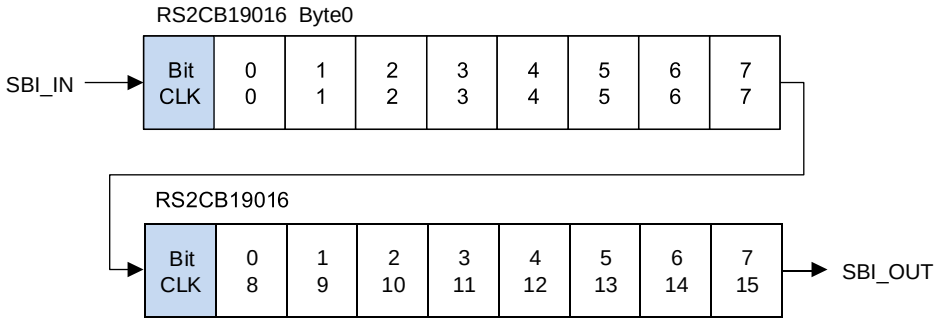



**Figure 23. RS2CB19016 Side-Band Shift Order**

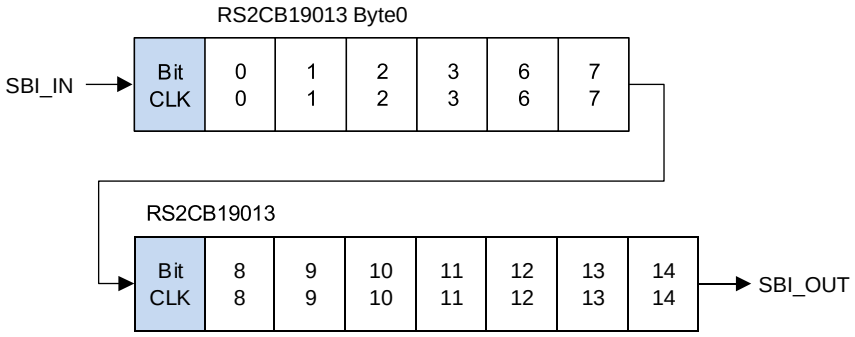



**Figure 24. RS2CB19013 Side-Band Shift Order**

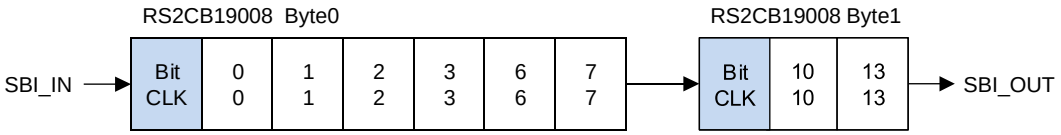



**Figure 25. RS2CB19008 Side-Band Shift Order**

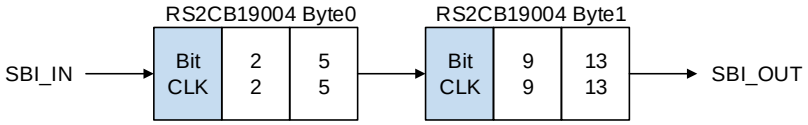



**Figure 26. RS2CB19004 Side-Band Shift Order**

### 5.5.4.2 Side-Band Interface Timing

Figure 26 shows the basic timing of the side-band interface. The SHFT_LDb pin goes high to enable the SBI_CLK input. Next, the rising edge of SBI_CLK clocks SBI_IN data into the shift register. After the 24th clock (assuming the RS2CB19020), stop the SBI_CLK low and drive the SHFT_LDB pin low. The falling edge of SHFT_LDb latches the shift register contents to the output control register, disabling or enabling the outputs. Always shift the complete set of bits into the shift register to control the outputs. For the Side-Band Interface AC/DC Electrical Characteristics, see Table 28.

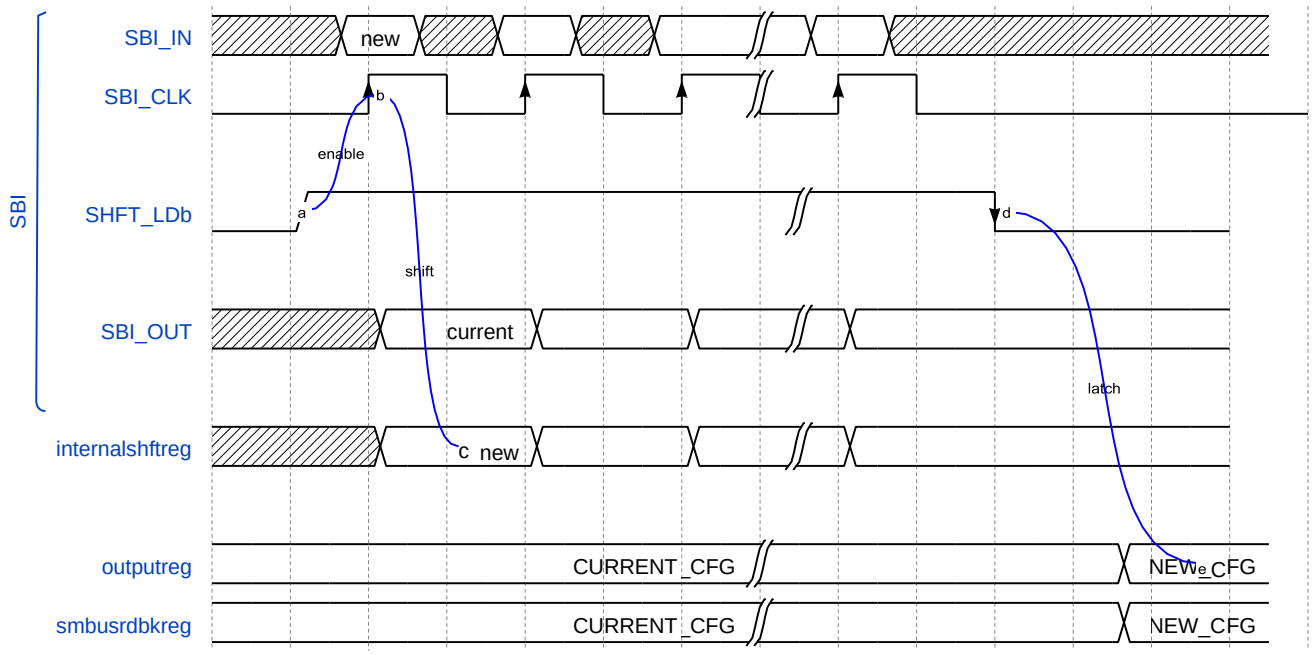



**Figure 26. Side-Band Interface Functional Timing**

#### 5.5.4.3 Side-Band Interface Connection Topologies

The RS2CB19xxx support two SBI connection topologies: Star and Daisy-chain.

In a Star topology, multiple devices can share the SBI_CLK and SBI_IN pins. In this topology, each RS2CB190xx has a dedicated **SHFT_LDb** pin.

In a Daisy-chain topology, the SBI_OUT of one device connects to the SBI_IN of a downstream device. When using the daisy-chain topology, the user must shift a complete set of bits for the combined devices. Two daisy-chained RS2CB19020 require shifting 2 × 20 = 40 bits. An RS2CB19016 followed by an RS2CB19008 would require shifting 8 + 16 = 24 bits. When the SHFT_LDb pin is low, the SBI interface ignores any activity on the SBI_CLK and SBI_IN pins.

Figure 27 shows a star topology connection for the RS2CB19xxx SBI interface. The star topology allows independent configuration of each device. For the RS2CB19020, this means shifting 20 bits at a time. A disadvantage is that a separate SHFT_LDb pin is required for each device. The star topology allows additional devices to be controlled at the cost of an additional GPIO per device.

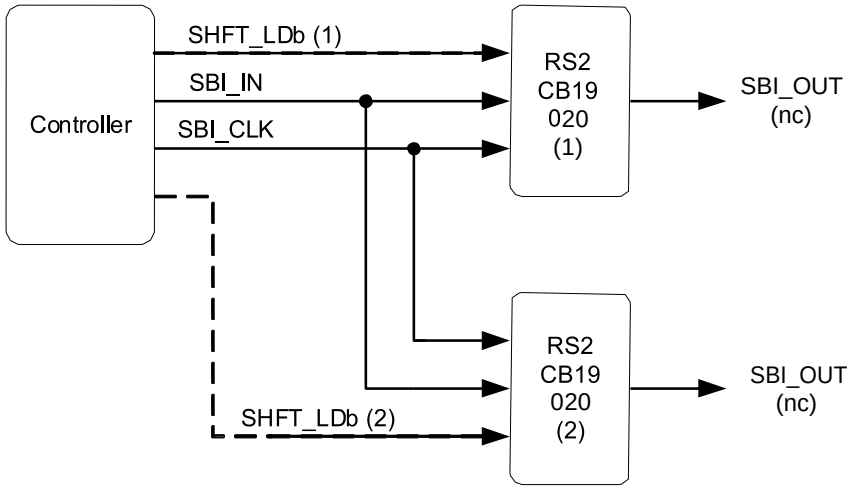



**Figure 27. Side-Band Interface Star Topology**

The Daisy-chain topology allows configuration of any number of devices with only three signals from the SBI controller. It uses the SBI_OUT pin of one device to drive the SBI_IN pin of the next device in the daisy chain. Users must take care to shift the proper number of bits in this configuration. For the example shown in Figure 28, the SBI bit stream consists of 32 bits.

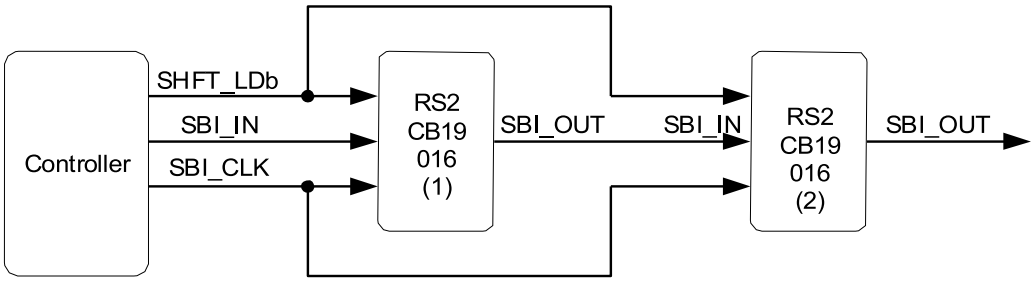



**Figure 28. Side-Band Interface Daisy-Chain Topology**

### 5.5.5 Output Enable/Disable Priority

The RS2CB19xxx output enable/disable priority is an “AND” function of all enable methods. This means that the SMBus output enable bit AND the OEb pin (if present/assigned) AND the SBI must indicate that the output is enabled in order for the output to be enabled. A logical representation of the priority logic is shown in Figure 29.

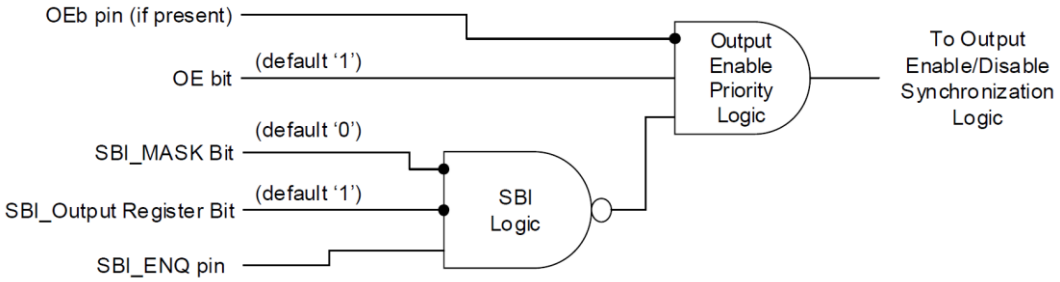
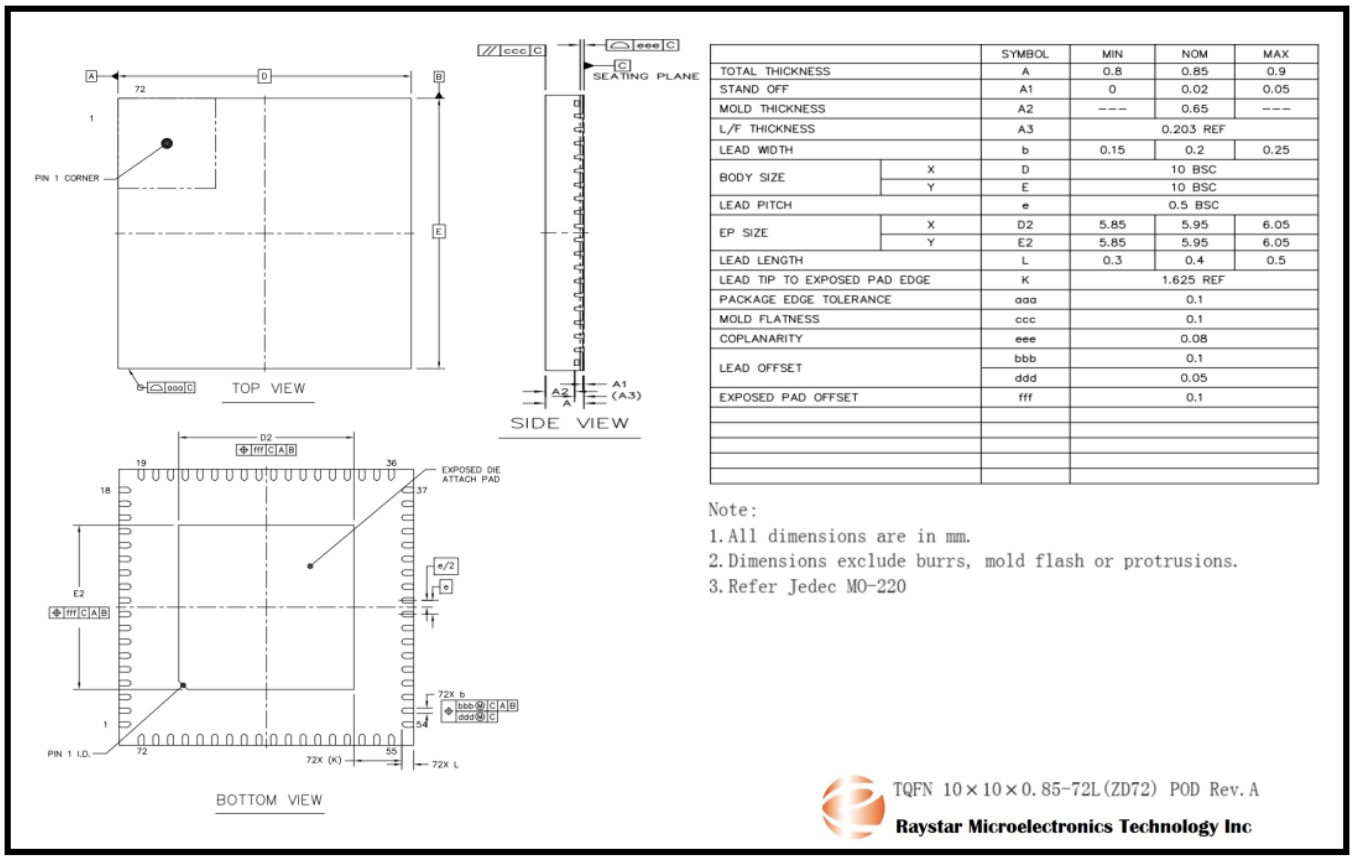



**Figure 29. Output Enable/Disable Priority (Logical)**

# 6. Package Information

The package outline drawings are located at the end of this document and are accessible from the website. The package information is the most current data available and is subject to change without revision of this document.

**TQFN 10x10X0.85-72L**

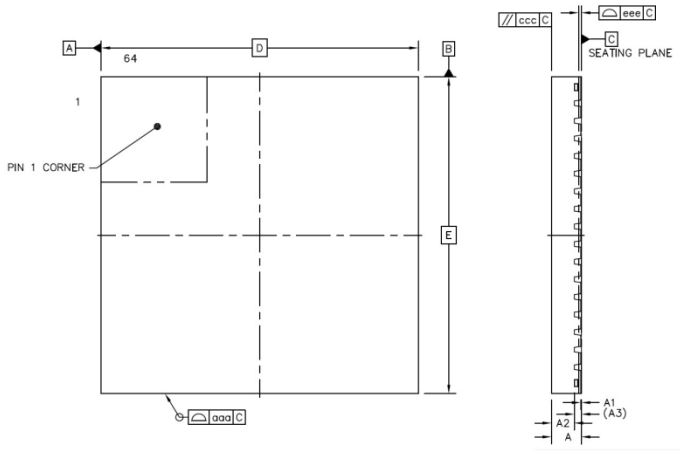



| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | | 10 BSC | |
| | Y | E | | 10 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | D2 | 5.85 | 5.95 | 6.05 |
| | Y | E2 | 5.85 | 5.95 | 6.05 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 1.625 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

Note:
1. All dimensions are in mm.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MO-220

TQFN 10×10×0.85-72L(ZD72) POD Rev.A
Raystar Microelectronics Technology Inc

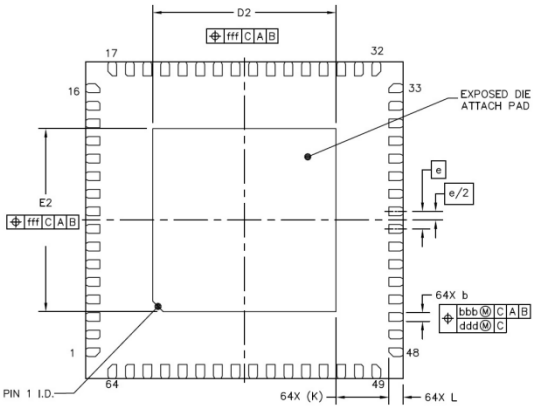
## TQFN 9X9X0.85-64L




Top View

Side View

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | | 9 BSC | |
| | Y | E | | 9 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | D2 | 5.1 | 5.2 | 5.3 |
| | Y | E2 | 5.1 | 5.2 | 5.3 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 1.5 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |



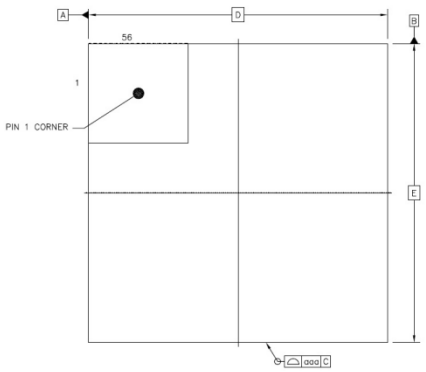

Bottom View

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

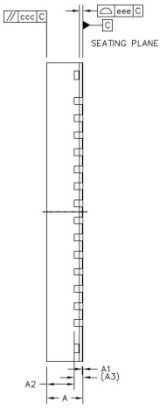
TQFN 9X9X0.85-64L(ZD64) POD Rev.0

Raystar Microelectronics Technology Inc

## TQFN 7X7X0.85-56L

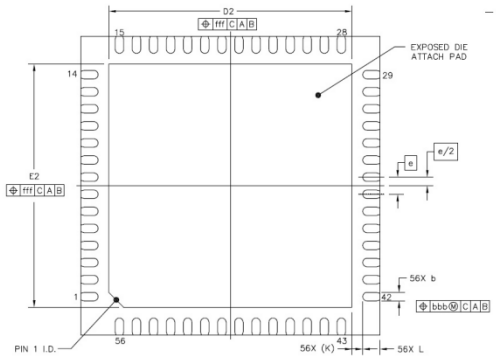



Top View




Side View

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | | 7 BSC | |
| | Y | E | | 7 BSC | |
| LEAD PITCH | | e | | 0.4 BSC | |
| EP SIZE | X | D2 | 5.6 | 5.7 | 5.8 |
| | Y | E2 | 5.6 | 5.7 | 5.8 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.25 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.07 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

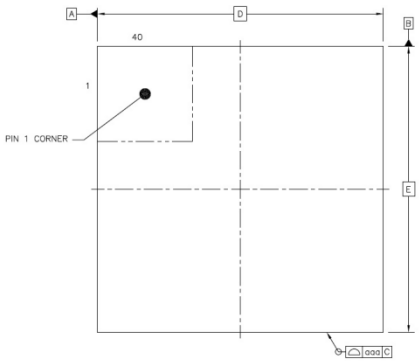



Bottom View

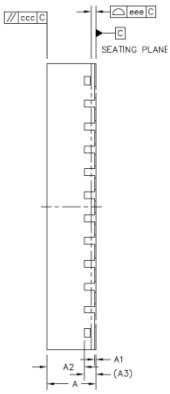
Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TQFN 7x7x0.85mm(ZL56) POD Rev.0
Raystar Microelectronics Technology Inc

## TQFN 5x5x0.85-40L

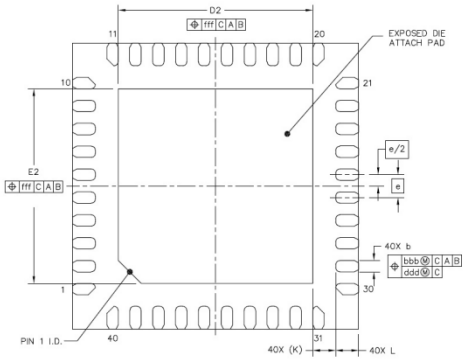



Top View




Side View

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | | 5 BSC | |
| | Y | E | | 5 BSC | |
| LEAD PITCH | | e | | 0.4 BSC | |
| EP SIZE | X | D2 | 3.3 | 3.4 | 3.5 |
| | Y | E2 | 3.3 | 3.4 | 3.5 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.4 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.07 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

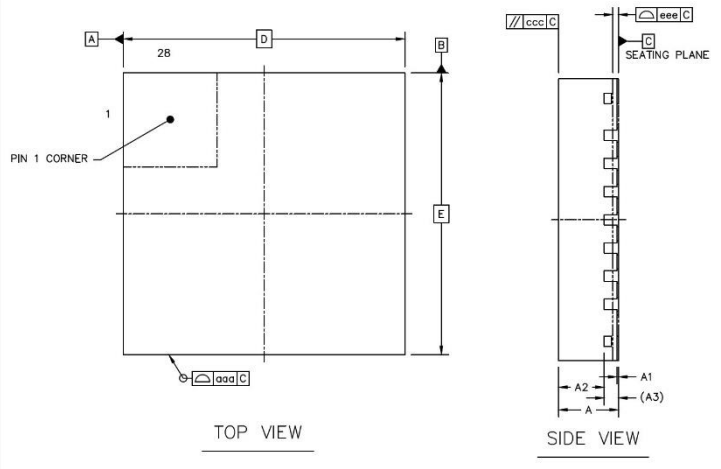


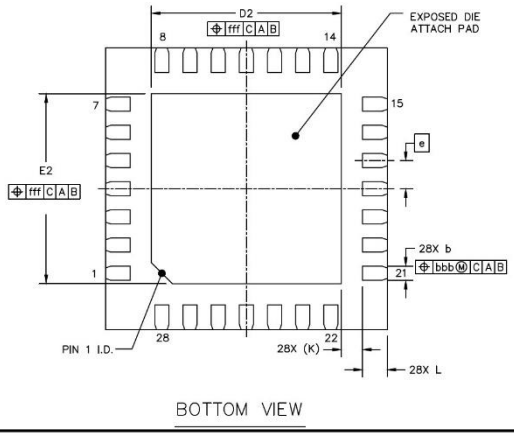

Bottom View

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TQFN 5x5x0.85mm(ZLA40) POD Rev.0
Raystar Microelectronics Technology Inc

## QFN 4x4x0.85-28L




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.647 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | | 4 BSC | |
| | Y | E | | 4 BSC | |
| LEAD PITCH | | e | | 0.4 BSC | |
| EP SIZE | X | D2 | 2.6 | 2.7 | 2.8 |
| | Y | E2 | 2.6 | 2.7 | 2.8 |
| LEAD LENGTH | | L | 0.25 | 0.35 | 0.45 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.3 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

Note:
1. All dimensions are in mm. Angels in degrees.
2. Refer Jedec MO-220.
3. Dimensions exclude burrs, mold flash or protrusions.

QFN4X4 28L POD Rev.0 (ZWA28)
Raystar Microelectronics Technology Inc.

# 7. Revision History

| Revision | Description | Date |
|---|---|---|
| V0.9 | Preliminary release | 2023/12/01 |
| V1.0 | Initial release | 2024/01/04 |
| V1.1 | 1.Modify several parameters.<br>2.Modify several pin types. | 2024/03/12 |
| V1.2 | 1.Update POD diagram for TQFN 10x10X0.85-72L(Page 74)<br>2.Modify CLK23 to CLK19,Byte 2 bit 7to Byte 0 bit 6, Byte 0 to Byte 1(Page 70) | 2024/9/24 |
| V1.3 | Add Part Number RS2CB19004 | 2025/01/17 |
| V1.4 | 1. Modify the RS2CB19004 Pin Descriptions error<br>2. Add PCIe Gen7 Data | 2025/12/3 |
| V1.5 | 1. Add RS2CB19004B, the default ouput amplitude is 750mV | 2026/08/31 |

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