RS7LSX108

Bi-directional Level Translator for
Open-drain and Push-Pull Applications

Features

- No Direction-Control
- Max Data Rates
  24Mbps (Push-Pull, 12MHz)
  1.2Mbps (Open-Drain, 0.6MHz)
- 1.1V to 5.5V on A ports and 1.1V to 5.5V on B Ports (VCCA≤VCCB)
- VCC Isolation: If Either VCC is at GND, Both Ports are in the High-Impedance State
- No Power-Supply Sequencing Required: VCCA or VCCB can be Ramped First
- Ioff Supports Partial Power-Down-Mode Operation
- ESD protection exceeds 4000V HBM
- Extended Temperature: -40°C to +125°C

Application

- I2C/SMBus, MDIO, SPI Interface
- Low-Voltage ASIC Level Translation
- Cell phone, Tablet, PC
- Server, Telecommunication

Description

The RS7LSX108 is a 8-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, VCCA and VCCB respectively.

A port supporting operating voltages from 1.1V to 5.5V while it tracks the VCCA supply, and the B ports supporting operating voltages from 1.1V to 5.5V while it tracks the VCCB supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V, 1.8V, 2.5V, 3.3V and 5V voltage nodes

The translator has integrated 10 kΩ pull-up resistors on the I/O lines. The integrated pull-up resistors are used to pull-up the I/O lines to either VCCA or VCCB. The RS7LSX108 is an excellent match for open-drain applications such as the I2C communication bus.

When the output-enable (EN) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, EN should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Information

Part Number	Package	Description
RS7LSX108L	TSSOP20	6.5 x 4.4 mm
RS7LSX108ZC	QFN-20	3.5 mm × 4.5 mm

Block Diagram

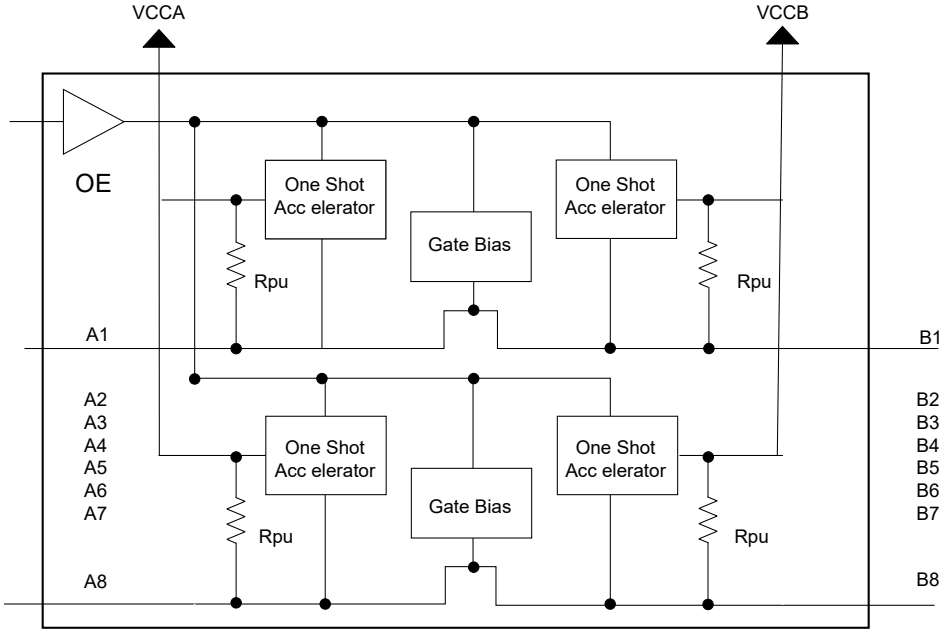
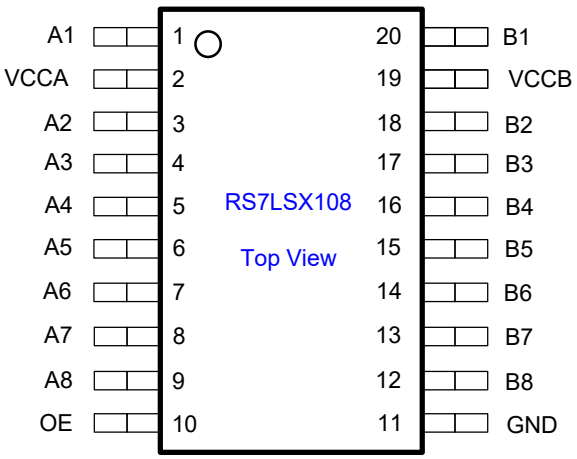


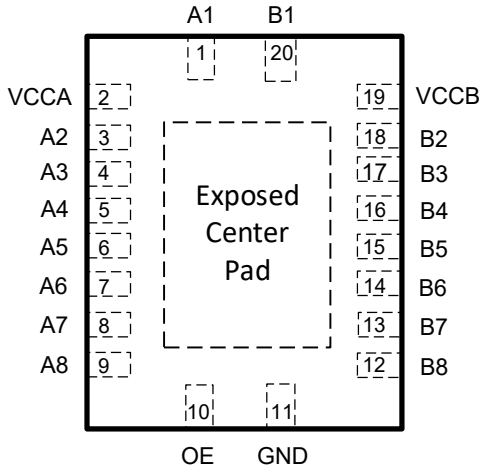
Figure 1: Block Diagram

Pin Configuration

TSSOP20 (Top view)



DFN 20 (Top view)



Pin Name	TSSOP-20	QFN-20	Type	Description
A1	1	1	I/O	Input/output 1. Referenced to VCCA
A2	3	3	I/O	Input/output 2. Referenced to VCCA
A3	4	4	I/O	Input/output 3. Referenced to VCCA
A4	5	5	I/O	Input/output 4. Referenced to VCCA
A5	6	6	I/O	Input/output 5. Referenced to VCCA
A6	7	7	I/O	Input/output 6. Referenced to VCCA
A7	8	8	I/O	Input/output 7. Referenced to VCCA
A8	9	9	I/O	Input/output 8. Referenced to VCCA
B1	20	20	I/O	Input/output 1. Referenced to VCCB
B2	18	18	I/O	Input/output 2. Referenced to VCCB
B3	17	17	I/O	Input/output 3. Referenced to VCCB
B4	16	16	I/O	Input/output 4. Referenced to VCCB
B5	15	15	I/O	Input/output 5. Referenced to VCCB
B6	14	14	I/O	Input/output 6. Referenced to VCCB
B7	13	13	I/O	Input/output 7. Referenced to VCCB
B8	12	12	I/O	Input/output 8. Referenced to VCCB
GND	11	11	—	Ground
OE	10	10	Input	Tri-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to VCCA.
VCCA	2	2	Power	A-port supply voltage. 1.1 V ≤ VCCA ≤ 5.5 V, VCCA ≤ VCCB.
VCCB	19	19	Power	B-port supply voltage. 1.1 V ≤ VCCB ≤ 5.5 V.

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
Tstore	Storage Temperature	−65	-	+150	°C
VCCA	DC Supply Voltage port B	-0.3	-	6.5	V
VCCB	DC Supply Voltage port A	-0.3	-	6.5	V
VIOB	Vi(A) referenced DC Input / Output Voltage	-0.3	-	6.5	V
VIOB	Vi(B) referenced DC Input / Output Voltage	-0.3	-	6.5	V
VOE	Enable Control Pin DC Input Voltage	-0.3	-	6.5	V
Ishort	Short circuit duration (I/O to GND)			50	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VCCA	VCCA Positive DC Supply Voltage	1.1	-	5.5	V
VCCB	VCCB Positive DC Supply Voltage	1.1	-	5.5	V
VOE	Enable Control Pin Voltage	GND	-	5.5	V
VIO	I/O Pin Voltage	GND	-	5.5	V
Δt /ΔV	Input transition rise or fall time	-	-	10	ns/V
TA	Operating Temperature Range	−40	-	+125	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 125°C, 1.1V≤V_{CCA}≤5.5V, 1.1V≤V_{CCB}≤5.5V

Symbol	Parameter	Test Conditions*1		MIN	TYP	MAX	Unit
VIHA	A port Input HIGH Voltage	1.1V≤VCCA ≤1.95		VCCA – 0.2			V
		1.95<VCCA ≤5.5V		VCCA – 0.4			V
VILA	A port Input LOW Voltage	1.1V≤VCCA≤5.5V		-	-	0.15	V
VIHB	B port Input HIGH Voltage	1.1V≤VCCA ≤1.95		VCCA – 0.2	-	-	V
		1.95<VCCA ≤5.5V		VCCA – 0.4			
VILB	B port Input LOW Voltage	1.1V≤VCCA≤5.5V		-	-	0.15	V
VIH(EN)	Control Pin Input HIGH Voltage	1.1V≤VCCA≤5.5V		0.65*VCCA	-	-	V
VIL(EN)	Control Pin Input LOW Voltage	1.95V≤VCCA≤5.5V		-	-	0.35*VCCA	V
		1.1V≤VCCA＜1.95V				0.15	
VOHA	A port Output HIGH Voltage	IOH = –20 μA 1.1V≤VCCA≤5.5V		0.67* VCCA	-	-	V
VOLA	A port Output LOW Voltage	IOH = 180 μA 1.1V≤VCCA≤1.65V		-	-	0.55	V
		IOH = 220 μA 1.65V≤VCCA≤2.3V					
		IOH = 300 μA 2.3V≤VCCA≤3V					
		IOH = 400 μA 3V≤VCCA≤4.5V					
		IOH = 620 μA 4.5V≤VCCA≤5.5V					
VOHB	B port Output HIGH Voltage	IOH = –20 μA 1.1V≤VCCB≤5.5V		0.67*VCCB	-	-	V
VOLB	B port Output LOW Voltage	IOH = 180 μA 1.1V≤VCCB≤1.65V		-	-	0.55	V
		IOH = 220 μA 1.65V≤VCCB≤2.3V					
		IOH = 300 μA 2.3V≤VCCB≤3V					
		IOH = 400 μA 3V≤VCCB≤4.5V					
		IOH = 620 μA 4.5V≤VCCB≤5.5V					
ICCA	VCCA Supply Current	EN=High	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V	-		12	μA
			VCCA= 5.5V, VCCB= 0V	-	-	12	μA
			VCCA= 0V, VCCB=5.5V	-		-2	μA
ICCB	VCCB Supply Current	EN=High	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V	-		12	μA
			VCCA= 5.5V, VCCB= 0V	-		-2	μA
			VCCA= 0V, VCCB=5.5V	-		12	μA
ICCA+ICCB	Combined supply current	EN=High	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V			24	μA
ICCZA	Static supply current VCCA	EN=Low	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V			12	μA
ICCZB	Static supply current VCCB					12	μA
I_{OZ}	I/O Tri−state Output Mode Leakage Current	A or B port EN=Low	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V			±2	μA
IOFF	Partial power down current	A port	VCCA=0V, VCCB=0V to 5.5V			±5	μA
		B port	VCCA=0V to 5.5V VCCB=0V			±5	μA
II-EN	Control pin leakage Current	VI = VCCI or GND		-	-	±2	μA

Note:

1. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design. Typical values are for V_{CCB} = +5 V, V_{CCA} = +3.3 V and T_A = +25°C.

AC Electrical characteristics

Timing Characteristics
(C_{LOAD} = 15pF, driver output impedance ≤ 50Ω, R_{LOAD} = 1 MΩ, T_A = -40°C to 125°C)

V_{CCA}= 1.2V±0.1V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 2.5V		VCCB = 3.3V		Unit
			MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		10		10	ns
		Open-drain		30		30	ns
tPLH_AB	Propagation Delay A → B	Push-pull		15		15	ns
		Open-drain		130		110	ns
tPHL_BA	Propagation Delay B → A	Push-pull		10		10	ns
		Open-drain		140		130	ns
tPLH_BA	Propagation Delay B → A	Push-pull		15		15	ns
		Open-drain		50		50	ns
tEN	Enable Time	EN to A or B		200		200	ns
tDIS	Disable Time	EN to A or B		200		200	ns
tRA	A port Rise Time	Push-pull		30		30	ns
		Open-drain		800		600	ns
tRB	B port Rise Time	Push-pull		30		30	ns
		Open-drain		800		600	ns
tFA	A port Fall Time	Push-pull		20		25	ns
		Open-drain		30		30	ns
tFB	B port Fall Time	Push-pull		20		25	ns
		Open-drain		30		30	ns
tSKEW	Channel to Channel Skew			1		1	1
MDR	Maximum Data Rate	Push-pull		24		24	Mbps
		Open-drain		0.8		0.8	Mbps

* Conversion from 1.2V to 1.8V or 5V is not advised.

V_{CCA}= 1.8V±0.15V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		10		9		9	ns
		Open-drain		30		30		30	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		11		11	ns
		Open-drain		100		100		100	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9		9	ns
		Open-drain		30		30		30	ns
tPLH_BA	Propagation Delay B → A	Push-pull		14		12		12	ns
		Open-drain		100		100		100	ns
tEN	Enable Time	EN to A or B		200		200		200	ns
tDIS	Disable Time	EN to A or B		300		300		300	ns
tRA	A port Rise Time	Push-pull		30		30		30	ns
		Open-drain		900		750		600	ns
tRB	B port Rise Time	Push-pull		30		30		30	ns
		Open-drain		900		750		600	ns
tFA	A port Fall Time	Push-pull		20		25		25	ns
		Open-drain		30		30		30	ns
tFB	B port Fall Time	Push-pull		25		30		30	ns
		Open-drain		30		30		30	ns
tSKEW	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull		24		24		24	Mbps
		Open-drain		0.8		0.8		1	Mbps

V_{CCA}= 2.5V±0.2V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		10		9		9	ns
		Open-drain		30		30		30	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		10		10	ns
		Open-drain		70		70		70	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9		9	ns
		Open-drain		30		30		30	ns
tPLH_BA	Propagation Delay B → A	Push-pull		14		12		12	ns
		Open-drain		70		70		70	ns
tEN	Enable Time	EN to A or B		200		200		200	ns
tDIS	Disable Time	EN to A or B		300		300		300	ns
tRA	A port Rise Time	Push-pull		30		30		30	ns
		Open-drain		1000		850		600	ns
tRB	B port Rise Time	Push-pull		30		30		30	ns
		Open-drain		1000		850		600	ns
tFA	A port Fall Time	Push-pull		20		30		30	ns
		Open-drain		30		30		30	ns
tFB	B port Fall Time	Push-pull		25		25		25	ns
		Open-drain		30		30		30	ns
tSKEW	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull		24		24		24	Mbps
		Open-drain		0.8		0.8		1	Mbps

V_{CCA}= 3.3V±0.3V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		9		9	ns
		Open-drain		30		30	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		12	ns
		Open-drain		50		30	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9	ns
		Open-drain		30		30	ns
tPLH_BA	Propagation Delay B → A	Push-pull		11		10	ns
		Open-drain		50		50	ns
tEN	Enable Time	EN to A or B		200		200	ns
t_{DIS}	Disable Time	EN to A or B		300		300	ns
tRA	A port Rise Time	Push-pull		30		30	ns
		Open-drain		120		120	ns
t_{RB}	B port Rise Time	Push-pull		30		30	ns
		Open-drain		900		700	ns
tFA	A port Fall Time	Push-pull		25		25	ns
		Open-drain		900		700	ns
t_{FB}	B port Fall Time	Push-pull		25		25	ns
		Open-drain		30		30	ns
tSKEW	Channel to Channel Skew			1		1	ns
MDR	Maximum Data Rate	Push-pull		24		24	Mbps
		Open-drain		0.8		1.2	Mbps

V_{CCA}= 5V±0.5V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 5V		Unit
			MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		9	ns
		Open-drain		30	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12	ns
		Open-drain		30	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9	ns
		Open-drain		30	ns
tPLH_BA	Propagation Delay B → A	Push-pull		10	ns
		Open-drain		50	ns
tEN	Enable Time	EN to A or B		200	ns
t_{DIS}	Disable Time	EN to A or B		300	ns
tRA	A port Rise Time	Push-pull		30	ns
		Open-drain		750	ns
t_{RB}	B port Rise Time	Push-pull		30	ns
		Open-drain		750	ns
tFA	A port Fall Time	Push-pull		25	ns
		Open-drain		30	ns
t_{FB}	B port Fall Time	Push-pull		25	ns
		Open-drain		30	ns
tSKEW	Channel to Channel Skew			1	ns
MDR	Maximum Data Rate	Push-pull		24	Mbps
		Open-drain		1.2	Mbps

Test Circuits

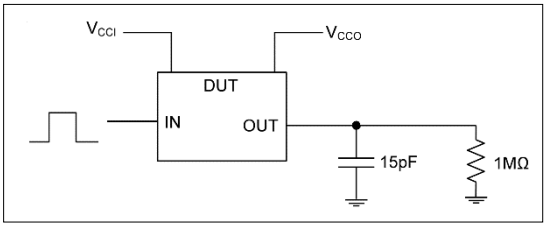


Figure 2 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

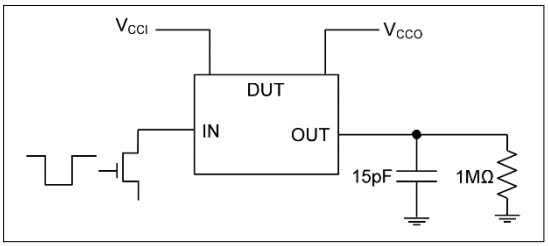
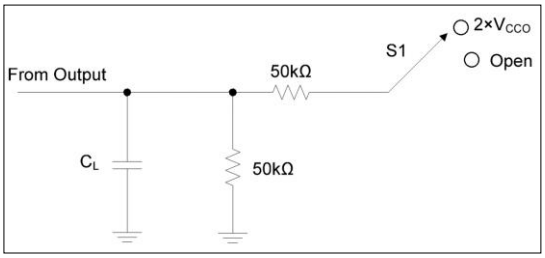


Figure 3 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} ,t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} ,t_{PZH} (t_{en})	Open

Figure 4 Load Circuit for Enable-Time and Disable-Time Measurement

Notes:

1. CL includes probe and jig capacitance.
2. t_{en} is the same as t_{PZL} and t_{PZH}. t_{dis} is the same as t_{PLZ} and t_{PHZ}.
3. V_{CCI} is the supply voltage associated with the input.
4. V_{CCO} is the supply voltage associated with the output.

Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

PRR ≤10 MHz
Z_O = 50 Ω
dv/dt ≥1 V/ns

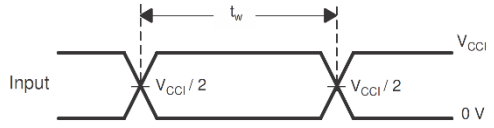


Figure 5 Pulse Duration

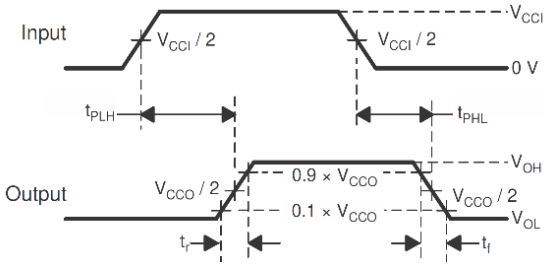


Figure 6 Propagation Delay Times

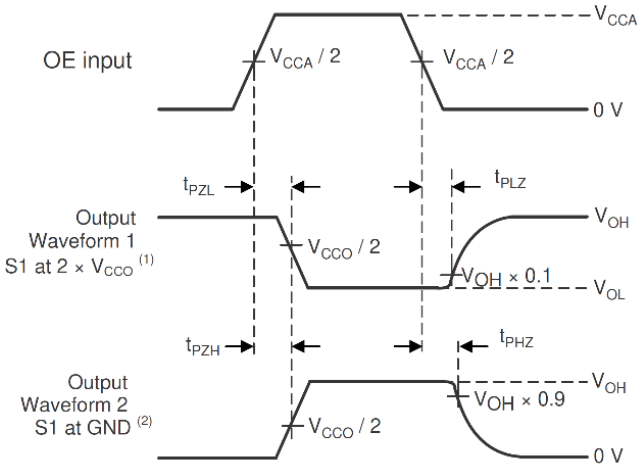


Figure 7 Enable and Disable Times

1. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
2. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Functional Description

The RS7LSX108 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.1 V to 5.5 V. The B-port accepts I/O voltages from 1.1 V to 5.5 V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

Each A-port I/O has a pull-up resistor (RPUA) to VCCA and each B-port I/O has a pull-up resistor (RPUB) to VCCB. RPUA and RPUB have a value of 40 kΩ when the output is driving low. RPUA and RPUB have a value of 4 kΩ when the output is driving high. RPUA and RPUB are disabled when OE = Low.

Architecture

Figure 8 describes semi-buffered architecture design this application requires for both push-pull and open- drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300 Ω to 500 Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design needs no direction- control signal (to control the direction of data flow from A to B or from B to A). The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

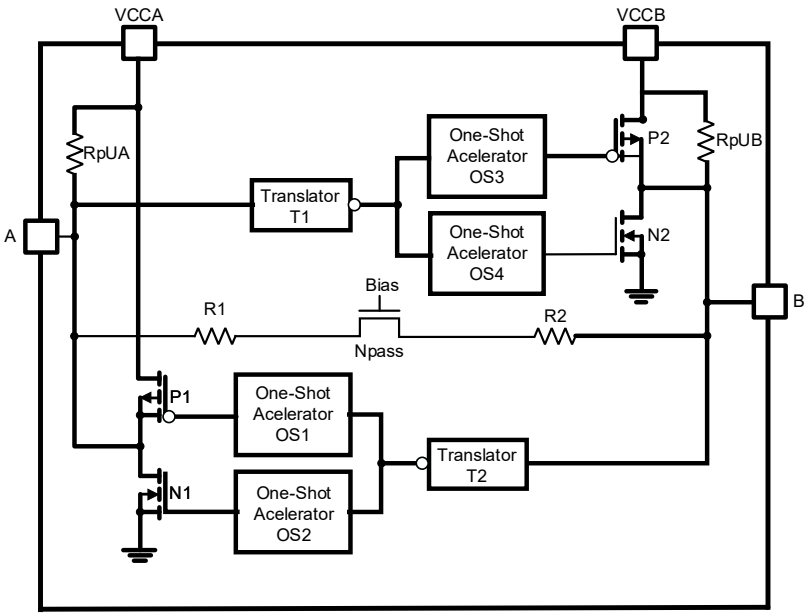


Figure 8 Level Shifter Architecture

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and these speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

Input Driver Requirements

The continuous DC-current sinking capability is determined by the external system-level open-drain (or push- pull) drivers that are interfaced to the RS7LSX108 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current sourcing capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time (tfA, tfB) of a signal depends on the edge-rate and output impedance of the external device driving RS7LSX108 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the tPHL and maximum data rates also depend on the output impedance of the external driver. The values for tfA, tfB, tPHL, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

Output Load Considerations

Raystar recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 15 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the RS7LSX108 output. Therefore, Raystar recommends that this lumped-load capacitance is considered in order to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Enable and Disable

The RS7LSX108 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (tdis) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (ten) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

Pull-up or Pull-down Resistors on I/O Lines

The RS7LSX108 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (RPUA) to VCCA and each B-port I/O has a pull-up resistor (RPUB) to VCCB. RPUA and RPUB have a value of 40 kΩ when the output is driving low. RPUA and RPUB have a value of 4 kΩ when the output is driving high. RPUA and RPUB are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower VOL values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

Device Functional Modes

The RS7LSX108 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

Application Information

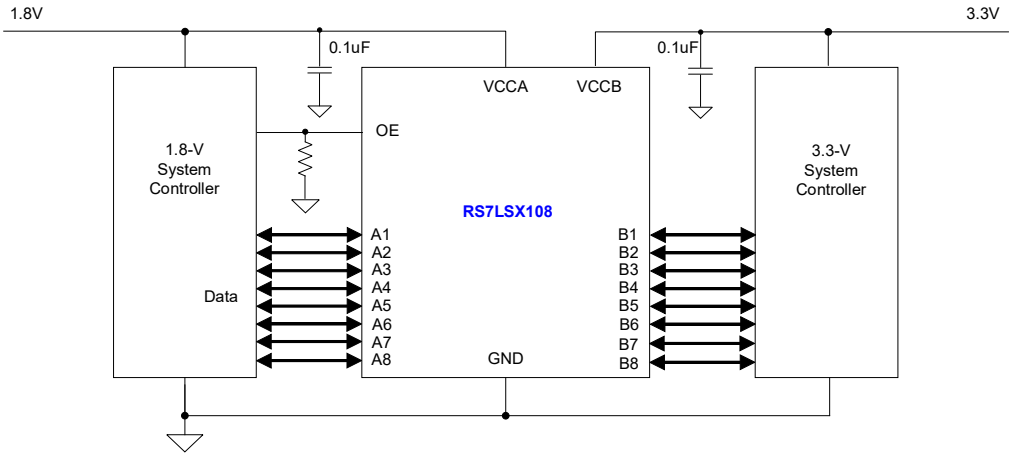


Figure 9 Application Circuit

Design Requirements

To begin the design process, determine the following:

Use the supply voltage of the device that is driving the RS7LSX108 device to determine the input and output voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.

The RS7LSX108 device has smart internal pull-up resistors. The max date rate under open-drain mode is 1.2Mbps. If a date rate is required, 10 kΩ pull-up resistors can be added at the input and output terminals.

External pull-up resistors can be added to reduce the total RC of a signal trace if necessary. An external pull-down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull-down resistor.

$$VOH = VCCx \times R_{PD} / (R_{PD} + 4\ k\Omega)$$

Power Supply Recommendations

During operation, ensure that VCCA ≤ VCCB at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by VCCA and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until VCCA and VCCB are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

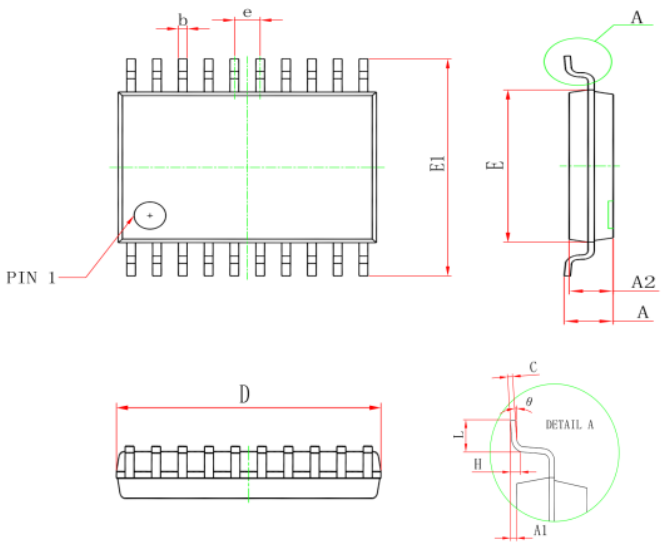
Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.

Short trace lengths should be used to avoid excessive loading.

PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 15 ns, ensuring that any reflection encounters low impedance at the source driver.

Package Information

TSSOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Note:
1. All dimensions are in mm. Angels in degrees.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MS-012

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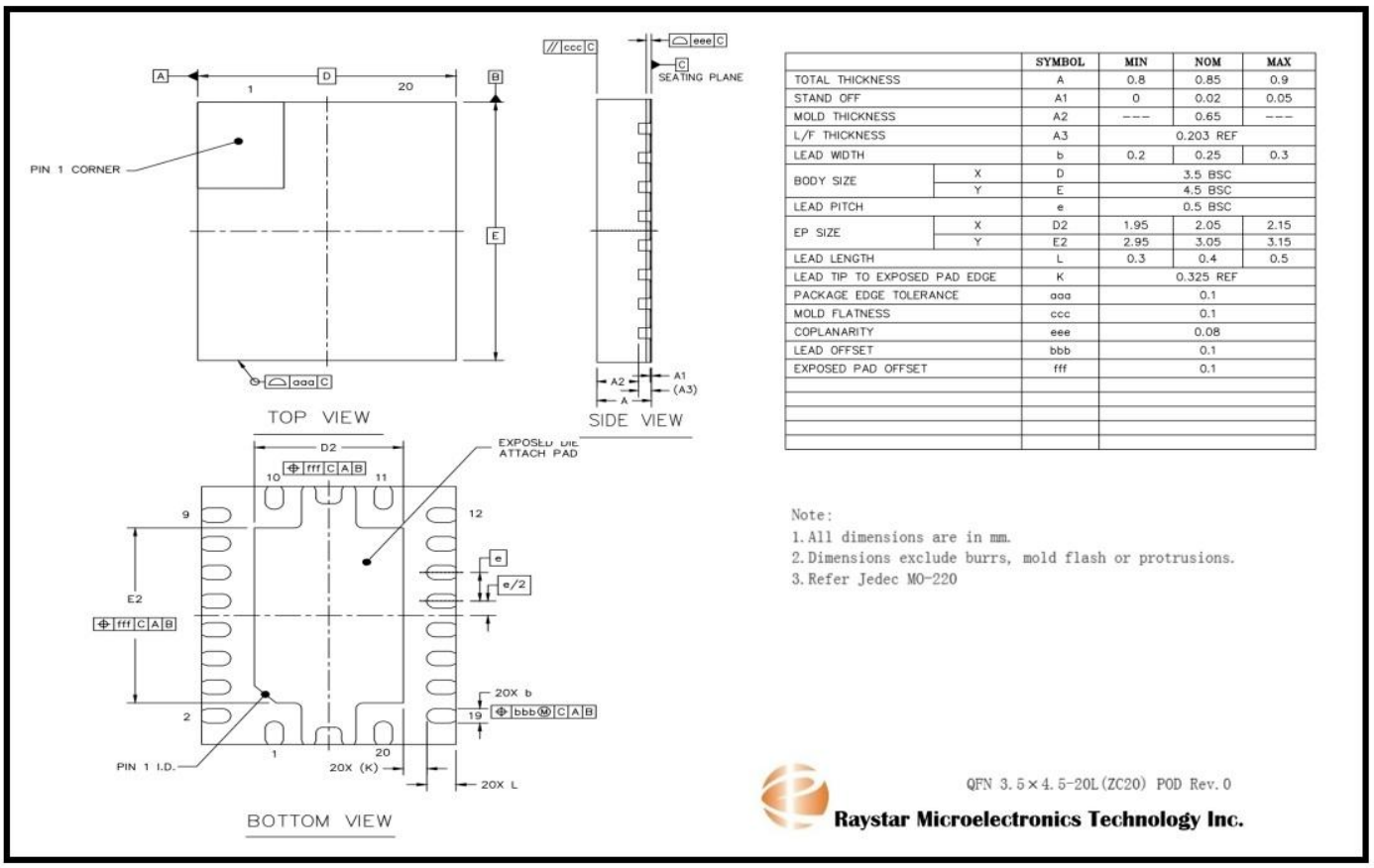
QFN-20



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.95	2.05	2.15
	Y	E2	2.95	3.05	3.15
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Note:
1. All dimensions are in mm.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MO-220

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Revision History

Revision	Description	Date
0.9	Preliminary	2026/3/3
1.0	Initial Release	2026/4/22
1.1	Revise the architecture and application circuit description.	2026/8/13