Features

- Supply voltage: 1.7 V to 3.6 V
- Battery supply voltage: 1.55 V to 3.6 V
- Built-in 32.768 kHz DTCXO
- Provides year, month, day, weekday, hours, minutes and seconds based on a 32.768 kHz quartz crystal
- Real-time clock and calendar
- Two independent IIC with speed 400 kHz Max.
- IIC clock Timeout 35 ms max
- Support both Binary Mode and BCD Mode.
- Support Daylight Saving Mode.
- Support 24-hour and 12-hour Mode.
- RTC_CLR、Alarm、Interrupt、RTC Fail、Oscillator Fail flag.
- Battery-backed 128 byte SRAM
- Offset register
- Operating temperature : -40 °C to 85 °C.

Description

The RS4TC85053ZK build in a 32.768 kHz DTCXO.

In addition to providing a calendar optimized for low power consumption and automatic switching to battery on primary power loss. Featuring clock output, ALRT (interrupt) output and 128 bytes of battery backup SRAM. The RS4TC85053ZK includes two IIC buses. The primary IIC bus has the read/write capability on RTC and SRAM registers. The second IIC bus also can read/write most registers with the control bits set by primary IIC controller.

Ordering Information

Part Number	Package	Package Description
RS4TC85053ZK	DFN12	12 terminals; 0.5 mm pitch; 3 mm x 3 mm x 1.15 mm body

Applications

- Server and computer precision timekeeping
- Network-powered and industrial electronics
- Products with long automated unattended operation time
- White goods

Function Block

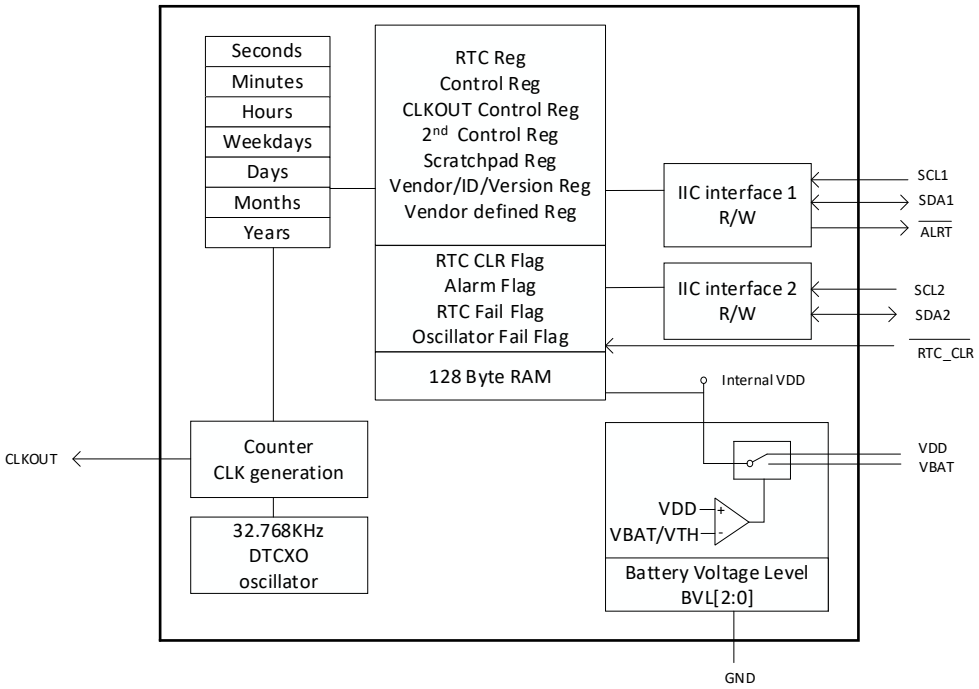


Figure1 Function block

Typical Application Circuit

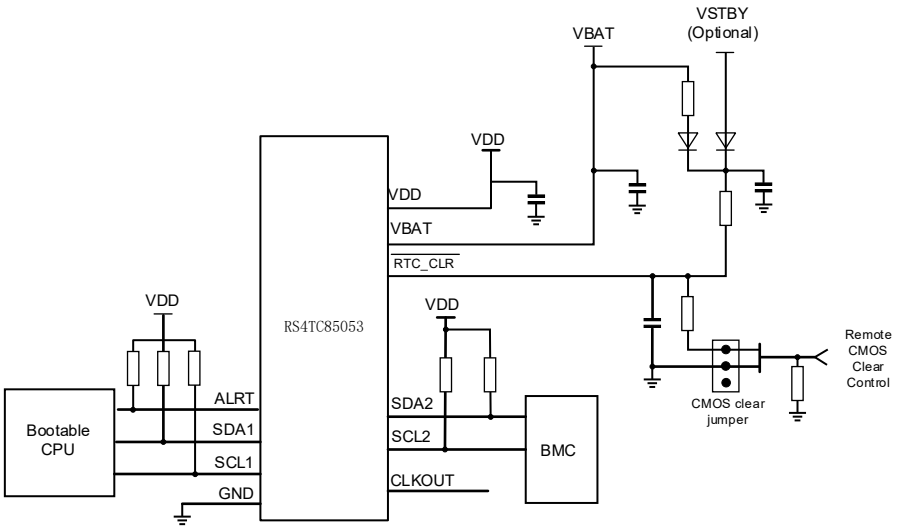


Figure2 Typical application circuit(with battery)

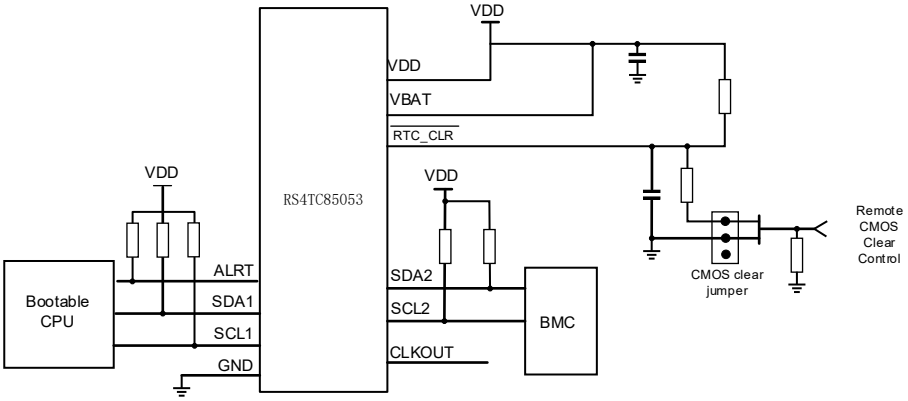


Figure3 Typical application circuit(without battery)

Pin Configuration

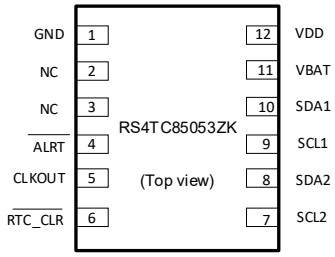


Figure4 Pin configuration

Pin Description

Symbol	Pin	Type	Description
GND	1	Supply	ground supply voltage
NC	2	/	No use
NC	3	/	No use
ALRT	4	O	interrupt output, open-drain and active-low
CLKOUT	5	O	clock output
RTC_CLR	6	I	active low to clear battery-backed SRAM
SCL2	7	I	2nd IIC bus serial clock
SDA2	8	I/O	2nd IIC bus serial data
SCL1	9	I	primary IIC bus serial clock
SDA1	10	I/O	Primary IIC bus serial data
V_{BAT}	11	Supply	battery backup supply voltage
V_{DD}	12	Supply	supply voltage

Function Description

The RS4TC85053ZK contains 8-bit registers for time information and 128 byte SRAM-related system configuration. Included is an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the real-time Clock (RTC) and calendar, and two IIC-bus interfaces with a maximum frequency 400 kHz.

The first IIC bus can read all RTC and SRAM registers including read and write most of registers except the read-only registers.

The second IIC bus can read all RTC and SRAM registers, while write capability for some registers is blocked, or gated by the primary IIC bus.

The built-in address register will increment automatically after each read or write of a data byte. After register FFh, the auto-incrementing will wrap around to address 00h. When the SRAM is accessed, the wrap-around will happen after address 7Fh.

All registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

The seconds, minutes, hours, days, months, and years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format or binary format.

When reading the RTC time registers, the contents of all time registers are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented. The internal counters are running at background to maintain the time accuracy.

RTC and SRAM registers overview

Device	Device address
RTC	1101 111
SRAM	1010 111

The time registers Offset 0 to 09h. They can be coded in the BCD format or binary format.

The other registers (0Ah to 11h) are the control register, status register, CLKOUT control register, version register,…etc.

Registers Table

Address	Register	BCD Data Mode									Binary Mode	Default[1]
		D7	D6	D5	D4	D3	D2	D1	D0	Range	Range	
00h	Seconds	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
01h	Seconds Alarm	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
02h	Minutes	0	x10 mins			x1 Minutes				00-59	00-3B	00h
03h	Minutes Alarm	0	x10 mins			x1 Minutes				00-59	00-3B	00h
04h	Hours (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hours (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
05h	Hours Alarm (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hours Alarm (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
06h	Day of the Week (Sunday =1)	Day of Week								1-7	01-07	07h
07h	Day of the Month[2]	Day of Month								1-31	01-1F	01h
08h	Month	Month								1-12	01-0C	01h
09h	Year	Year								0-99	00-63	00h
0Ah	Control Register	ST	DM	HF	DSM	AIE	OFIE	CIE	TWO	-	-	00h
0Bh	Status Register	AF	OF	RTCF	CIF	-	BVL2	BVL1	BVL0	-	-	-
0Ch	CLKOUT Control	CKE	-	-	-	-	-	CKD [1:0]		-	-	00h
0Dh	2nd Control Register	-	-	-	-	-	-	-	MWO			00h
0Eh	Scratchpad	Scratchpad register										00h
0Fh	Version Register	Major Version				Minor Version				-	-	10h
10h	Vendor ID Register	Vendor Code										66h
11h	Model Register	Model Code										53h
12h	Offset	OFFSET [7:0]								-	-	00h
13h	Oscillator	-	OFFM	-	-							02h
14h	Access config	XCLK	-	-	-	-	-	-	-	-	-	00h
15h	Sec_timestp	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
16h	Min_timestp	0	x10 mins			x1 Minutes				00-59	00-3B	00h

Address	Register	BCD Data Mode					Binary Mode	Default[1]
17h	Hour timestp (12 Hour Mode)	0:AM 1:PM	0	x10 Hours	x1 Hours	1-12	01-0C (AM) 81-8C (PM)	12h
	Hour_timestp (24 Hour Mode)	0	0	x10 Hours	x1 Hours	00-23	00-17	12h
18h	DayWk_timestp (Sunday =1)	Day of Week				1-7	01-07	07h
19h	DayMon_timestp	Day of Month				1-31	01-1F	01h
1Ah	Mon_timestp	Month				1-12	01-0C	01h
1Bh	Year_timestp	Year				0-99	00-63	00h
1Ch	R_code1	R code 1				-	-	00h
1Dh	R_code2	R code 2				-	-	00h
1Eh to FFh	reserved	reserved				-	-	00h

[1] After power up, all registers are set to the associated default value.

[2] If the year counter contains a value, which is exactly divisible by 4, the RS4TC85053ZK compensates for leap years by adding a 29th day to February

RTC register read/write capability by the two IIC buses

Address	Register	Primary IIC		2nd IIC		Note
control bit TWO		TWO=1	TWO=0 (default)	TWO=1	TWO=0 (default)	Only primary IIC controller can write “TWO” bit
00h	Seconds	Read/Write	Read only	Read only	Read/Write	
01h	Seconds Alarm	Read/Write		Read only		
02h	Minutes	Read/Write	Read only	Read only	Read/Write	
03h	Minutes Alarm	Read/Write		Read only		
04h	Hours (12 Hour Mode)	Read/Write	Read only	Read only	Read/Write	
	Hours (24 Hour Mode)	Read/Write	Read only	Read only	Read/Write	
05h	Hours Alarm (12 Hour Mode)	Read/Write		Read only		
	Hours Alarm (24 Hour Mode)	Read/Write		Read only		
06h	Day of the Week (Sunday =1)	Read/Write	Read only	Read only	Read/Write	
07h	Day of the Month	Read/Write	Read only	Read only	Read/Write	
08h	Month	Read/Write	Read only	Read only	Read/Write	
09h	Year	Read/Write	Read only	Read only	Read/Write	
0Ah	Control Register	Read/Write	Read/ Write	Read only	Read only	
0Bh	Status Register	Read/Write	Read/ Write	Read only	Read only	

Address	Register	Primary IIC		2nd IIC		Note
control bit XCLK		XCLK=1	XCLK=0 (default)	XCLK=1	XCLK=0 (default)	Only primary IIC controller can write “XCLK” bit
0Ch	CLKOUT Control	Read/Write	Read only	Read only	Read/Write	
12h	Offset Register	Read/Write	Read only	Read only	Read/Write	
13h	Oscillator Register	Read/Write	Read only	Read only	Read/Write	

Access config		Primary IIC	2nd IIC
0Dh	2nd Control Register	Read/Write	Read only
0Eh	Scratchpad	Read/Write	Read only
14h	Access config	Read/Write	Read only

Read only Register		Primary IIC	2nd IIC
0Fh -11h	Version Model related registers	Read only	Read only
15h - 1Dh	Timestamp and R_code registers	Read only	Read only
1Eh – FFh	reserved	Read only	Read only

SRAM register map

Address	Register name	Reset By	Default	Note
00h-7Fh	SRAM Byte	RTC_CLR	00h	128 bytes of battery backup SRAM

SRAM registers read/write capability by the two IIC buses

Address	Register	Primary IIC		2nd IIC		Note
control bit MWO		MWO=1	MWO=0 (default)	MWO=1	MWO=0 (default)	Only primary IIC controller can write “MWO” bit. This bit is in RTC 2nd control register.
00h-7Fh	SRAM Byte	Read/Write	Read only	Read only	Read/Write	

Time, calendar and alarm registers (00h to 09h)

The processor program can access time and calendar information by reading the appropriate locations. The contents of the time, calendar and alarm registers (00h to 09h) may be either binary or binary-code decimal(BCD). These registers are updated once per second.

BCD time format

The Binary-Coded Decimal (BCD) encodes numbers where each digit is represented by a separate bit field. Each bit field may only contain the values 0 to 9. In this way, decimal numbers and counting is implemented.
Example: 59 encoded as an entire number is represented by 3Bh or 111011. In BCD the 5 is represented as 5h or 0101 and the 9 as 9h or 1001 which combines to 59h.

	Upper-digit (ten’s place)				Digit (unit place)			
	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
…	…	…	…	…	…	…	…	…
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1
..	…	…	…	…	…	…	…	…
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

Setting and reading the time registers

The data flow and data dependencies starting from the 1 Hz clock tick.

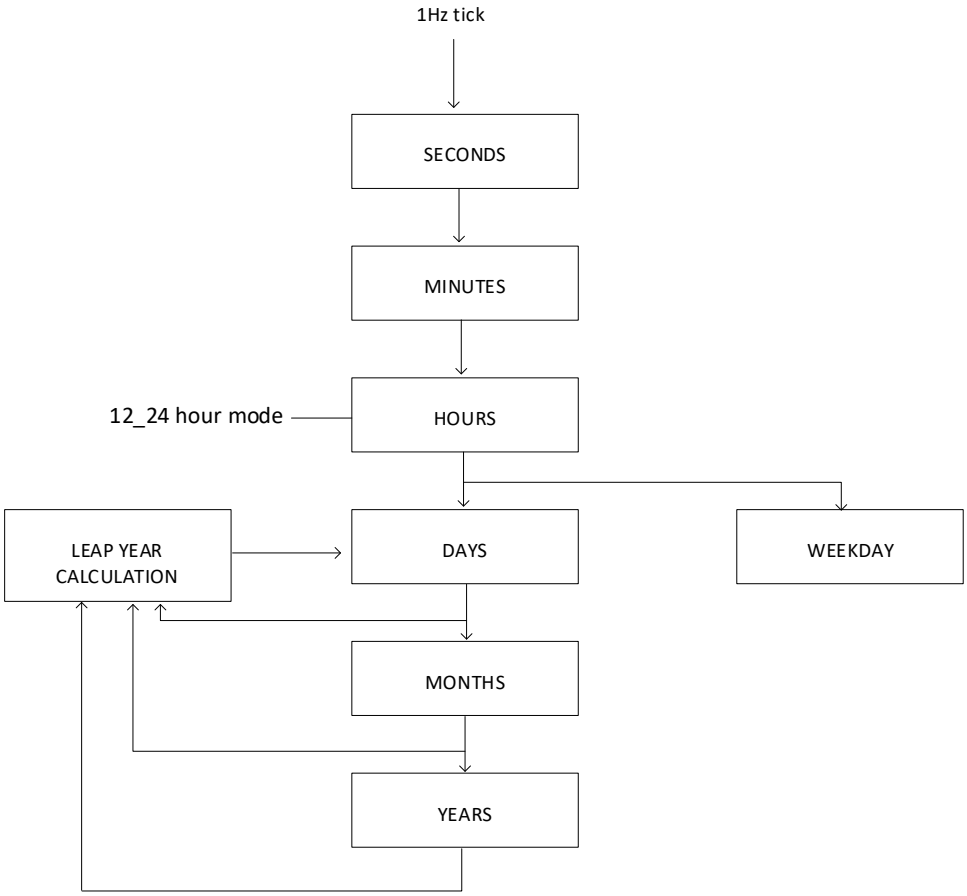


Figure5 Data flow for the time function

During read operations, the time registers are copied into an output register. The RTC continues counting in the background. When reading or writing the time it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

Alarm registers (01h, 03h and 05h)

The alarm registers are located at 01h for seconds alarm, 03h for minutes alarm, 05h for hours alarm.
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the AIE alarm interrupt enable bit bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes.
The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation.

- An alarm interrupt **each hour** is created with a "don't care" code in the hours alarm byte.
- An alarm interrupt **each minute** is is created with "don't care" codes in the hours and minutes alarm bytes.
- An alarm interrupt **each second** is created with a "don't care" code in the hours, minutes and seconds alarm bytes.

Address	Register	BCD Range	Binary Range	Default	Primary IIC	2nd IIC
01h	Seconds Alarm	00-59	00-3B	00h	Read/Write	Read only
03h	Minutes Alarm	00-59	00-3B	00h	Read/Write	Read only
05h	Hours Alarm (12 Hour Mode)	1-12	01-0C (AM) 81-8C (PM)	12h	Read/Write	Read only
	Hours Alarm (24 Hour Mode)	00-23	00-17	12h	Read/Write	Read only

Control, status, CLKOUT, and 2nd control register (0Ah to 0Dh)

The control register is to control related RTC function.
The status register is to show the status of alarm setting, oscillator status and battery voltage range. The CLKOUT register is to for clock output configuration.
The second control register is the additional control register.

Address	Register	Primary IIC	2nd IIC
0Ah	Control Register	Read/write	Read only
0Bh	Status Register	Read/write	Read only
0Dh	2^{nd} Control Register	Read/write	Read only
0Ch	CLKOUT Control	Read/write (XCLK=1)	Read/write (XCLK=0)

Control register (0Ah)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	Control Register	ST	DM	HF	DSM	AIE	OFIE	CIE	TWO

Bit	Symbol	Reset by	Value	Description
D7	ST (Stop)	N/A	0	Normal Mode
			1	Stop the RTC
D6	DM (Data Mode)	N/A	0	BCD Mode
			1	Binary Mode
D5	HF (Hour Format)	N/A	0	12 Hour Mode
			1	24 Hour Mode
D4	DSM (Daylight Saving Mode)	N/A	0	Disable Daylight Saving Mode
			1	Enable Daylight saving Mode
D3	AIE (Alarm Interrupt Enable)	RTC_CLR	0	Disable Alarm Interrupt
			1	Enable Alarm Interrupt. Allows an interrupt to occur when the AF is set from an alarm match from the update cycle.
D2	OFIE (Oscillator Fail Interrupt Enable)	RTC_CLR	0	Disable the Oscillator Fail Interrupt
			1	Enable the Oscillator Fail Interrupt
D1	CIE (RTC Clear Interrupt Enable)	N/A	0	Disable interrupt (ALRT Assertion) when the RTC_CLR assertion is detected
			1	Enable interrupt (ALRT Assertion) when the RTC_CLR assertion is detected
D0	TWO (Time Reg Write Ownership)	N/A	0	2nd IIC bus has the write access to the Time registers
			1	Primary IIC bus has the write access to the Time registers.

ST bit function

The function of the ST (stop) bit is to allow for accurate starting of the time circuits. The ST bit function will cause the upper part of the prescaler (F2 to F14) to be held in reset and thus no 1 Hz ticks will be generated . The time circuits can then be set and will not increment until the ST bit is released.

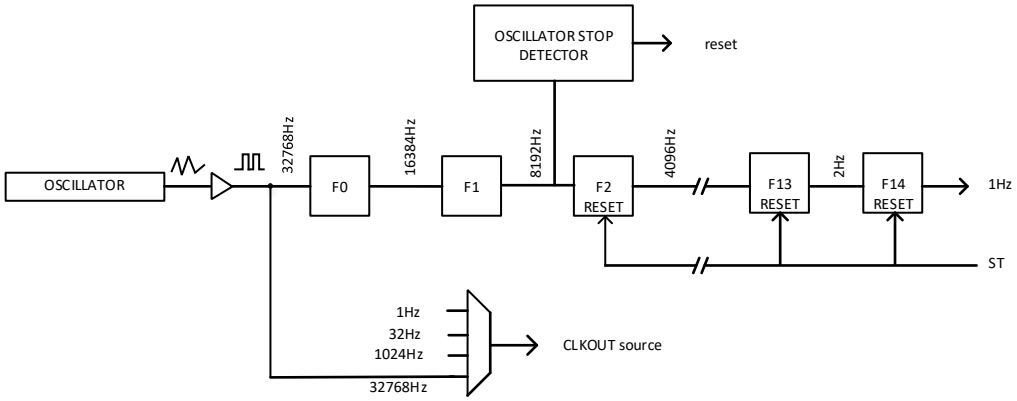


Figure6 ST bit function diagram

The ST bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz, and 1 Hz.

The lower two stages of the prescaler (F0 and F1) are not reset; and because the IIC-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8.192 kHz cycle.

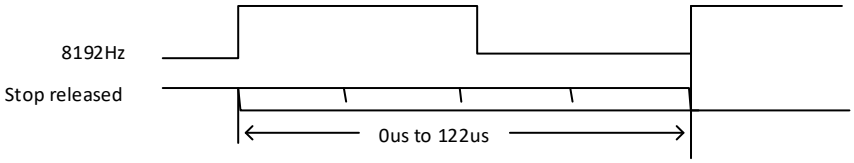
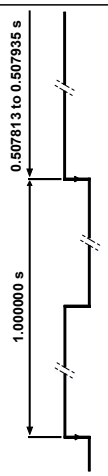


Figure7 ST bit release timing

Bit ST	Prescaler bits F0F1-F2 to F14	[1]	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally					
0	01-0 0001 1101 0100			12:45:12	prescaler counting normally
ST bit is activated by user. F0F1 are not reset and values cannot be predicted externally					
1	XX-0 0000 0000 0000			12:45:12	prescaler is reset; time circuits are frozen
New time is set by user					
1	XX-0 0000 0000 0000			8:00:00	prescaler is reset; time circuits are frozen
ST bit is released by user					
	XX-0 0000 0000 0000			8:00:00	prescaler is now running
	XX-1 0000 0000 0000			8:00:00	-
	XX-0 1000 0000 0000			8:00:00	-
	XX-1 1000 0000 0000			8:00:00	-
	:			:	:
	11-1 1111 1111 1110			8:00:00	-
	00-0 0000 0000 0001			8:00:01	0 to 1 transition of F14 increments the time circuits
	10-0 0000 0000 0001			8:00:01	-
	:			:	:
	11-1 1111 1111 1111			8:00:01	-
	00-0 0000 0000 0000			8:00:01	-
	10-0 0000 0000 0000			8:00:01	-
	:			:	-
	11-1 1111 1111 1110			8:00:01	-
	00-0 0000 0000 0001			8:00:02	0 to 1 transition of F14 increments the time circuits



The first increment of the time circuits is between 0.507813 s and 0.507935 s after ST bit is released. The uncertainty is caused by the prescaler bits F0 and F1 not being reset (see Table 17) and the unknown state of the 32 kHz clock.

DSM bit function

The daylight saving mode is enabled by DSM (Daylight Saving Mode) =1. The spec is shown below:

- The first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM.
- The last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM

Status register (0Bh)

Status register (0Bh) describes the statuses of Alarm flag, oscillator fail bit, RTC fail bit and RTC clear flag.

The BVL[2:0] bits are measured and updated once per second.

Address	Register	D7	D6	D5	D4	D3	D2-D0
0Bh	Status Register	AF	OF	RTCF	CIF	Rsvd	BVL[2:0][1]

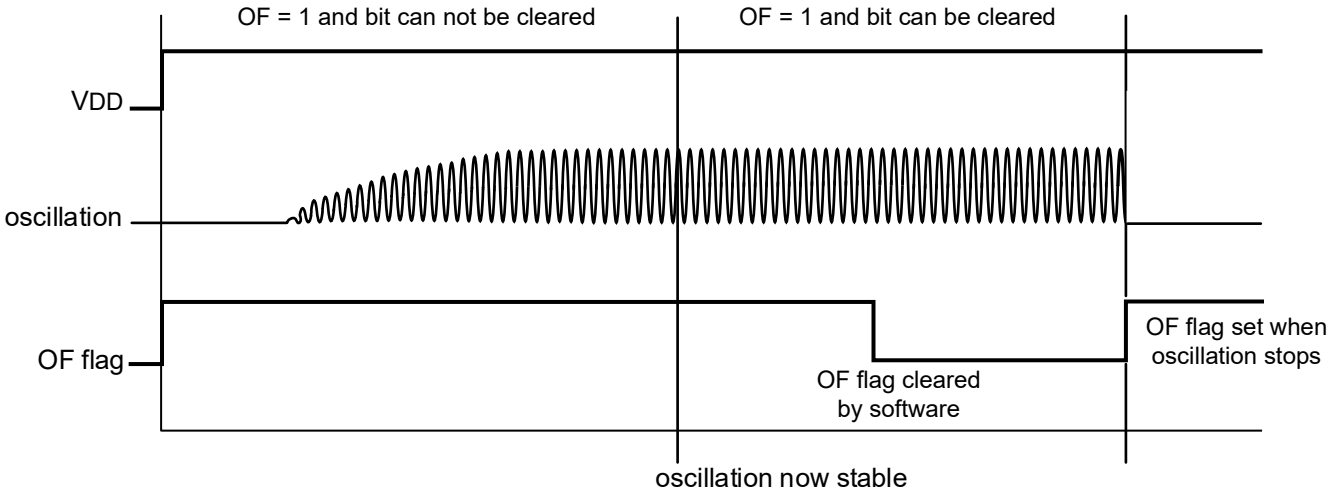
[1] BVL[2:0] are read only.

Bit	Symbol	Reset by	Value	Description
D7	AF (Alarm Flag)	RTC_CLR	1	after all Alarm values Match the current time.
			0	Write '0' to clear it.
D6	OF (Oscillator Fail Bit/Flag)	N/A	1	Set when oscillator failed/stopped. Set in following Conditions: 1. First Time power is applied. 2. Oscillator has failed (freq is either zero or very far away from the desired 32.768KHz) 3. The ST Bit is Set to '1'
			0	Write '0' to clear it.
D5	RTCF (RTC Fail Bit)	N/A	1	Set when device powers up after lost all power (V_{DD} and V_{BAT}).
			0	Write '0' to Clear it.
D4	CIF (RTC Clear Flag)	N/A	1	Set when the RTC_CLR Pin assertion is detected.
			0	Write '0' to clear it.
D3	Rsvd	N/A	-	Reserved
D2 – D0	BVL[2:0]	N/A	000	Battery Voltage Level ⩽1.7 V
			001	Battery Voltage Level (1.7 V, 1.9V]
			010	Battery Voltage Level (1.9V, 2.1V]
			011	Battery Voltage Level (2.1V, 2.3V]
			100	Battery Voltage Level (2.3V, 2.5V]
			101	Battery Voltage Level (2.5V, 2.7 V]
			110	Battery Voltage Level (2.7 V, 3.0V]
			111	Battery Voltage Level > 3.0V

OF (Oscillator Fail Flag)

The OF flag is set whenever the oscillator is “first time power is applied”, “Oscillator has failed” or “the ST Bit is Set to ‘1’”. The flag remains set until cleared by using the IIC interface. When the oscillator is not running, then the OF flag cannot be cleared. This method can be used to monitor the oscillator.

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in a range of 200 ms to 2 s, depending on crystal type, temperature, and supply voltage.



CLKOUT Control register (0Ch)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	CLKOUT Control	CKE	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	CKD1	CKD0

Bit	Symbol	Value	Description
D7	CKE (Clock Output Enable)	1	The Clock Output is activated. Note: Clock Output is always disabled when only powered by VBAT. (VDD is not valid)
		0	CLKOUT output is inhibited and pin is set to high-impedance
D6-D2	Rsvd	-	Reserved
D1-D0	CKD[1:0]	00 01 10 11	32.768kHz 1.024 kHz 32 Hz 1 Hz

2nd Control Register (0Dh)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	2nd control register	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	MWO

Bit	Symbol	Reset by	Value	Description
D7-D1	Rsvd	N/A	-	Reserved
D0	MWO	$\overline{\text{RTC\_CLR}}$	0	2nd IIC bus has the write access to the SRAM registers
			1	Primary IIC bus has the write access to the SRAM registers.

If an IIC write transaction is performed on the secondary IIC bus while the primary IIC bus writes to the 2nd Control register, the synchronization of the internal MWO state may be delayed.
While writing to this 2nd Control register, ensure there is no ongoing write on the secondary IIC bus. If not, perform an IIC read or write transaction of any register on the primary IIC bus to have a correct MWO state.

Scratchpad register (0Eh)

Address	Register	D7-D0	default	Primary IIC	2nd IIC
0Eh	Scratchpad	Scratchpad register	00h	Read/Write	Read only

Version related register (0Fh, 10h and 11h)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	Version	0	0	0	1	0	0	0	0
10h	Vendor	0	1	1	0	0	1	1	0
11h	Model	0	1	0	1	0	0	1	1

Offset register (12h)

The RS4TC85053ZK incorporates an offset register (address 12h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

Address	Register	D7 – D0	Description
12h	Offset	OFFSET[7:0]	Offset value

Address	Register	Primary IIC		2nd IIC		Note
control bit XCLK		XCLK=1	XCLK=0 (default)	XCLK=1	XCLK=0 (default)	Only primary IIC controller can write "XCLK" bit
12h	Offset Register	Read/Write	Read only	Read only	Read/Write	For clock calibration,the primary IIC can change the access capability

There are two modes which define the correction period, normal mode and fast mode.
The normal mode is suitable for offset trimming. The fast mode is suitable for dynamic offset correction e.g. implementing a temperature correction. The fast mode consumes more current. Offset mode is defined by bit OFFM in the Oscillator register.
To program a new OFFSET[7:0] or OFFM value, it requires to wait 135 ms min after an OFFSET[7:0] or OFFM write-event respectively.

OFFM bit - oscillator control register (address 13h)

Bit	Symbol	Value	Description
6	OFFM		offset mode bit
		0 (default)	normal mode: correction is made every 4 hours; 2.170 ppm/step
		1	fast mode: correction is made once every 8 minutes;2.0345 ppm/ step

For OFFM = 0, each LSB introduces an offset of 2.170 ppm. For OFFM = 1, each LSB introduces an offset of 2.0345 ppm. The offset value is coded in two's complement giving a range of +127 LSB to -128 LSB.

OFFSET[7:0]	Offset value in decimal	Offset value in ppm	
		Normal mode OFFM = 0	Fast mode OFFM = 1
01111111	+127	+275.590	+258.3815
01111110	+126	+273.420	+256.3470
:			:
00000010	+2	+4.340	+4.0690
00000001	+1	+2.170	+2.0345
00000000IU	0	0 (default)	0
11111111	-1	-2.170	-2.0345
11111110	-2	-4.340	-4.0690
:			:
10000001	-127	-275.590	-258.3815
10000000	-128	-277.760	-260.416

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied.

Correction when OFFM = 0

The correction is triggered once every four hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Correction value	Every n^{th} hour	Actual minute
+1 or-1	4	00
+2 or -2	4	00 and 01
+3 or-3	4	00, 01, and 02
:	:	:
+59 or -59	4	00 to 58
+60 or -60	4	00 to 59
+61 or-61	4	00 to 59
	4 + 1	00
+62 or -62	4	00 to 59
	4 + 1	00 and 01
:	:	:
+123 or-123	4	00 to 59
	4 + 1	00 to 59
	4+2	00, 01, and 02
-128	4	00 to 59
	4 + 1	00 to 59
	4+2	00 to 07

Correction when OFFM = 1

The correction is triggered once every eight minutes and then correction pulses are applied once per second until the programmed correction values have been implemented.

Clock correction is made more frequently in OFFM = 1; however, this can result in higher power consumption.

Correction value	Every n^{th} minute	Actual second
+1 or-1	8	00
+2 or -2	8	00 and 01
+3 or-3	8	00, 01, and 02
:	:	:
+59 or -59	8	00 to 58
+60 or -60	8	00 to 59
+61 or-61	8	00 to 59
	8 + 1	00
+62 or -62	8	00 to 59
	8 + 1	00 and 01
:	:	:
+123 or-123	8	00 to 59
	8 + 1	00 to 59
	8 + 2	00, 01, and 02
-128	8	00 to 59
	8 + 1	00 to 59
	8 + 2	00 o 07

Offset calibration workflow

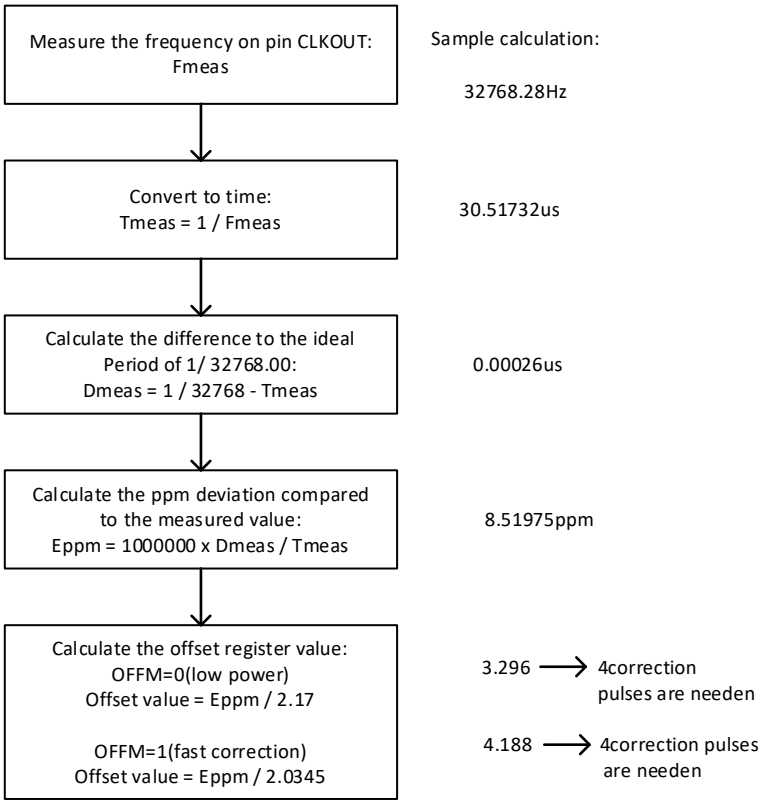


Figure8 Offset calibration calculation workflow

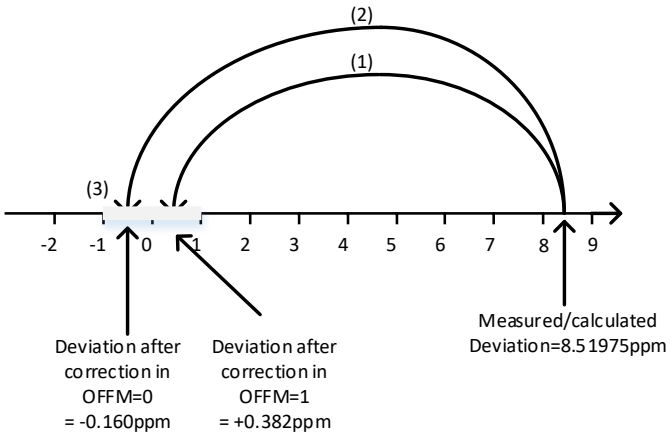


Figure 9. Result of offset calibration

(1) 4 correction pulses in OFFM = 0 correspond to -8.680 ppm.
(2) 4 correction pulses in OFFM = 1 correspond to -8.138 ppm.
(3) Reachable accuracy zone.

Oscillator register (13h)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
13h	Oscillator	-	OFFM	-	-				

Address	Register	Primary IIC		2nd IIC		Note
control bit XCLK		XCLK=1	XCLK=0 (default)	XCLK=1	XCLK=0 (default)	Only primary IIC controller can write “XCLK” bit
13h	Oscillator Register	Read/Write	Read only	Read only	Read/Write	For clock calibration The primary IIC can change the access capability)

Bit	Symbol	Value	Description
D6	OFFM	0 (default)	normal mode: correction is made every 4 hours
		1	fast mode: correction is made once every 8 minutes

Access register (14h)

Only primary IIC controller can write this Access register.

XCLK is the control bit to determine CLKOUT control (0Ch), Offset (12h),oscillator (13h) registers read/write capability by the two IIC buses.

Address	Register	D7	D6-D0
14h	Access	XCLK	reserved

Address	Register	Primary IIC	2nd IIC
14h	Access	Read/Write	Read only

Bit	Symbol	Value	Description
D7	XCLK	0 (default)	The second IIC interface control the clock out calibration capability. Register 0Ch, 12h,13h
		1	The primary IIC interface control the clock out calibration capability. Register 0Ch, 12h,13h
D6-D0	rsvd	-	reserved

XCLK	Register	Primary IIC	Secondary IIC	description
0 (default)	CLKOUT Control (0Ch) Offset (12h) Oscillator(13h)	Read only	Read/write	The second IIC controls the clock calibration.
1	CLKOUT Control (0Ch) Offset (12h) Oscillator(13h)	Read/write	Read only	The primary IIC controls the clock calibration.

Timestamp registers (15h to 1Bh)

The timestamp is to record the time for the RTC time register write-event for advanced time accuracy offset register setting. The timestamp registers are from 15h to 1Bh.

The timestamp will not record the time for Alarm registers (01h, 03h and 05h) write-event.

Address	Register	BCD Data Mode									Binary Mode	Default
		D7	D6	D5	D4	D3	D2	D1	D0	Range	Range	
15h	Sec_timestp	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
16h	Min_timestp	0	x10 mins			x1 Minutes				00-59	00-3B	00h
17h	Hour_timestp (12 Hour Mode)	PM/ AM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hour_timestp (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
18h	DayWk_timestp (Sunday =1)	Day of Week								1-7	01-07	07h
19h	DayMon_timestp	Day of Month								1-31	01-1F	01h
1Ah	Mon_timestp	Month								1-12	01-0C	01h
1Bh	Year_timestp	Year								0-99	00-63	00h

R code registers (1Ch to 1Dh)

The R code registers are two-byte random numbers and read only for security application. It takes 200 µs max to generate the R code after a timestamp event.

Battery switch-over function

RS4TC85053ZK has the feature of battery switch-over. The internal power input will switch to battery operation when V_{DD} is less than 1.5 V typ.

When switched to battery, the V_{DD} power domain is disabled. This means that IIC pins are ignored, CLK output is disabled and Hi-Z.

128 byte SRAM (device address 1010 111)

There is a 128 byte SRAM available from address 00h to 7Fh. The SRAM can be written and read when powered from V_{DD}. The SRAM content is backed-up when the device is powered from V_{BAT}, but cannot be accessed as the interface is disabled.

The address pointer is set during interface initiation and will auto increment after each byte access. The pointer will wrap around from address 7Fh to 00h after the last byte is accessed

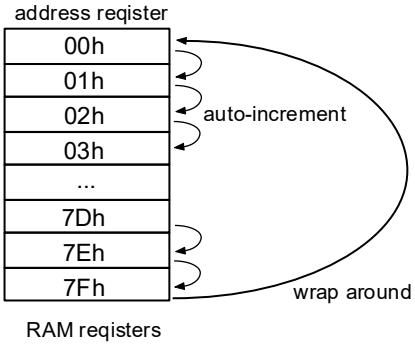


Figure9 SRAM register incrementing

The SRAM read/write capability is determined by the MWO bit and can be reset by RTC_CLR

Address	Register name	Reset By	Default	Note
00h-7Fh	SRAM Byte	RTC_CLR	00h	128 bytes of battery backup SRAM

Address	Register	Primary IIC		2nd IIC		Note
control bit MWO		MWO=1	MWO=0 (default)	MWO=1	MWO=0 (default)	Only primary IIC controller can write “MWO” bit. This bit is in RTC 2nd control register.
00h-7Fh	SRAM Byte	Read/Write	Read only	Read only	Read/Write	

IIC-bus interface

The IIC-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signal

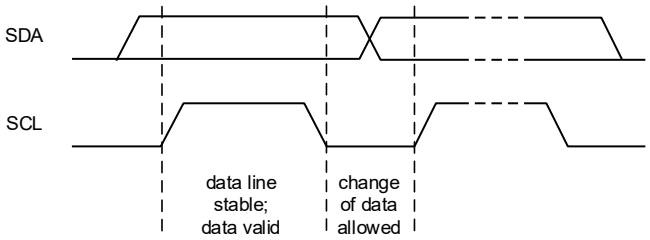


Figure10 Bit transfer

START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition – P

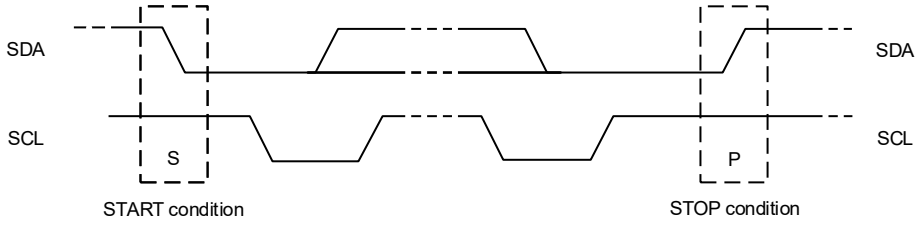


Figure11 Definition of START and STOP conditions

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A target receiver, which is addressed, must generate an acknowledge after the reception of each byte
- Also a controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition

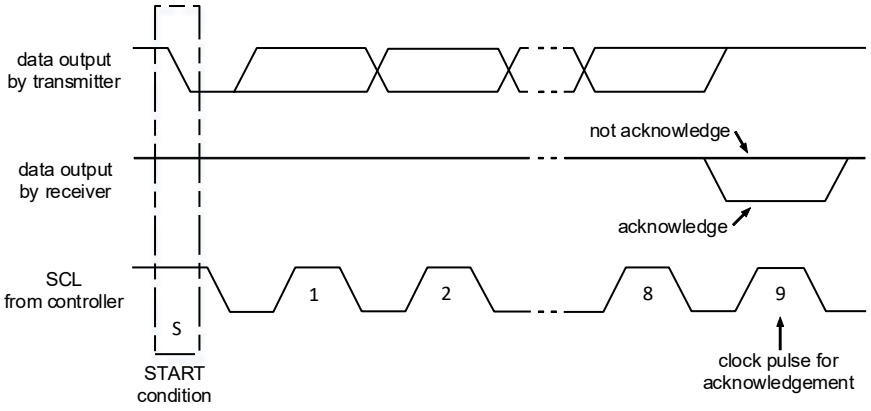


Figure12 Acknowledgement on the IIC bus

IIC-bus protocol

After a start condition, a valid hardware address has to be sent to a IIC device. The appropriate IIC-bus target addresses for RTC and SRAM

Register	D7	D6	D5	D4	D3	D2	D1	D0(R/W)	HEX
RTC	1	1	0	1	1	1	1	0:Write 1:Read	DEh :Write DFh: Read
SRAM	1	0	1	0	1	1	1	0:Write 1:Read	AEh :Write AFh: Read

The R/W bit defines the direction of the following single or multiple byte data transfer (read is logic 1, write is logic 0).

Write protocol

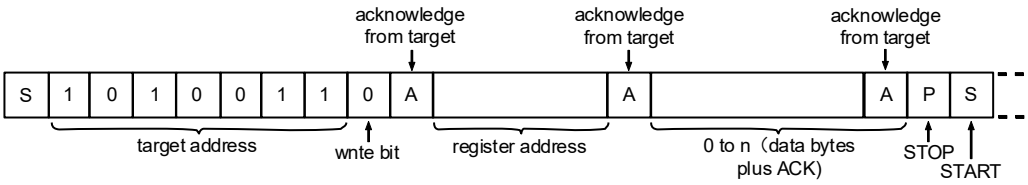


Figure13 Bus protocol ,writing to registers

Read protocol

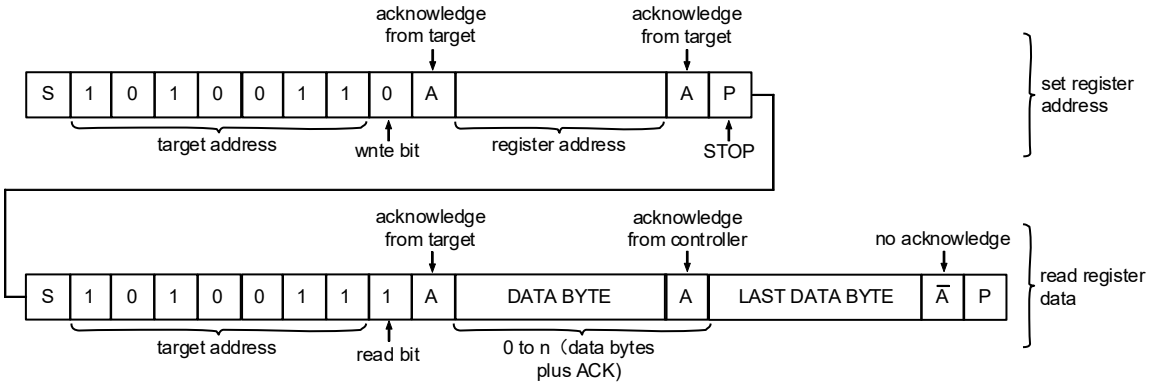


Figure14 Bus protocol ,reading to registers

I²C-bus timeout

If the SCL line is held LOW for longer than t_{to} (25 ms minimum; 35 ms maximum), the device resets to the idle state and waits for a new START condition. This ensures that the device never hangs up the bus if there are conflicts in the transmission sequence.

Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+5.5	V
V_{BAT}	battery supply voltage		-0.5	+5.5	V
V_I	input voltage	SCL, SDA, OSCI, RTC_CLR	-0.5	+5.5	V
V_O	output voltage		-0.5	+5.5	V
P_{tot}	total power dissipation		-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM		±5000	V
		CDM		±1000	V
I_{lu}	latch-up current	JESD78: $-0.5 \times V_{DD} < V_I < 1.5$	-100	+100	mA
T_{stg}	storage temperature		-65	+150	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Supplies						
V_{DD}	supply voltage	interface active; f_{SCL} = 400 kHz	1.7	-	3.6	V
V_{BAT}	battery supply voltage		1.55	-	3.6	V
I_{DD}	supply current	CLKOUT disabled; V_{DD} = 3.3 V; f_{SCL} = 0 Hz				
		T_{amb}= 25 °C	-	2	5	µA
		T_{amb}= -40 ℃ to +85 °C	-	5	10	µA
		CLKOUT disabled; V_{DD} = 3.3 V; f_{SCL} = 400 kHz		12		µA
		V_{DD} = 3.3 V, T_{amb}= 25 °C f_{SCL} = 400 kHz and all features are active.	-	-	1	mA
I_{BAT}	battery supply current	V_{DD} = 0 V VBAT = 3.3V				
		T_{amb}= 25 °C	-	400	1,050	nA
		T_{amb}= -40 ℃ to +85 °C	-	500	1,200	nA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Reference voltage						
Vth	threshold voltage of V_{DD} switch- over to Vbat	falling V_{DD}	1.1	1.4	1.6	V
		rising V_{DD}	1.25	1.55	1.6	V
		reference voltage hysteresis	-	±50	-	mV
Inputs						
V_I	input voltage		-0.5	-	+3.6	V
V_{IL}	LOW-level input voltage			-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-		V
I_{LI}	input leakage current	V_I = V_{SS} or V_{DD}	-	0	-	μA
		post ESD event	-0.5	-	+0.5	μA
V_{IL_CLR}	LOW-level input voltage of RTC_CLR		-0.3		+0.5	V
V_{IH_CLR}	HIGH-level input voltage of RTC_CLR		1.2		+3.6	V
t_{RTC_CLR}	RTC_CLR Minimum Assertion Windows		32			μs
Outputs						
V_{OH}	HIGH-level output voltage	on pin CLKOUT	0.8 V_{DD}	-	V_{DD}	V
V_{OL}	LOW-level ouput voltage	on pins SDA, ALRT, CLKOUT	0	-	0.2 V_{DD}	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 2.9 V; V_{DD} = 3.3 V; on pin CLKOUT	1	3		mA
I_{OL}	LOW-level output current	output sink current; V0l = 0.4 V; V_{DD} =3.3 V				
		on pin SDA, ALRT	3	8.5	-	mA
		on pin CLKOUT	1	3	-	mA
Oscillator						
Δf / f	Frequency stability	Ta= 25℃	-5	-	5	ppm

I2C AC Characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of VSS to VDD .These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Conditions	Fast Mode		Unit
			Min	Max	
Pin SCL					
f_{SCL}	SCL clock frequency,	[1]	1	400	kHz
t_{LOW}	LOW period of the SCL clock	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	-	0.6	-	µs
t_{to}	SMBus SCL time-out time	-	25	35	ms
Pin SDA					
$t_{SU;DAT}$	data set-up time	-	100	-	ns
$t_{HD;DAT}$	data hold time	-	0	-	ns
Pins SCL and SDA					
t_{BUF}	bus free time between a STOP and START condition	-	1.3	-	µs
$t_{SU;STO}$	set-up time for STOP condition	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals	[2] [3]	20 + 0.1Cb	300	ns
t_f	fall time of both SDA and SCL signals	[2] [3]	20 + 0.1Cb	300	ns
C_b	capacitive load for each bus line	-	-	400	pF
$t_{VD;ACK}$	data valid acknowledge time	[4]	-	0.9	µs
$t_{VD;DAT}$	data valid time	[5]	-	0.9	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.

[2] A controller device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the VIL of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[3] The maximum tf for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, tf is 250 ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin and the SDA/SCL bus lines without exceeding the maximum tf.

[4] tVD;ACK = time for acknowledgement signal from SCL LOW to SDA output LOW.

[5] tVD;DAT = minimum time for valid SDA output following SCL LOW.

[6] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

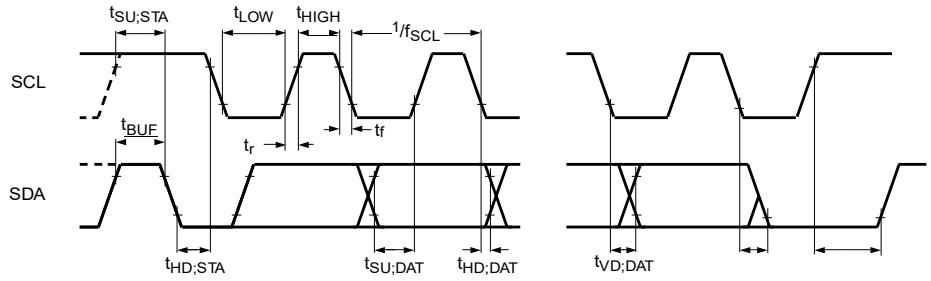
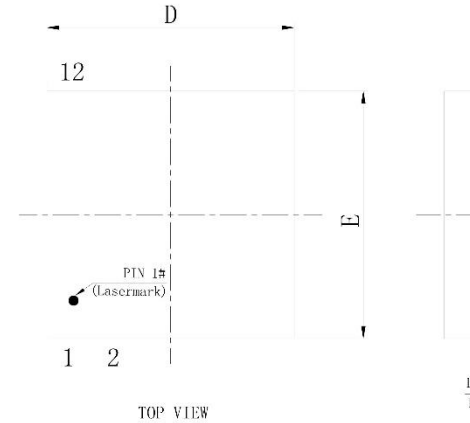
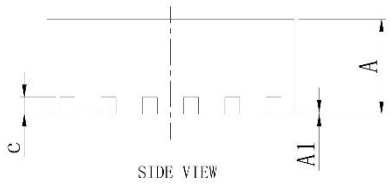
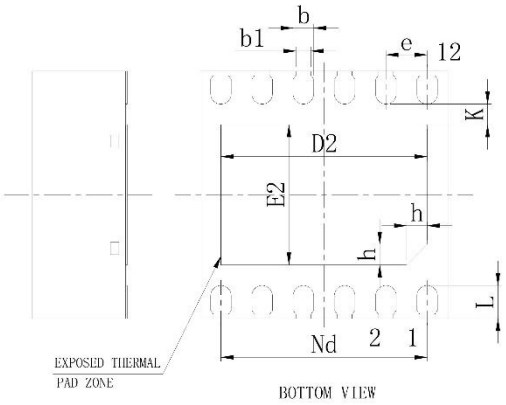


Figure 15. I^2C-bus timing diagram; rise and fall times refer to 30 % and 70 %

Package Information







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.10	1.15	1.20
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e		0.50BSC	
Nd		2.50BSC	
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
L	0.35	0.40	0.45
h	0.20	0.25	0.30
K		0.26REF	

Notes:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220.

DFN3X3X1.15 12L(ZK12) P0D

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary Release	2026/1/15
1.0	Initial Release	2026/6/18