RS7LSB102

Bi-directional Level Translator for
Open-drain and Push-Pull Applications

Features

- No Direction-Control
- Max Data Rates
  100 Mbps (Push-Pull)
- 1.1V to 5.5V on A ports and 1.1V to 5.5V on B Ports (VCCA≤VCCB)
- VCC Isolation: If Either VCC is at GND, Both Ports are in the High-Impedance State
- No Power-Supply Sequencing Required: VCCA or VCCB can be Ramped First
- Ioff Supports Partial Power-Down-Mode Operation
- ESD protection exceeds 4000V HBM
- Extended Temperature: -40°C to +125°C

Application

- I2C/SMBus, MDIO, SPI Interface
- Low-Voltage ASIC Level Translation
- Cell phone, Tablet, PC
- Server, Telecommunication

Description

The RS7LSB102 is a 2-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, VCCA and VCCB respectively.

A port supporting operating voltages from 1.1V to 5.5V while it tracks the VCCA supply, and the B ports supporting operating voltages from 1.1V to 5.5V while it tracks the VCCB supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V, 1.8V, 2.5V, 3.3V and 5V voltage nodes

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Information

Part Number	Package	Description
RS7LSB102V	VSSOP8	2.0mmx2.3mm
RS7LSB102ZE	DFN-8	2.0mmx3.0mm

Block Diagram

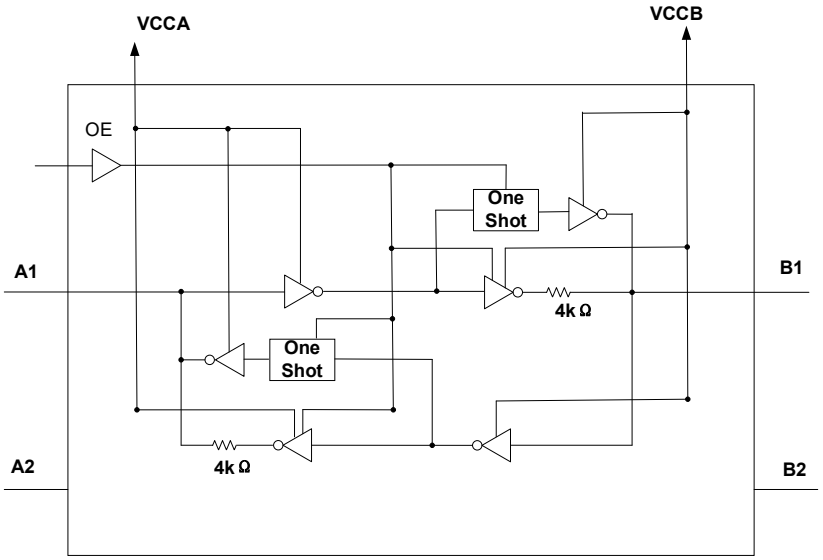
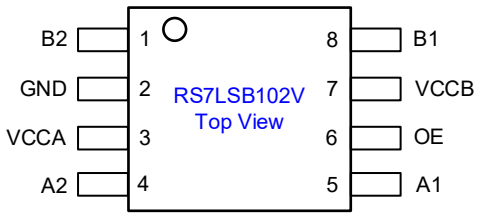


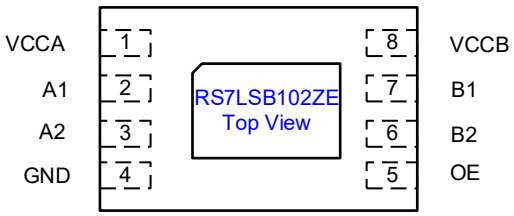
Figure 1: Block Diagram

Pin Configuration

VSSOP8 (Top view)



DFN-8 (Top view)



Pin Name	Pin No. VSSOP8	Pin No. DFN8	Type	Description
VCCA	3	1	Power	B-port supply voltage.1.1V ≤ VCCA ≤5.5V
A1	5	2	I/O	Input/output A. Referenced to VCCB
A2	4	3	I/O	Input/output A. Referenced to VCCB
GND	2	4	GND	Ground.
OE	6	5	Input	Output enables (active High). Pull OE low to place all outputs in 3-state mode.
B2	1	6	I/O	Input/output A. Referenced to VCCA
B1	8	**7**	I/O	Input/output A. Referenced to VCCA.
VCCB	7	8	Power	A-port supply voltage. 1.1V ≤ VCCB ≤5.5V

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
Tstore	Storage Temperature	−65	-	+150	°C
VCCA	DC Supply Voltage port B	-0.3	-	6.5	V
VCCB	DC Supply Voltage port A	-0.3	-	6.5	V
VIOB	Vi(A) referenced DC Input / Output Voltage	-0.3	-	6.5	V
VIOB	Vi(B) referenced DC Input / Output Voltage	-0.3	-	6.5	V
VOE	Enable Control Pin DC Input Voltage	-0.3	-	6.5	V
Ishort	Short circuit duration (I/O to GND)			50	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VCCA	VCCA Positive DC Supply Voltage	1.1	-	5.5	V
VCCB	VCCB Positive DC Supply Voltage	1.1	-	5.5	V
VOE	Enable Control Pin Voltage	GND	-	5.5	V
VIO	I/O Pin Voltage	GND	-	5.5	V
Δt /ΔV	Input transition rise or fall time	-	-	10	ns/V
TA	Operating Temperature Range	−40	-	+125	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 125°C, 1.1V≤V_{CCA}≤5.5V, 1.1V≤V_{CCB}≤5.5V

Symbol	Parameter	Test Conditions*1		MIN	TYP	MAX	Unit
VIHA	A port Input HIGH Voltage	1.1V≤VCCA ≤1.95		VCCA*0.75		VCCA	V
		1.95<VCCA ≤5.5V		VCCA*0.65		VCCA	V
VILA	A port Input LOW Voltage	1.1V≤VCCA ≤1.95		-	-	VCCA*0.25	V
		1.95<VCCA ≤5.5V		-	-	VCCA*0.35	V
VIHB	B port Input HIGH Voltage	1.1V≤VCCA ≤1.95		VCCB*0.75		VCCA	V
		1.95<VCCA ≤5.5V		VCCB*0.65		VCCB	V
VILB	B port Input LOW Voltage	1.1V≤VCCA ≤1.95		-	-	VCCB*0.25	V
		1.95<VCCA ≤5.5V		-	-	VCCB*0.35	V
VIH(EN)	Control Pin Input HIGH Voltage	1.1V≤VCCA ≤1.95		VCCA*0.75		VCCA	V
		1.95<VCCA ≤5.5V		VCCA*0.65		VCCA	V
VIL(EN)	Control Pin Input LOW Voltage	1.1V≤VCCA ≤1.95		-	-	VCCA*0.25	V
		1.95<VCCA ≤5.5V		-	-	VCCA*0.35	V
VOHA	A port Output HIGH Voltage	IOH = –20 μA 1.1V≤VCCA≤5.5V		VCCA-0.4	-	-	V
VOLA	A port Output LOW Voltage	IOH = 20μA 1.1V≤VCCA≤5.5V		-	-	0.4	V
VOHB	B port Output HIGH Voltage	IOH = –20 μA 1.1V≤VCCB≤5.5V		VCCB-0.4	-	-	V
VOLB	B port Output LOW Voltage	IOH = 20 μA 1.1V≤VCCB≤1.65V		-	-	0.4	V
ICCA	VCCA Supply Current	EN=High	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V	-		3	μA
			VCCA= 5.5V, VCCB= 0V	-	-	3	μA
			VCCA= 0V, VCCB=5.5V	-		-2	μA
ICCB	VCCB Supply Current	EN=High	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V	-		3	μA
			VCCA= 5.5V, VCCB= 0V	-		-2	μA
			VCCA= 0V, VCCB=5.5V	-		3	μA
ICCA+ICCB	Combined supply current	EN=High	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V			6	μA
ICCZA	Static supply current VCCA	EN=Low	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V			3	μA
ICCZB	Static supply current VCCB					3	μA
I_{OZ}	I/O Tri−state Output Mode Leakage Current	A or B port EN=Low	VCCA=1.1V to 5.5V, VCCB=1.1V to 5.5V			±2	μA
IOFF	Partial power down current	A port	VCCA=0V, VCCB=0V to 5.5V			±5	μA
		B port	VCCA=0V to 5.5V VCCB=0V			±5	μA
II-EN	Control pin leakage Current	VI = VCCI or GND		-	-	±2	μA

Note:

1. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design. Typical values are for V_{CCB} = +5 V, V_{CCA} = +3.3 V and T_A = +25°C.

AC Electrical characteristics

Timing Characteristics
(C_{LOAD} = 15pF, driver output impedance ≤ 50Ω, R_{LOAD} = 1 MΩ, T_A = -40°C to 125°C)

V_{CCA}= 1.2V±0.1V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 1.8V		VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		12		10		10		10	ns
tPLH_AB	Propagation Delay A → B	Push-pull		20		15		15		15	ns
tPHL_BA	Propagation Delay B → A	Push-pull		12		10		10		10	ns
tPLH_BA	Propagation Delay B → A	Push-pull		20		15		15		15	ns
tEN	Enable Time	EN to A or B		200		200		200		200	ns
tDIS	Disable Time	EN to A or B		250		250		250		250	ns
tRA	A port Rise Time	Push-pull		30		30		30		30	ns
tRB	B port Rise Time	Push-pull		30		30		30		30	ns
tFA	A port Fall Time	Push-pull		20		20		25		25	ns
tFB	B port Fall Time	Push-pull		20		20		25		25	ns
tSKEW	Channel to Channel Skew			1		1		1		1	1
MDR	Maximum Data Rate	Push-pull		20		20		20		20	Mbps

V_{CCA}= 1.8V±0.15V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		10		9		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		11		11	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		14		12		12	ns
tEN	Enable Time	EN to A or B		200		200		200	ns
tDIS	Disable Time	EN to A or B		250		250		250	ns
tRA	A port Rise Time	Push-pull		30		30		30	ns
tRB	B port Rise Time	Push-pull		30		30		30	ns
tFA	A port Fall Time	Push-pull		20		25		25	ns
tFB	B port Fall Time	Push-pull		25		30		30	ns
tSKEW	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull		52		60		60	Mbps

V_{CCA}= 2.5V±0.2V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		10		9		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		10		10	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		14		12		12	ns
tEN	Enable Time	EN to A or B		200		200		200	ns
tDIS	Disable Time	EN to A or B		250		250		250	ns
tRA	A port Rise Time	Push-pull		30		30		30	ns
tRB	B port Rise Time	Push-pull		30		30		30	ns
tFA	A port Fall Time	Push-pull		20		30		30	ns
tFB	B port Fall Time	Push-pull		25		25		25	ns
tSKEW	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull		70		100		100	Mbps

V_{CCA}= 3.3V±0.3V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		9		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		12	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		11		10	ns
tEN	Enable Time	EN to A or B		200		200	ns
t_{DIS}	Disable Time	EN to A or B		250		250	ns
t_{RA}	A port Rise Time	Push-pull		30		30	ns
t_{RB}	B port Rise Time	Push-pull		30		30	ns
tFA	A port Fall Time	Push-pull		25		25	ns
t_{FB}	B port Fall Time	Push-pull		25		25	ns
tSKEW	Channel to Channel Skew			1		1	ns
MDR	Maximum Data Rate	Push-pull		100		100	Mbps

V_{CCA}= 5V±0.5V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 5V		Unit
			MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		10	ns
tEN	Enable Time	EN to A or B		200	ns
t_{DIS}	Disable Time	EN to A or B		250	ns
tRA	A port Rise Time	Push-pull		30	ns
t_{RB}	B port Rise Time	Push-pull		30	ns
tFA	A port Fall Time	Push-pull		25	ns
t_{FB}	B port Fall Time	Push-pull		25	ns
tSKEW	Channel to Channel Skew			1	ns
MDR	Maximum Data Rate	Push-pull		100	Mbps

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Test Circuits

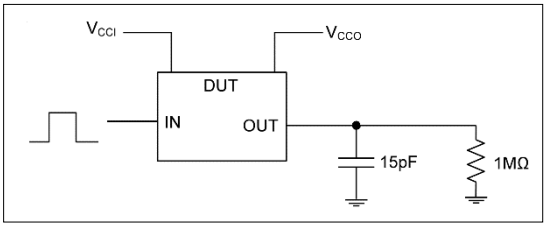


Figure 2 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

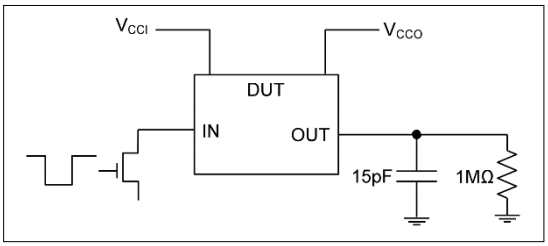
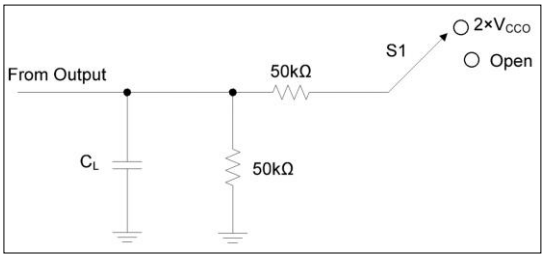


Figure 3 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} ,t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} ,t_{PZH} (t_{en})	Open

Figure 4 Load Circuit for Enable-Time and Disable-Time Measurement

Notes:

1. CL includes probe and jig capacitance.
2. t_{en} is the same as t_{PZL} and t_{PZH}. t_{dis} is the same as t_{PLZ} and t_{PHZ}.
3. V_{CCI} is the supply voltage associated with the input.
4. V_{CCO} is the supply voltage associated with the output.

Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

PRR ≤10 MHz
Z_O = 50 Ω
dv/dt ≥1 V/ns

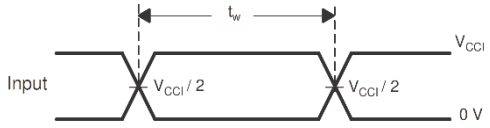


Figure 5 Pulse Duration

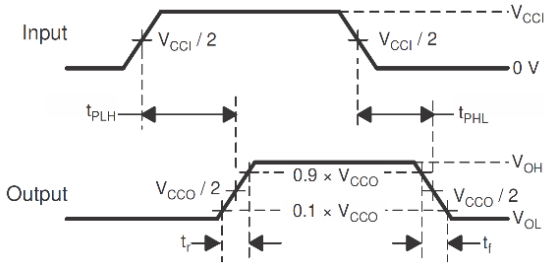


Figure 6 Propagation Delay Times

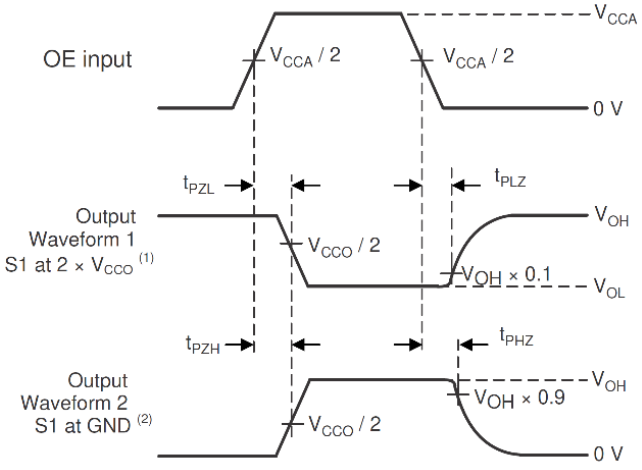


Figure 7 Enable and Disable Times

1. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
2. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Functional Description

The RS7LSB102 device is a 2-bit bidirectional voltage level converter specifically designed for converting logic voltage levels. This device is of a buffer architecture, which features an edge rate accelerator (monostable) to enhance the overall data rate. This device can only convert push-pull CMOS logic outputs.

The RS7LSB102 architecture (see fig8) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the RS7LSB102 can maintain a high or low, but are designed to be weak, so that they can be over driven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low- to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition.

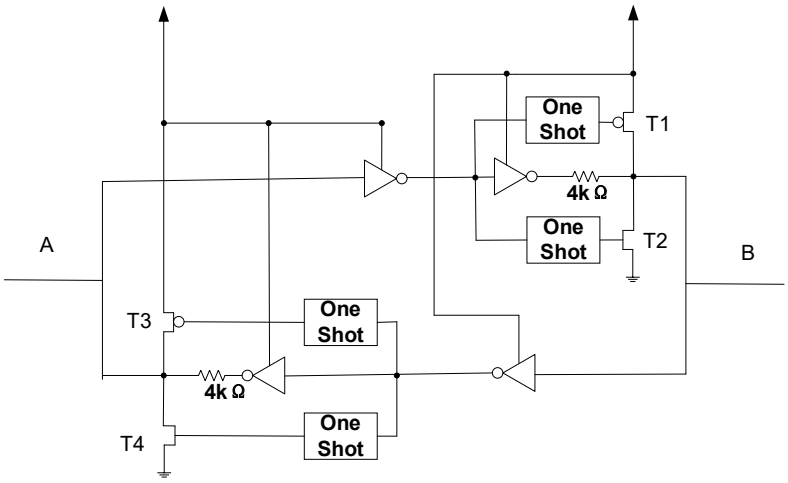
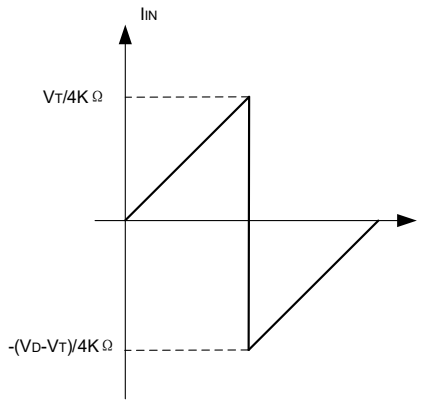


Figure 8 Level Shifter Architecture

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the RS7LSB102 are shown in fig9. For proper operation, the device driving the data I/Os of the RS7LSB102 must have drive strength of at least ±2 mA.



(1) V_T is the input threshold voltage of the RS7LSB102 (typical VCCI/2).

(2) VD is the supply voltage of the external driver.

Power Up

There is no requirement for the power sequence. During operation, RS7LSB102 can work at both $V_{CCA} \leq V_{CCB}$ During power-up sequencing, any power supply can be ramped up first. The RS7LSB102 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

Enable and Disable

The RS7LSB102 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistor on I/O Lines

The RS7LSB102 is designed to drive capacitive loads of up to 70 pF. The output drivers of the RS7LSB102 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the RS7LSB102.
For the same reason, the RS7LSB102 should not be used in applications such as I2C or 1-Wire where an open drain driver is connected on the bidirectional data I/O. For these applications, use a device from the RS7LSXXX series of level translators.

Application Information

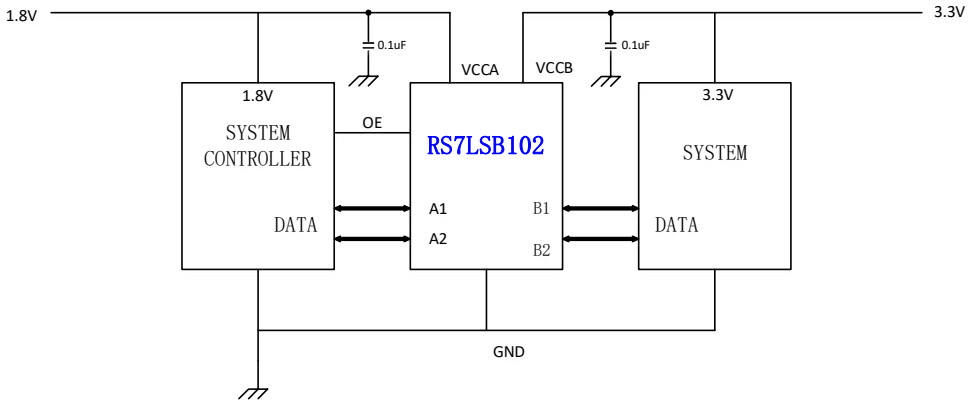


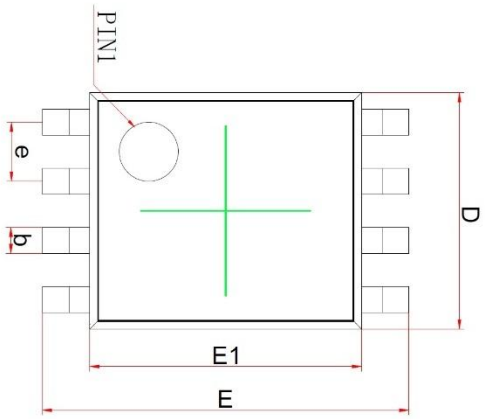
Figure 10 Application Circuit

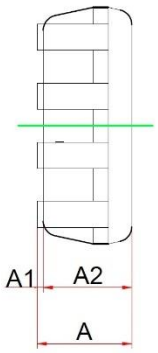
Power Supply Guidelines

Suggests conducting a meticulous PCB layout with shorter PCB wiring lengths to avoid excessive capacitive loads and ensure correct OS triggering. The PCB signal wiring length must be kept sufficiently short so that any reflected round-trip delay is less than the monostable duration. This ensures that any reflections encounter low impedance at the driver, thereby improving signal integrity. The OS circuit is designed to maintain a duration of approximately 10 ns. The maximum capacitance of the lumped load to be driven also directly depends on the monostable duration. For heavy capacitive loads, the monostable may time out before the signal is fully driven to the positive power rail. The OS duration has been set to achieve a better balance among considerations such as dynamic ICC, load driving capability, and maximum bit rate. The PCB wiring length and connectors have increased the capacitance of the RS7LSB102 output, so Raystar suggests considering this lumped load capacitance to avoid OS re-triggering, bus contention, output signal oscillation, or other adverse system-level effects.

Package Information

VSSOP8





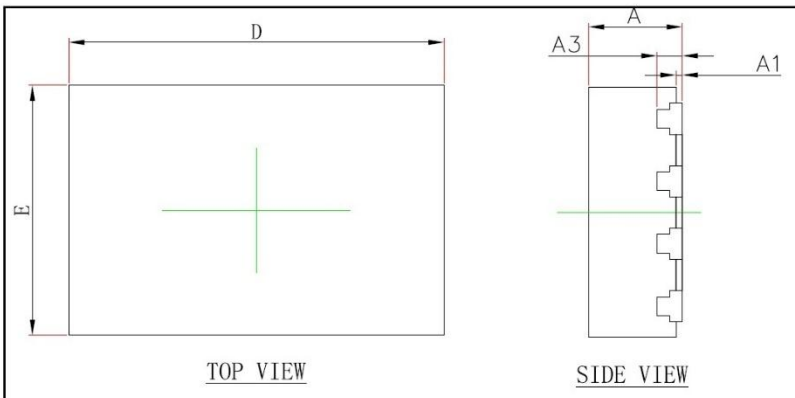
Symbol	Dimensions In Millimeters		
	Min.	Nor.	Max.
A	--	--	1.000
A1	0.000	--	0.150
A2	0.600	0.750	0.850
A3	0.190	0.200	0.210
b	0.170	0.220	0.270
c	0.080	--	0.230
D	1.900	2.000	2.100
E	3.000	3.100	3.200
E1	2.200	2.300	2.400
e	0.500BSC		
L	0.150	--	0.400
L1	0.400REF.		
θ	0°	--	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

VSSOP08 (V08) Rev.0
Raystar Microelectronics Technology Inc.

Package Information

TDFN-8L



Symbol	Dimensions In Millineters	
	Min	Max
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF.	
D	2.900	3.100
E	1.900	2.100
D1	1.400	1.600
E1	1.400	1.600
b	0.180	0.280
e	0.500BSC.	
k	0.450REF.	
L	0.250	0.350

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TDFN 2X3-8L(ZE08) POD Rev.0
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary	2026/3/2
1.0	Initial Release	2026/4/17