



Features

- No Direction-Control
- Max Data Rates
100 Mbps (Push-Pull)
- 1.1V to 5.5V on A ports and 1.1V to 5.5V on B
Ports ($V_{CCA} \leq V_{CCB}$)
- VCC Isolation: If Either VCC is at GND, Both
Ports are in the High-Impedance State
- No Power-Supply Sequencing Required: VCCA
or VCCB can be Ramped First
- Ioff Supports Partial Power-Down-Mode
Operation
- ESD protection exceeds 4000V HBM
- Extended Temperature: -40°C to +125°C

Application

- I2C/SMBus, MDIO, SPI Interface
- Low-Voltage ASIC Level Translation
- Cell phone, Tablet, PC
- Server, Telecommunication

Description

The RS7LSB106 is a 6-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, VCCA and VCCB respectively.

A port supporting operating voltages from 1.1V to 5.5V while it tracks the VCCA supply, and the B ports supporting operating voltages from 1.1V to 5.5V while it tracks the VCCB supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V, 1.8V, 2.5V, 3.3V and 5V voltage nodes

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Information

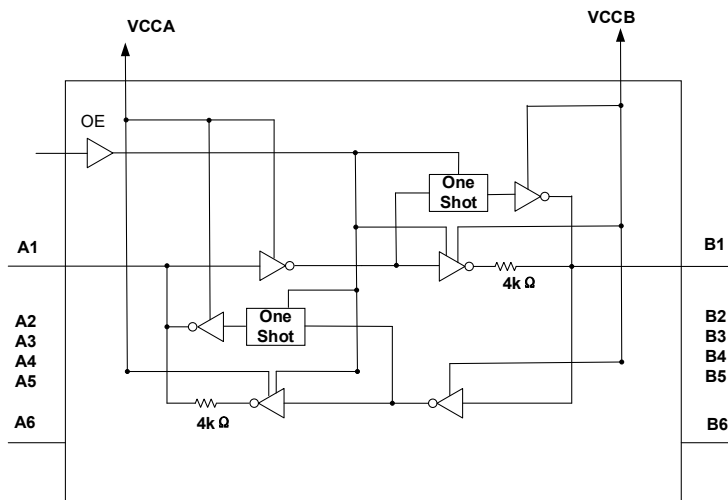
Part Number	Package	Description
RS7LSB106L	TSSOP16	5 x 4.4 mm

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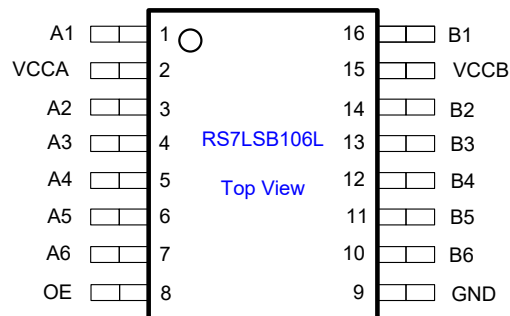
RS7LSB106Bi-directional Level Translator for
Open-drain and Push-Pull Applications

Block Diagram

**Figure 1: Block Diagram**

Pin Configuration

TSSOP16 (Top view)



Pin Name	TSSOP-16	Type	Description
A1	1	I/O	Input/output 1. Referenced to VCCA
A2	3	I/O	Input/output 2. Referenced to VCCA
A3	4	I/O	Input/output 3. Referenced to VCCA
A4	5	I/O	Input/output 4. Referenced to VCCA
A5	6	I/O	Input/output 5. Referenced to VCCA
A6	7	I/O	Input/output 6. Referenced to VCCA
B1	16	I/O	Input/output 1. Referenced to VCCB
B2	14	I/O	Input/output 2. Referenced to VCCB
B3	13	I/O	Input/output 3. Referenced to VCCB
B4	12	I/O	Input/output 4. Referenced to VCCB
B5	11	I/O	Input/output 5. Referenced to VCCB
B6	10	I/O	Input/output 6. Referenced to VCCB
GND	9	—	Ground
OE	8	Input	Tri-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to VCCA.
VCCA	2	Power	A-port supply voltage. $1.1\text{ V} \leq VCCA \leq 5.5\text{ V}$, $VCCA \leq VCCB$.
VCCB	15	Power	B-port supply voltage. $1.1\text{ V} \leq VCCB \leq 5.5\text{ V}$.



Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
Tstore	Storage Temperature	-65	-	+150	°C
VCCA	DC Supply Voltage port B	-0.3	-	6.5	V
VCCB	DC Supply Voltage port A	-0.3	-	6.5	V
VIOB	Vi(A) referenced DC Input / Output Voltage	-0.3	-	6.5	V
VIOB	Vi(B) referenced DC Input / Output Voltage	-0.3	-	6.5	V
VOE	Enable Control Pin DC Input Voltage	-0.3	-	6.5	V
Ishort	Short circuit duration (I/O to GND)			50	mA

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VCCA	VCCA Positive DC Supply Voltage	1.1	-	5.5	V
VCCB	VCCB Positive DC Supply Voltage	1.1	-	5.5	V
VOE	Enable Control Pin Voltage	GND	-	5.5	V
VIO	I/O Pin Voltage	GND	-	5.5	V
$\Delta t / \Delta V$	Input transition rise or fall time	-	-	10	ns/V
TA	Operating Temperature Range	-40	-	+125	°C

**DC Electrical Characteristics**Unless otherwise specified, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $1.1\text{V} \leq V_{CCA} \leq 5.5\text{V}$, $1.1\text{V} \leq V_{CCB} \leq 5.5\text{V}$

Symbol	Parameter	Test Conditions*1		MIN	TYP	MAX	Unit
VIHA	A port Input HIGH Voltage	$1.1\text{V} \leq V_{CCA} \leq 1.95$		$V_{CCA} \times 0.75$		V_{CCA}	V
		$1.95 < V_{CCA} \leq 5.5\text{V}$		$V_{CCA} \times 0.65$		V_{CCA}	V
VILA	A port Input LOW Voltage	$1.1\text{V} \leq V_{CCA} \leq 1.95$		-	-	$V_{CCA} \times 0.25$	V
		$1.95 < V_{CCA} \leq 5.5\text{V}$		-	-	$V_{CCA} \times 0.35$	V
VIHB	B port Input HIGH Voltage	$1.1\text{V} \leq V_{CCA} \leq 1.95$		$V_{CCB} \times 0.75$		V_{CCA}	V
		$1.95 < V_{CCA} \leq 5.5\text{V}$		$V_{CCB} \times 0.65$		V_{CCB}	V
VILB	B port Input LOW Voltage	$1.1\text{V} \leq V_{CCA} \leq 1.95$		-	-	$V_{CCB} \times 0.25$	V
		$1.95 < V_{CCA} \leq 5.5\text{V}$		-	-	$V_{CCB} \times 0.35$	V
VIH(EN)	Control Pin Input HIGH Voltage	$1.1\text{V} \leq V_{CCA} \leq 1.95$		$V_{CCA} \times 0.75$		V_{CCA}	V
		$1.95 < V_{CCA} \leq 5.5\text{V}$		$V_{CCA} \times 0.65$		V_{CCA}	V
VIL(EN)	Control Pin Input LOW Voltage	$1.1\text{V} \leq V_{CCA} \leq 1.95$		-	-	$V_{CCA} \times 0.25$	V
		$1.95 < V_{CCA} \leq 5.5\text{V}$		-	-	$V_{CCA} \times 0.35$	V
VOHA	A port Output HIGH Voltage	$I_{OH} = -20\text{ }\mu\text{A}$ $1.1\text{V} \leq V_{CCA} \leq 5.5\text{V}$		$V_{CCA} - 0.4$	-	-	V
VOLA	A port Output LOW Voltage	$I_{OH} = 20\text{ }\mu\text{A}$ $1.1\text{V} \leq V_{CCA} \leq 5.5\text{V}$		-	-	0.4	V
VOHB	B port Output HIGH Voltage	$I_{OH} = -20\text{ }\mu\text{A}$ $1.1\text{V} \leq V_{CCB} \leq 5.5\text{V}$		$V_{CCB} - 0.4$	-	-	V
VOLB	B port Output LOW Voltage	$I_{OH} = 20\text{ }\mu\text{A}$ $1.1\text{V} \leq V_{CCB} \leq 1.65\text{V}$		-	-	0.4	V
ICCA	VCCA Supply Current	EN=High	$V_{CCA}=1.1\text{V to } 5.5\text{V},$ $V_{CCB}=1.1\text{V to } 5.5\text{V}$	-		12	μA
			$V_{CCA}= 5.5\text{V}, V_{CCB}= 0\text{V}$	-	-	12	μA
			$V_{CCA}= 0\text{V}, V_{CCB}=5.5\text{V}$	-		-2	μA
ICCB	VCCB Supply Current	EN=High	$V_{CCA}=1.1\text{V to } 5.5\text{V},$ $V_{CCB}=1.1\text{V to } 5.5\text{V}$	-		12	μA
			$V_{CCA}= 5.5\text{V}, V_{CCB}= 0\text{V}$	-		-2	μA
			$V_{CCA}= 0\text{V}, V_{CCB}=5.5\text{V}$	-		12	μA
ICCA+ICCB	Combined supply current	EN=High	$V_{CCA}=1.1\text{V to } 5.5\text{V},$ $V_{CCB}=1.1\text{V to } 5.5\text{V}$			24	μA
ICCZA	Static supply current VCCA	EN=Low	$V_{CCA}=1.1\text{V to } 5.5\text{V},$ $V_{CCB}=1.1\text{V to } 5.5\text{V}$			12	μA
ICCZB	Static supply current VCCB					12	μA
I_{OZ}	I/O Tri-state Output Mode Leakage Current	A or B port EN=Low	$V_{CCA}=1.1\text{V to } 5.5\text{V},$ $V_{CCB}=1.1\text{V to } 5.5\text{V}$			± 2	μA
IOFF	Partial power down current	A port	$V_{CCA}=0\text{V},$ $V_{CCB}=0\text{V to } 5.5\text{V}$			± 5	μA
		B port	$V_{CCA}=0\text{V to } 5.5\text{V}$ $V_{CCB}=0\text{V}$			± 5	μA
II-EN	Control pin leakage Current	$V_I = V_{CCI} \text{ or } \text{GND}$		-	-	± 2	μA

Note:

- All units are production tested at $T_A = +25^{\circ}\text{C}$. Limits over the operating temperature range are guaranteed by design. Typical values are for $V_{CCB} = +5\text{V}$, $V_{CCA} = +3.3\text{V}$ and $T_A = +25^{\circ}\text{C}$.



AC Electrical characteristics

Timing Characteristics

($C_{LOAD} = 15\text{pF}$, driver output impedance $\leq 50\Omega$, $R_{LOAD} = 1\text{M}\Omega$, $T_A = -40^\circ\text{C}$ to 125°C)

$V_{CCA} = 1.2\text{V} \pm 0.1\text{V}$

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 1.8V		VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A $\rightarrow$ B	Push-pull		12		10		10		10	ns
tPLH_AB	Propagation Delay A $\rightarrow$ B	Push-pull		20		15		15		15	ns
tPHL_BA	Propagation Delay B $\rightarrow$ A	Push-pull		12		10		10		10	ns
tPLH_BA	Propagation Delay B $\rightarrow$ A	Push-pull		20		15		15		15	ns
tEN	Enable Time	EN to A or B		200		200		200		200	ns
tDIS	Disable Time	EN to A or B		250		250		250		250	ns
tRA	A port Rise Time	Push-pull		30		30		30		30	ns
tRB	B port Rise Time	Push-pull		30		30		30		30	ns
tFA	A port Fall Time	Push-pull		20		20		25		25	ns
tFB	B port Fall Time	Push-pull		20		20		25		25	ns
tSKEW	Channel to Channel Skew			1		1		1		1	1
MDR	Maximum Data Rate	Push-pull		20		20		20		20	Mbps

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RS7LSB106Bi-directional Level Translator for
Open-drain and Push-Pull Applications **$V_{CCA} = 1.8V \pm 0.15V$**

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB = 2.5V		VCCB = 3.3V		VCCB = 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		10		9		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		11		11	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		14		12		12	ns
tEN	Enable Time	EN to A or B		200		200		200	ns
tDIS	Disable Time	EN to A or B		250		250		250	ns
tRA	A port Rise Time	Push-pull		30		30		30	ns
tRB	B port Rise Time	Push-pull		30		30		30	ns
tFA	A port Fall Time	Push-pull		20		25		25	ns
tFB	B port Fall Time	Push-pull		25		30		30	ns
tSKEW	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull		52		60		60	Mbps

 **$V_{CCA} = 2.5V \pm 0.2V$**

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 2.5V		VCCB = 3.3V		VCCB= 5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A $\rightarrow$ B	Push-pull		10		9		9	ns
tPLH_AB	Propagation Delay A $\rightarrow$ B	Push-pull		12		10		10	ns
tPHL_BA	Propagation Delay B $\rightarrow$ A	Push-pull		9		9		9	ns
tPLH_BA	Propagation Delay B $\rightarrow$ A	Push-pull		14		12		12	ns
tEN	Enable Time	EN to A or B		200		200		200	ns
tDIS	Disable Time	EN to A or B		250		250		250	ns
tRA	A port Rise Time	Push-pull		30		30		30	ns
tRB	B port Rise Time	Push-pull		30		30		30	ns
tFA	A port Fall Time	Push-pull		20		30		30	ns
tFB	B port Fall Time	Push-pull		25		25		25	ns
tSKEW	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull		70		100		100	Mbps

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RS7LSB106Bi-directional Level Translator for
Open-drain and Push-Pull Applications **$V_{CCA} = 3.3V \pm 0.3V$**

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB = 3.3V		VCCB = 5V		Unit
			MIN	MAX	MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		9		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12		12	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		11		10	ns
tEN	Enable Time	EN to A or B		200		200	ns
tDIS	Disable Time	EN to A or B		250		250	ns
tRA	A port Rise Time	Push-pull		30		30	ns
tRB	B port Rise Time	Push-pull		30		30	ns
tFA	A port Fall Time	Push-pull		25		25	ns
tFB	B port Fall Time	Push-pull		25		25	ns
tSKEW	Channel to Channel Skew			1		1	ns
MDR	Maximum Data Rate	Push-pull		100		100	Mbps

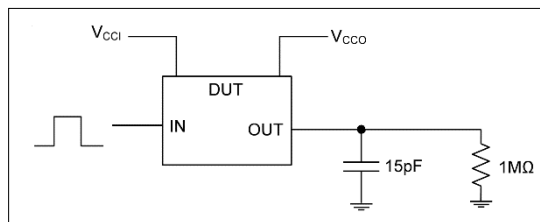
 **$V_{CCA} = 5V \pm 0.5V$**

Over recommended operating free-air temperature range (unless otherwise noted)

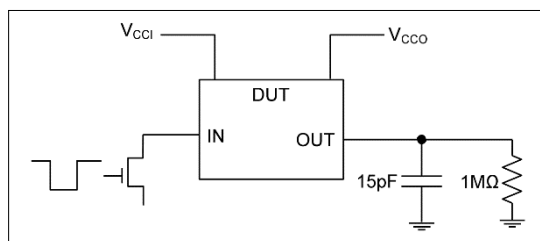
Symbol	Parameter	Test Conditions	VCCB= 5V		Unit
			MIN	MAX	
tPHL_AB	Propagation Delay A → B	Push-pull		9	ns
tPLH_AB	Propagation Delay A → B	Push-pull		12	ns
tPHL_BA	Propagation Delay B → A	Push-pull		9	ns
tPLH_BA	Propagation Delay B → A	Push-pull		10	ns
tEN	Enable Time	EN to A or B		200	ns
tDIS	Disable Time	EN to A or B		250	ns
tRA	A port Rise Time	Push-pull		30	ns
tRB	B port Rise Time	Push-pull		30	ns
tFA	A port Fall Time	Push-pull		25	ns
tFB	B port Fall Time	Push-pull		25	ns
tSKEW	Channel to Channel Skew			1	ns
MDR	Maximum Data Rate	Push-pull		100	Mbps



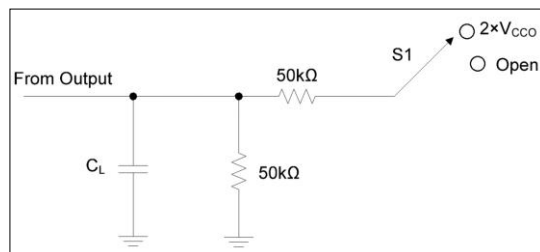
Test Circuits



**Figure 2 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement
Using a Push-Pull Driver**



**Figure 3 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement
Using an Open-Drain Driver**



TEST	S1
t_{PZL}, t_{PLZ} (t_{dis})	$2 \times V_{CCO}$
t_{PHZ}, t_{PZH} (t_{en})	Open

Figure 4 Load Circuit for Enable-Time and Disable-Time Measurement

Notes:

1. C_L includes probe and jig capacitance.
2. t_{en} is the same as t_{PZL} and t_{PZH} . t_{dis} is the same as t_{PLZ} and t_{PHZ} .
3. V_{CCI} is the supply voltage associated with the input.
4. V_{CCO} is the supply voltage associated with the output.



Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

PRR ≤ 10 MHz

$Z_O = 50\ \Omega$

$dv/dt \geq 1$ V/ns

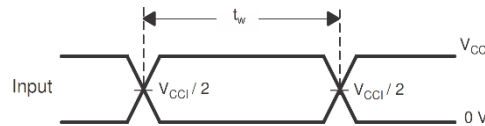


Figure 5 Pulse Duration

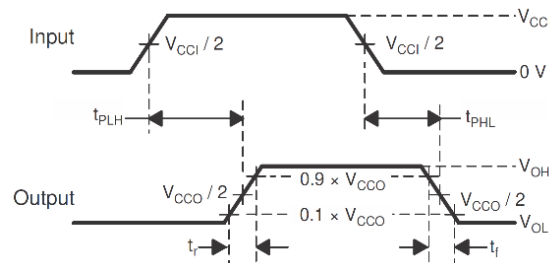


Figure 6 Propagation Delay Times

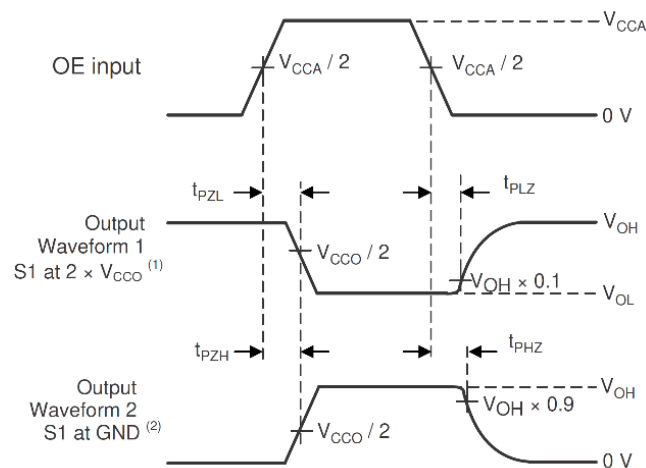


Figure 7 Enable and Disable Times

1. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
2. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.



Functional Description

The RS7LSB106 device is a 6-bit bidirectional voltage level converter specifically designed for converting logic voltage levels. This device is of a buffer architecture, which features an edge rate accelerator (monostable) to enhance the overall data rate. This device can only convert push-pull CMOS logic outputs.

The RS7LSB106 architecture (see fig8) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the RS7LSB106 can maintain a high or low, but are designed to be weak, so that they can be over driven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low- to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition.

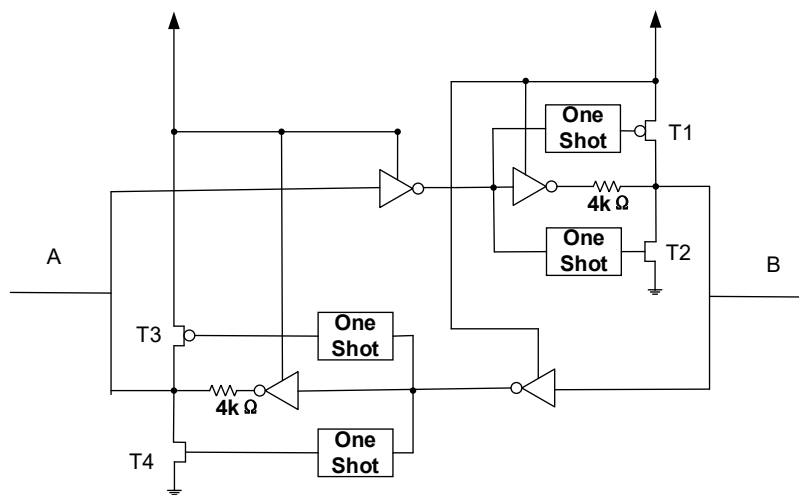
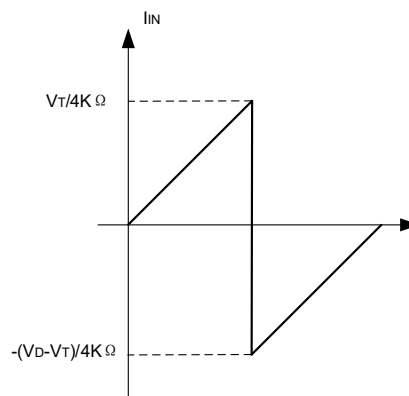


Figure 8 Level Shifter Architecture

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the RS7LSB106 are shown in fig9. For proper operation, the device driving the data I/Os of the RS7LSB106 must have drive strength of at least ± 2 mA.



- (1) V_T is the input threshold voltage of the RS7LSB106 (typical $V_{CCI}/2$).
- (2) V_D is the supply voltage of the external driver.

**Power Up**

There is no requirement for the power sequence. During operation, RS7LSB106 can work at both $V_{CCA} \leq V_{CCB}$. During power-up sequencing, any power supply can be ramped up first. The RS7LSB106 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0\text{ V}$).

Enable and Disable

The RS7LSB106 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistor on I/O Lines

The RS7LSB106 is designed to drive capacitive loads of up to 70 pF. The output drivers of the RS7LSB106 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k Ω to ensure that they do not contend with the output drivers of the RS7LSB106.

For the same reason, the RS7LSB106 should not be used in applications such as I2C or 1-Wire where an open drain driver is connected on the bidirectional data I/O. For these applications, use a device from the RS7LSXXX series of level translators.



Application Information

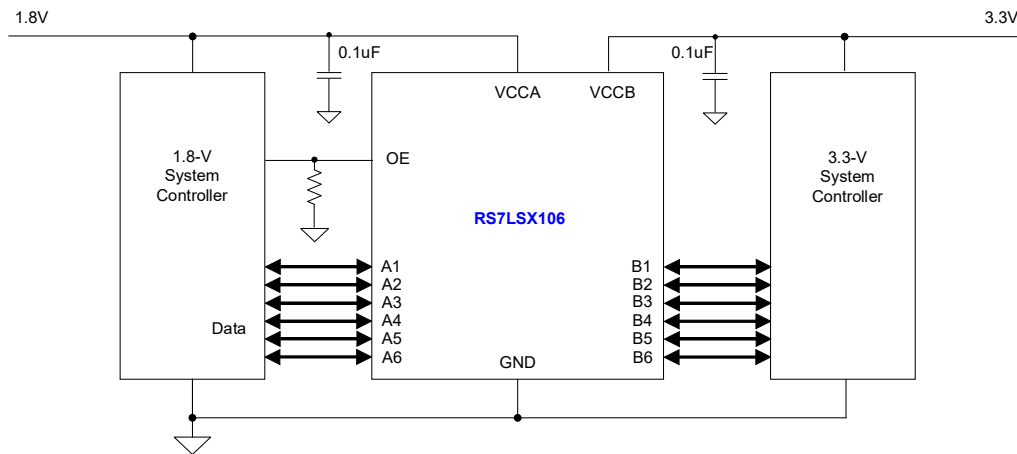


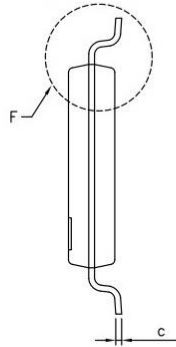
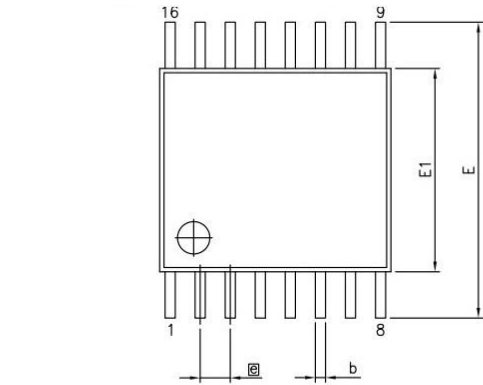
Figure 10 Application Circuit

Power Supply Guidelines

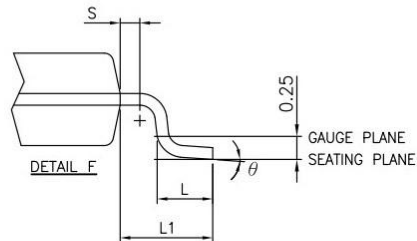
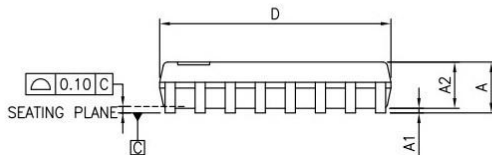
Suggests conducting a meticulous PCB layout with shorter PCB wiring lengths to avoid excessive capacitive loads and ensure correct OS triggering. The PCB signal wiring length must be kept sufficiently short so that any reflected round-trip delay is less than the monostable duration. This ensures that any reflections encounter low impedance at the driver, thereby improving signal integrity. The OS circuit is designed to maintain a duration of approximately 10 ns. The maximum capacitance of the lumped load to be driven also directly depends on the monostable duration. For heavy capacitive loads, the monostable may time out before the signal is fully driven to the positive power rail. The OS duration has been set to achieve a better balance among considerations such as dynamic ICC, load driving capability, and maximum bit rate. The PCB wiring length and connectors have increased the capacitance of the RS7LSB106 output, so Raystar suggests considering this lumped load capacitance to avoid OS re-triggering, bus contention, output signal oscillation, or other adverse system-level effects.

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RS7LSB106Bi-directional Level Translator for
Open-drain and Push-Pull Applications**Package Information****TSSOP16**

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°

**Note:**

- 1.All dimensions are in mm. Angles in degrees.
- 2.Dimensions exclude burrs, mold flash or protrusions.
- 3.Refer Jedec MS-012

**Raystar Microelectronics Technology Inc.**

TSSOP16 POD Rev.0

**RSM**

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RS7LSB106Bi-directional Level Translator for
Open-drain and Push-Pull Applications**Revision History**

Revision	Description	Date
0.9	Preliminary	2026/3/3
1.0	Initial Release	2026/4/17