



## Features

- PCIe 3.0 compliant
- PCIe 3.0 Phase Jitter -0.45 ps RMS
- LVDS compatible outputs
- Supply voltage of 3.3V  $\pm$ 10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 40ps cycle-to-cycle (typ)
- Spread of -0.5%, -1.0%, -1.5%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- QFN-20L 3x3x0.85mm package

## Application

- Cloud/High-performance Computing
- nVME Storage
- Network
- Accelerators

## Block Diagram

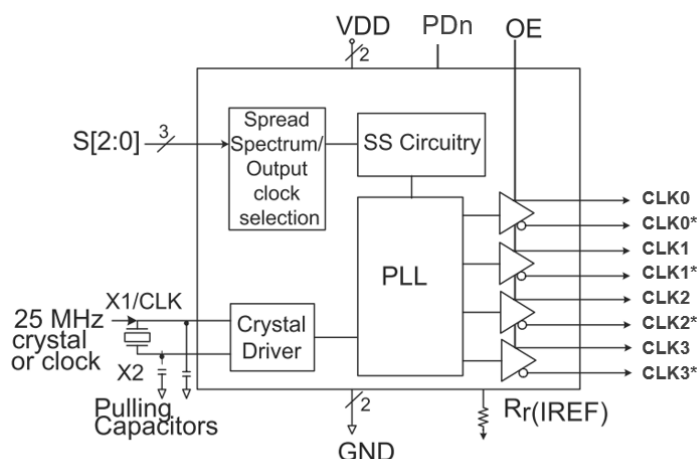


Figure 1 Block Diagram

## Description

The RS2CG5704B is a spread spectrum clock generator compliant to PCI Express 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

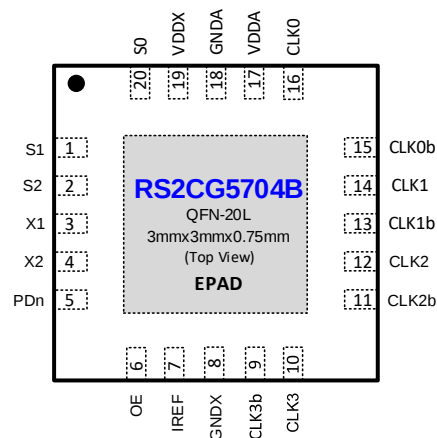
The RS2CG5704B provides four differential (HCSL) or LVDS spread spectrum outputs. The RS2CG5704B is configured to select spread and clock selection. Using Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces four pairs of differential outputs (HCSL) at 100MHz or 200MHz clock frequencies. It also provides spread selection of -0.5%, -1.0%, -1.5% and no spread.

## Ordering Information

| Part Number  | Package | Description               |
|--------------|---------|---------------------------|
| RS2CG5704BXC | QFN-20L | 3x3x0.85mm<br>Pitch=0.4mm |



## Pin Configuration



**Figure 2 Pin Configuration**

| Pin No. | Pin Name | I/O Type | Description                                                                                              |
|---------|----------|----------|----------------------------------------------------------------------------------------------------------|
| 1       | S1       | Input    | Spread Spectrum Select pin #1. Internal pull-up resistor.                                                |
| 2       | S2       | Input    | Spread Spectrum Select pin #2. Internal pull-up resistor.                                                |
| 3       | X1       | Input    | Crystal connection.                                                                                      |
| 4       | X2       | Output   | Crystal connection.                                                                                      |
| 5       | PDn      | Input    | Power down. Internal pull-up resistor.                                                                   |
| 6       | OE       | Input    | Output enable. Tri-states output (High=enable outputs); Low=disable outputs). Internal pull-up resistor. |
| 7       | IREF     | Output   | Precision resistor attached to this pin is connected to the internal current reference.                  |
| 8       | GNDX     | Power    | Connect to digital circuit ground.                                                                       |
| 9       | CLK3b    | Output   | Selectable 100/200 MHz Spread Spectrum differential complement output clock 3.                           |
| 10      | CLK3     | Output   | Selectable 100/200 MHz Spread Spectrum differential true output clock 3.                                 |
| 11      | CLK2b    | Output   | Selectable 100/200 MHz Spread Spectrum differential complement output clock 2.                           |
| 12      | CLK2     | Output   | Selectable 100/200 MHz Spread Spectrum differential true output clock 2.                                 |
| 13      | CLK1b    | Output   | Selectable 100/200 MHz Spread Spectrum differential complement output clock 1.                           |
| 14      | CLK1     | Output   | Selectable 100/200 MHz Spread Spectrum differential true output clock 1.                                 |
| 15      | CLK0b    | Output   | Selectable 100/200 MHz Spread Spectrum differential complement output clock 0.                           |
| 16      | CLK0     | Output   | Selectable 100/200 MHz Spread Spectrum differential true output clock 0.                                 |
| 17      | VDDA     | Power    | Connect to a +3.3V analog source.                                                                        |
| 18      | GNDA     | Power    | Output and Analog circuit ground                                                                         |
| 19      | VDDX     | Power    | Connect to +3.3V source.                                                                                 |
| 20      | S0       | Input    | Spread Spectrum Select pin #0. Internal pull-up resistor.                                                |



Table1 Spread Selection Table

| S2 | S1 | S0 | Spread %  | Spread Type    | Output Frequency |
|----|----|----|-----------|----------------|------------------|
| 0  | 0  | 0  | -0.5      | Down           | 100              |
| 0  | 0  | 1  | -1.0      | Down           | 100              |
| 0  | 1  | 0  | -1.5      | Down           | 100              |
| 0  | 1  | 1  | No Spread | Not Applicable | 100              |
| 1  | 0  | 0  | -0.5      | Down           | 200              |
| 1  | 0  | 1  | -1.0      | Down           | 200              |
| 1  | 1  | 0  | -1.5      | Down           | 200              |
| 1  | 1  | 1  | No Spread | Not Applicable | 200              |

## Absolute Maximum Ratings

| Symbol             | Parameter                  | MIN  | TYP | MAX     | Unit |
|--------------------|----------------------------|------|-----|---------|------|
| T <sub>store</sub> | Storage Temperature        | -65  | -   | +150    | °C   |
| V <sub>DD</sub>    | DC Supply Voltage port B   | -0.5 | -   | 5.5     | V    |
| V <sub>IO</sub>    | Input / Output Voltage     | -0.5 | -   | VDD+0.5 | V    |
| ESD                | ESD HBM protection (input) | 2000 |     |         | V    |

### Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended operation conditions

| Symbol          | Parameter                                   | MIN  | TYP | MAX  | Unit |
|-----------------|---------------------------------------------|------|-----|------|------|
| V <sub>DD</sub> | V <sub>CCA</sub> Positive DC Supply Voltage | 3.0  | -   | 3.6  | V    |
| V <sub>I</sub>  | Control Pin Input Voltage                   | -0.3 | -   | 3.6  | V    |
| T <sub>A</sub>  | Operating Temperature Range                 | -40  | -   | +125 | °C   |



## DC Electrical Characteristics

Unless otherwise specified,  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $3.0\text{V} \leq V_{DD} \leq 3.6\text{V}$

| Symbol | Parameter                         | Conditions                                                       | MIN      | TYP | MAX      | Unit          |
|--------|-----------------------------------|------------------------------------------------------------------|----------|-----|----------|---------------|
| VDD    | Supply Voltage                    |                                                                  | 3.0      | 3.3 | 3.6      | V             |
| VIH    | Input High Voltage <sup>(1)</sup> | OE, S0, S1, S2                                                   | 0.7VDD   |     | VDD +0.3 | V             |
| VIL    | Input Low Voltage <sup>(1)</sup>  | OE, S0, S1, S2                                                   | GND -0.3 |     | 0.3VDD   | V             |
| IIL    | Input Leakage Current             | $0 \leq V_{in} \leq V_{DD}$ Without input pull-up and pull-downs | -5       |     | 5        | $\mu\text{A}$ |
| IDD    | Operating Supply Current          | $R_L = 50\Omega$ , $C_L = 2\text{pF}$                            |          | 105 | 130      | mA            |
| IDDOE  |                                   | OE = LOW                                                         |          | 40  | 50       | mA            |
| IDDPD  | Power down Current                | No pad load, PDn=LOW                                             |          | 60  | 100      | $\mu\text{A}$ |
| CIN    | Input Capacitance                 |                                                                  |          |     | 7        | pF            |
| COUT   | Output Capacitance                |                                                                  |          |     | 6        | pF            |
| LPIN   | Pin Inductance                    |                                                                  |          |     | 5        | nH            |
| ROUT   | Output Resistance                 | CLK Outputs                                                      | 3.0      |     |          | k $\Omega$    |

**Note:**

1.  $R_L = 50\text{ ohm}$  with  $C_L = 2\text{ pF}$
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW



## HCSL Output AC Characteristics

(V<sub>DD</sub> = 3.3V ±10%, T<sub>A</sub> = -40°C to +85°C)

| Symbol              | Parameter                          | Conditions                              | MIN  | TYP  | MAX | Unit |
|---------------------|------------------------------------|-----------------------------------------|------|------|-----|------|
| FIN                 | Input Frequency                    |                                         |      | 25   |     | MHz  |
| VOUT                | Output Frequency                   | S2=HIGH                                 |      |      | 200 | MHz  |
|                     |                                    | S2=LOW                                  |      |      | 100 | MHz  |
| VOH                 | Output High Voltage (1,2)          | 100 MHz HCSL output<br>@ VDD = 3.3V     | 660  | 800  | 900 | mV   |
| VOL                 | Output Low Voltage(1,2)            |                                         | -150 | 0    | 150 | mV   |
| VCPA                | Crossing Point Voltage(1,2)        | Absolute                                | 250  | 350  | 550 | mV   |
| VCN                 | Crossing Point Voltage(1,2,4)      | Variation over all edges                |      |      | 140 | mV   |
| JCC                 | Jitter, Cycle-to-Cycle(1,3)        |                                         |      | 40   | 60  | ps   |
| J <sub>RMS2.0</sub> | PCIe 2.0 RMS Jitter                | PCIe 2.0 Test Method @ 100MHz<br>Output |      |      | 3.1 | ps   |
| J <sub>RMS3.0</sub> | PCIe 3.0 RMS Jitter                | PLL L-BW @ 2M & 5M 1st H3               |      | 2.1  | 3   | ps   |
|                     |                                    | PLL L-BW @ 2M & 4M 1st H3               |      | 2.38 | 3   | ps   |
|                     |                                    | PLL H-BW @ 2M & 5M 1st H3               |      | 0.48 | 1   | ps   |
|                     |                                    | PLL H-BW @ 2M & 4M 1st H3               |      | 0.47 | 1   | ps   |
| MF                  | Modulation Frequency               | Spread Spectrum                         | 30   | 31.5 | 33  | kHz  |
| t <sub>OR</sub>     | Rise Time(1,2)                     | From 0.175V to 0.525V                   | 150  | 332  | 700 | ps   |
| t <sub>OF</sub>     | Fall Time(1,2)                     | From 0.525V to 0.175V                   | 150  | 344  | 700 | ps   |
| TSKEW               | Skew between outputs               | At Crossing Point Voltage               |      |      | 50  | ps   |
| TDUTY-CYCLE         | Duty Cycle(1,3)                    |                                         | 45   |      | 55  | %    |
| TOE                 | Output Enable Time(5)              | All outputs                             |      |      | 10  | μs   |
| TOT                 | Output Disable Time(5)             | All outputs                             |      |      | 10  | μs   |
| t <sub>STABLE</sub> | From power-up to VDD=3.3V          | From Power-up VDD=3.3V                  |      | 3.0  |     | ms   |
| t <sub>SPREAD</sub> | Setting period after spread change | Setting period after spread change      |      | 3.0  |     | ms   |

**Note:**

1. R<sub>L</sub> = 50 ohm with C<sub>L</sub> = 2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW



## Application Information

### Decoupling Capacitors

Decoupling capacitors of 0.01 $\mu$ F should be connected between each VDD pin and the ground plane and placed as close to the VDD pin as possible.

### Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

### Crystal Capacitors

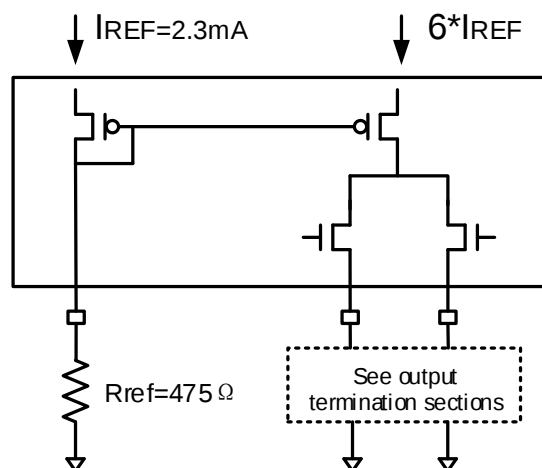
$C_L$  = Crystals' load capacitance in pF  
Crystal Capacitors (pF) =  $(C_L - 8) * 2$

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF.  $(16-8)*2=16$ .

### Current Source (IREF) Reference Resistor – Rref

If board target trace impedance is 50 $\Omega$ ,

then  $R_{ref} = 475\Omega$  providing an IREF of 2.32 mA. The output current (IOH) is 6\*IREF.



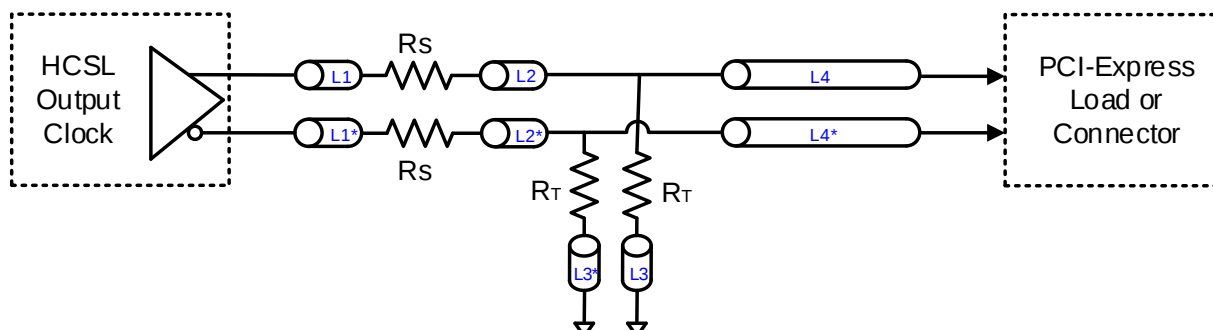
### Output Termination

The PCI Express differential clock outputs of the RS2CG5704B are open-source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The RS2CG5704B can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.



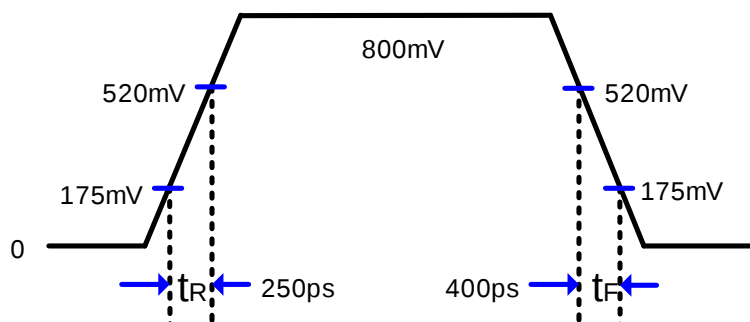
## PCIe Device Routing (HCSL)



### PCI Express Layout Guidelines

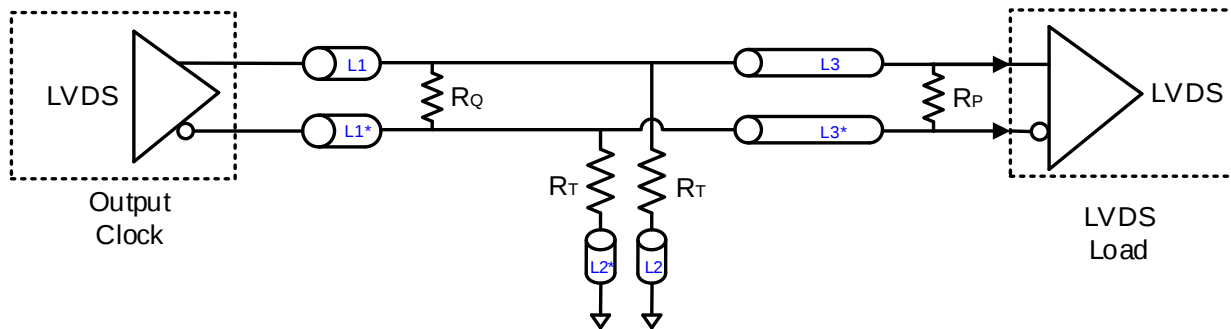
| Common Recommendations for Differential Routing                 | Dimension or Value    | Unit |
|-----------------------------------------------------------------|-----------------------|------|
| L1 length, route as non-coupled 50Ω trace.                      | 0.5 max               | inch |
| L2 length, route as non-coupled 50Ω trace.                      | 0.2 max               | inch |
| L3 length, route as non-coupled 50Ω trace.                      | 0.2 max               | inch |
| $R_S$                                                           | 33                    | Ω    |
| $R_T$                                                           | 49.9                  | Ω    |
| Differential Routing on a Single PCB                            | Dimension or Value    | Unit |
| L4 length, route as coupled microstrip 100Ω differential trace. | 2 min to 16 max       | inch |
| L4 length, route as coupled strip-line 100Ω differential trace. | 1.8 min to 14.4 max   | inch |
| Differential Routing to a PCI Express connector                 | Dimension or Value    | Unit |
| L4 length, route as coupled microstrip 100Ω differential trace. | 0.25 min to 14 max    | inch |
| L4 length, route as coupled strip-line 100Ω differential trace. | 0.225 min to 12.6 max | inch |

### Typical HCSL Waveform





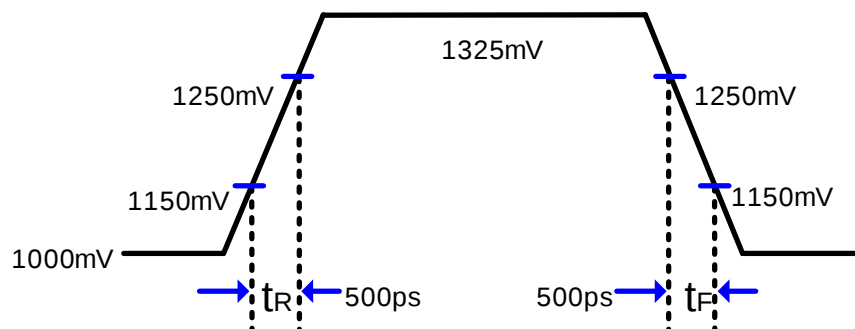
## LVDS Device Routing



### LVDS Device Routing Guidelines

| LVDS Recommendations for Differential Routing                  | Dimension or Value | Unit |
|----------------------------------------------------------------|--------------------|------|
| L1 length, route as non-coupled 50Ω trace.                     | 0.5 max            | inch |
| L2 length, route as non-coupled 50Ω trace.                     | 0.2 max            | inch |
| RP                                                             | 100                | Ω    |
| RQ                                                             | 100                | Ω    |
| RT                                                             | 150                | Ω    |
| L3 length, route as 100Ω differential trace(strip-line)        | 14 max.            | inch |
| L3 length, route as 100Ω differential trace.(Micro Strip-line) | 12 max.            | inch |

### Typical LVDS Waveform



**RSM**

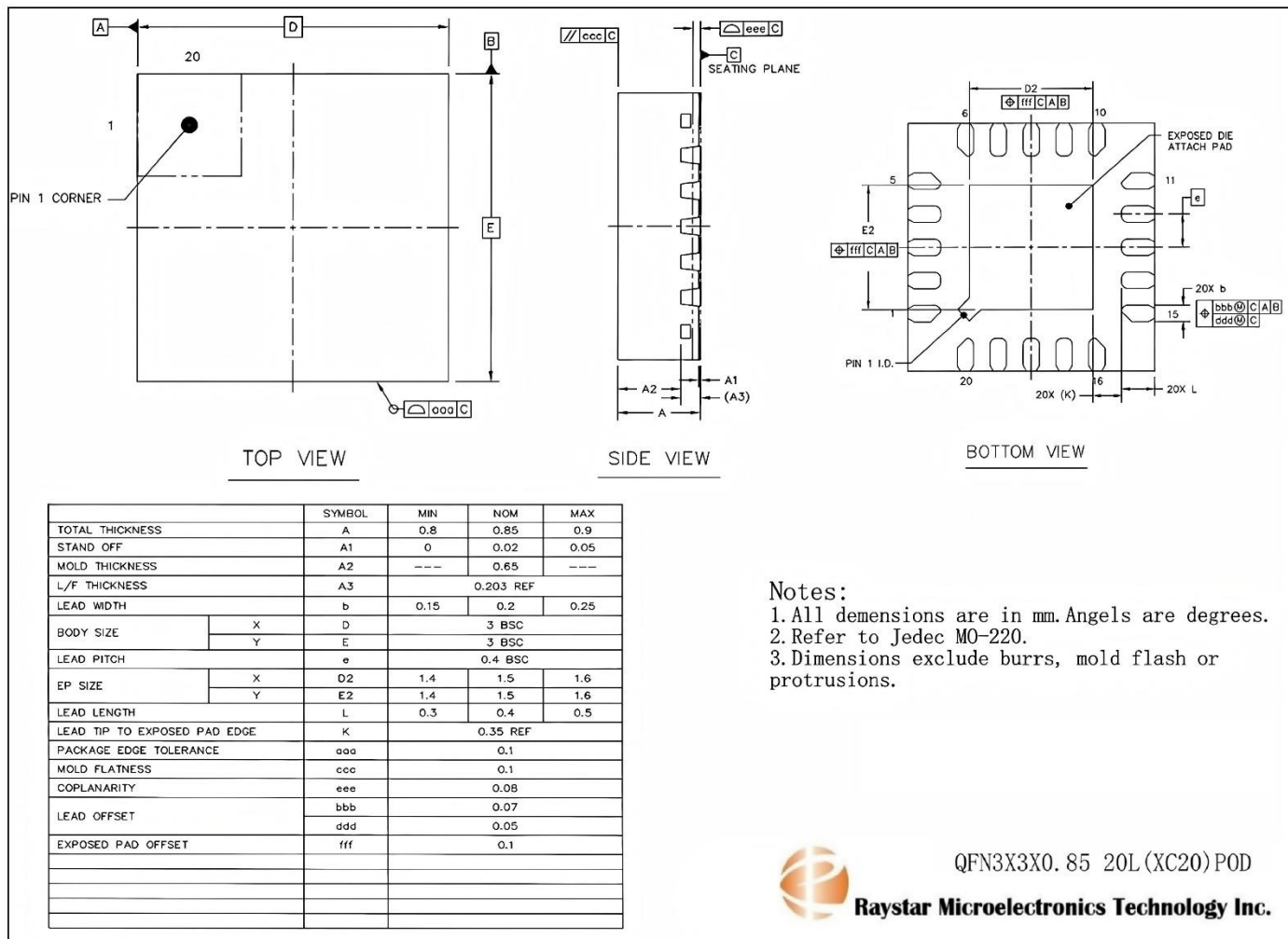
www.raystar-tek.com

**RS2CG5704B**

PCIe3.0 Clock Generator with 4 HCSL Outputs

## Packaging Information

### QFN-20L



QFN3X3X0.85 20L (XC20) P0D

**Raystar Microelectronics Technology Inc.**



## Revision History

| Revision | Description                                        | Date       |
|----------|----------------------------------------------------|------------|
| V1.0     | Initial release                                    | 2026/06/04 |
| V1.1     | Modify the feature and description error on Page 1 | 2026/06/25 |
|          |                                                    |            |