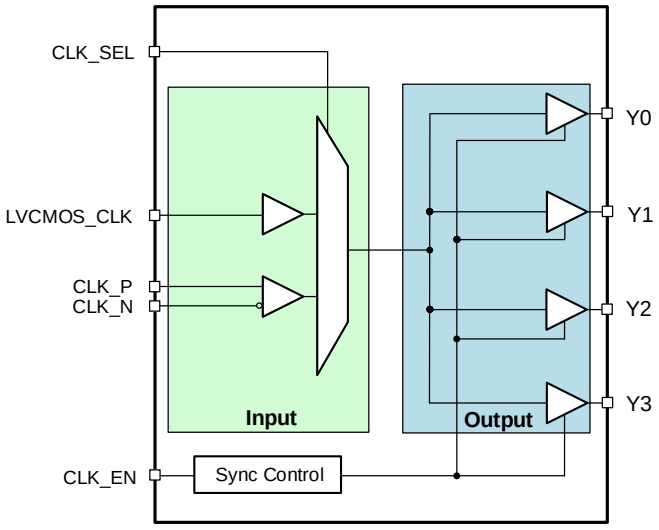
Features

- 2:4 LVCMOS Output Clock Buffer
- 12kHz to 20MHz additive phase jitter: 25fs(Typical) RMS at 156.25MHz
- Operates DC to 200MHz
- Universal Input: LVPECL,LVDS,HCSL,SSTL, LVCMOS and LVTTL
- Output Skew: 30ps(Typical)
- Total Propagation Delay: 2ns(Typical)
- Synchronous and Glitch-Free Output Enable Is Available
- Spread-spectrum tolerant
- -40 to +85°C,
- 3.3V/2.5V Core Power Supply
- 3.3V/2.5V/1.8V/1.5V Output Power Supply
- VDDO can't be greater than VDD
- TQFN-16L 3.0 x 3.0mm package

Applications

- Wireless and Wired Infrastructure
- Networking and Data Communications
- Medical electronics
- Portable Test and Measurement

Block Diagram



Description

The RS2CB0814 device is a high-performance, low-jitter, low-power clock fanout buffer which can distribute to ten low-jitter LVCMOS clock outputs from one of three inputs, whose primary and secondary inputs can feature differential or single-ended signals and crystal input. Such a buffer is good for use in a variety of mobile and wired infrastructure, data communication, computing, low-power medical imaging, and portable test and measurement applications. When the input is an illegal level, the output is at a defined state. One can set the core to 2.5V or 3.3V, and output to 1.5V/1.8V/2.5V or 3.3V. The overall additive jitter performance is 25fs RMS (typical).

Ordering Information

Part Number	Package	Description
RS2CB0814ZHE	TQFN-16L	3.0×3.0x0.75 mm

Notes:
[1] E = Pb-free and Green

Pin Configuration

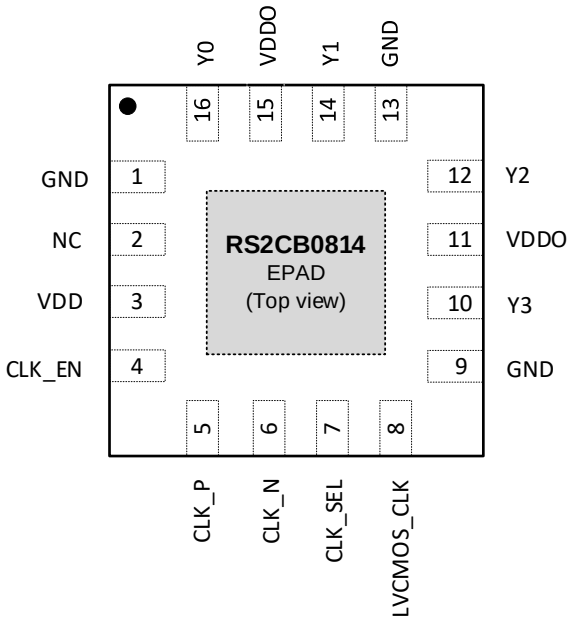


Figure 1. Pin Assignments for TQFN-16L Package

Pin Description

Table 1. Pin Descriptions

Pin Name	Number	Type	Description	Notes	
CLK_EN	4	I, SE, PD	Output Enable. Typically connected to VDD with an external 1-kΩ pullup. When unused, leave floating. 0 = Outputs are forced to logic low state 1 = Outputs are enabled with LVCMOS/LVTTL levels	1	
CLK_P	5	I, DIF, SE	.Primary true clock input or single-ended clock.	3	
CLK_N	6	I, DIF	Primary complementary clock input. Leave CLK_N floating if CLK_P is driven by a single-ended clock	2	
CLK_SEL	7	I, SE, PD	Clock select input. Typically connected to VDD with an external 1-kΩ pullup. When unused, leave floating. 0 = Select LVCMOS_CLK (pin 8) 1 = Select CLK_P, CLK_N (pins 5, 6)	1	
LVCMOS_CLK	8	I, PD	Single-ended clock input with internal 51-kΩ (typ) pulldown resistor to GND. Typically connected to a single-ended clock input. When unused,leave floating. Accepts LVCMOS/LVTTL levels.	3	
Y0	16	O, SE	LVCMOS Output 0.		
Y1	14	O, SE	LVCMOS Output 1.		
Y2	12	O, SE	LVCMOS Output 2.		
Y3	10	O, SE	LVCMOS Output 3.		
VDD	3	Power	Power Supply for operating Core and Clock Input.		

Pin Name	Number	Type	Description	Notes	
VDDO	11, 15	Power	Power Supply for Clock Output.		
GND	1, 9, 13	GND	Ground pin.		
NC	2		Not connected.		
EPAD		GND	Connect EPAD to ground.		

1. CMOS control input with internal pull-down resistor(150 kΩ).
2. Clock input with internal biased to Vdd / 2 (pullup or pulldown of 150 kΩ).
3. Clock input with internal pull-down resistor(150 kΩ).

Table 2. Signal Types

Term	Description
I	Input
O	Output
PD	Pull-down
PU	Pull-up
SE	Single-ended
DIF	Differential
Power	Power
GND	Ground

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CB0814 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN	MAX	Units	Notes
Core Supply Voltage	V_{DD}		-0.5	4.6	V	1,2
Output Supply Voltage	V_{DDO}		-0.5	4.6	V	1,2
Input Voltage	V_{IN}		-0.5	V_{DD} +0.5	V	
Output Voltage	V_{OUT}		-0.5	V_{DD} +0.5	V	
Storage-temperature Temperature	T_{STG}		-65	125	°C	
Junction Temperature	T_J	Maximum operating junction temperature.		125	°C	
Input ESD Protection	ESD	Human Body Model.	2500		V	
		Charged-device Model	1000		V	

1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Core Supply Voltage	V_{DD}		2.375	2.5	2.625	V	
			3.135	3.3	3.465		
Output Supply Voltage	V_{DDO}		1.35	1.5	1.65	V	1
			1.6	1.8	2		
			2.375	2.5	2.625		
			3.135	3.3	3.465		
High-level output current, LVCMOS	I_{OH}				-24	mA	
Low-level output current, LVCMOS	I_{OL}				24	mA	
Operating Temperature	T_A		-40	25	85	°C	

1. V_{DDO} can't be greater than V_{DD} ($V_{DDO} \leq V_{DD}$).

Current Consumption

2.375V ≤ V_{DD} ≤ 3.45V, 1.35V ≤ V_{DDO} ≤ V_{DD}, -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at V_{DD} = V_{DDO} = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Table 5. Current Consumption

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Power supply current through VDD	I_{DD}	V_{DD} / V_{DDO} = 3.3V CLK_EN = 0V or V_{DD}; Ref. input = 0 V or V_{DD}; I_O = 0mA;		2		mA	
		V_{DD} / V_{DDO} = 1.8V CLK_EN = 0V or V_{DD}; Ref. input = 0 V or V_{DD}; I_O = 0mA;		1			
Power supply current through VDDO	I_{DDO}	V_{DD} / V_{DDO} =3.3V CLK_EN = 0V or V_{DD}; Ref. input = 0 V or V_{DD}; I_O = 0mA;		10		mA	
		V_{DD} / V_{DDO} =1.8V CLK_EN = 0V or V_{DD}; Ref. input = 0 V or V_{DD}; I_O = 0mA;		5			

Input Characteristics

2.375V ≤ V_{DD} ≤ 3.45V, 1.35V ≤ V_{DDO} ≤ V_{DD}(V_{DDO} ≤ V_{DD}), -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at V_{DD} = V_{DDO} = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Table 6. Input Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
DC Characteristic (CLK_EN, CLK_SEL, CLK_P/N, LVCMOS_CLK)							
Input High Current	I_{IH}	V_{DD}=3.465V, V_{IH}=3.465V			40	µA	
Input Low Current	I_{IL}	V_{DD}=3.465V, V_{IH}=0V			-40		
Input edge rate	ΔV/ΔT	20%--80%		2		V/ns	
Pullup or pulldown resistance	$R_{PU/PD}$			150		kΩ	
Input capacitance	C_{IN}			2		pF	
Single-Ended DC Characteristic							
Input High Voltage	V_{IH}	V_{DD} = 3.3V ±5%	2		V_{DD}+0.3	V	1
		V_{DD} = 2.5V ±5%	1.6		V_{DD}+0.3		
Input Low Voltage	V_{IL}	V_{DD} = 3.3V ±5%	-0.3		1.3		
		V_{DD} = 2.5V ±5%	-0.3		0.9		
Single-Ended DC Characteristic (CLK_EN, CLK_SEL)							
Input High Voltage	V_{IH}		0.7 x V_{DD}			V	
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V	
Differential DC Characteristic (CLK_P/N)							
Differential input voltage swing	$V_{I,DIFF}$		0.15		1.3	V	2
Input common-mode voltage	V_{ICM}		0.5		V_{DD}-0.85		3
AC Characteristic (CLK_P/N)							
Input Frequency	F_{IN}				200	MHz	
Input duty cycle	I_{DC}		40%		60%		

1. PRI/SEC_INN biased to VDD/2.
2. V_{IL} should not be less than –0.3V.
3. Input common-mode voltage is defined as V_{IH} (see Figure 19).

Output Characteristics

2.375V ≤ VDD ≤ 3.45V, 1.35V ≤ VDDO ≤ VDD(VDDO ≤ VDD), -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at VDD = VDDO = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured. Test conditions: load 50Ω to VDDO/2

Table 7. Output Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Output Skew	$t_{SK(O)}$	Measured between outputs(Ym to Yn)		30	50	ps	
Part-to-Part Skew	$t_{SK(PP)}$				300	ps	1
Propagation Delay Clock IN to Clock OUT	t_{DELAY}	V_{DD} = 3.3 V ±5%, V_{DDO} = 1.35 V to V_{DD}	1.5	1.95	5.0	ns	
		V_{DD} = 2.5 V ±5%, V_{DDO} = 1.35 V to V_{DD}	1.8	2.4	6.0		
Output slew rate, rising and falling	$t_{SLEW-RATE}$	V_{DDO}=3.3V +/- 5%, 20% to 80%	5.6	7.3	9.0	V/ns	
		V_{DDO}=2.5V +/- 5%, 20% to 80%	3.9	4.8	5.4		
		V_{DDO}=1.8V +/- 200mV, 20% to 80%	1.6	2.1	2.5		
		V_{DDO}=1.5V +/- 150mV, 20% to 80%	0.9	1.2	1.4		
Output Frequency	F_{OUT}				200	MHz	
Output High Voltage	V_{OH}	V_{DDO} = 3.135V to 3.465V	0.8*V_{DDO}			V	
		V_{DDO} = 2.375V to 2.625V	0.8*V_{DDO}				
		V_{DDO} = 1.6V to 2V	0.7*V_{DDO}				
		V_{DDO} = 1.35V to 1.65V	0.7*V_{DDO}				
Output Low Voltage	V_{OL}	V_{DDO} = 3.135V to 3.465V			0.2*V_{DDO}	V	
		V_{DDO} = 2.375V to 2.625V			0.2*V_{DDO}		
		V_{DDO} = 1.6V to 2V			0.3*V_{DDO}		
		V_{DDO} = 1.35V to 1.65V			0.3*V_{DDO}		
Output Resistance	R_{CLKOUT}	V_{DDO} = 3.3V		15		ohm	
		V_{DDO} = 2.5V		20			
		V_{DDO} = 1.8V		25			
		V_{DDO} = 1.5V		30			
System-level additive jitter	t_{RJIT}	Single-ended input, V_{DD} = 3.3V V_{DDO} = 3.3V		25		fs, RMS	2
		Single-ended input, V_{DD} = 2.5V or 3.3V V_{DDO} = 1.5V,1.8V,2.5V, $F_{IN/OUT}$=125MHz		30			
		Differential input, V_{DD} = 3.3V V_{DDO} = 3.3V		30			
		Differential input, V_{DD} = 2.5V or 3.3V V_{DDO} = 1.5V,1.8V,2.5V, $F_{IN/OUT}$=125MHz		30			
Noise floor	NF	10KHz offset		–145		dBc/Hz	3
		100KHz offset		–156			
		1MHz offset		–163			
		10MHz offset		–164			
		20MHz offset		–164			
		10KHz offset		–145			4
		100KHz offset		–155			
		1MHz offset		–160			
		10MHz offset		–161			
		2-MHz offset		–162			
Output duty cycle	O_{DC}	$F_{IN/OUT}$=125MHz, I_{DC} = 50%	45%		55%		5
Output enable or disable time	t_{EN}				2	Cycle	

MUX isolation	$MUX_{ISOLATION}$	125MHz	55			dB	6

1. Calculation for part-to-part skew is the difference between the fastest and the slowest tpd across multiple devices.
2. Integration range: 12KHz–20MHz; input source see the *System-Level Additive-Jitter Measurement* section.
3. Single-ended input, $f_{IN/OUT}$ = 125MHz, VDD = VDDO = 3.3V.
4. Differential input, $f_{IN/OUT}$ = 125MHz, VDD = VDDO = 3.3V.
5. Stable V_{IH}, V_{IL}, and V_{CM}
6. See Figure 18.

Phase Noise

VDD = VDDO = 2.5V or 3.3V, CLK_P/N = 25MHz, TA = 25°C (unless otherwise noted).

Table 8. PHASE NOISE

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
RMS phase jitter	Jrms	IB = 12kHz to 5MHz, VDD = VDDO = 3.3V		80		fs rms	
		IB = 12kHz to 5MHz, VDD = VDDO = 2.5V		115			
Phase noise (see Figure 15)	PN	f_{offset} = 100Hz, VDD = VDDO = 3.3V		–92		dBc/Hz	
		f_{offset} = 1kHz, VDD = VDDO = 3.3V		–137			
		f_{offset} = 10kHz, VDD = VDDO = 3.3V		–163			
		f_{offset} = 100kHz, VDD = VDDO = 3.3V		–168			
		f_{offset} = 1MHz, VDD = VDDO = 3.3V		–168			
		f_{offset} = 5MHz, VDD = VDDO = 3.3V		–169			
		f_{offset} = 100Hz, VDD = VDDO = 2.5V		–91			
		f_{offset} = 1kHz, VDD = VDDO = 2.5V		–136			
		f_{offset} = 10kHz, VDD = VDDO = 2.5V		–159			
		f_{offset} = 100kHz, VDD = VDDO = 2.5V		–164			
		f_{offset} = 1MHz, VDD = VDDO = 2.5V		–165			
		f_{offset} = 5MHz, VDD = VDDO = 2.5V		–165			

Parameter Measurement Information

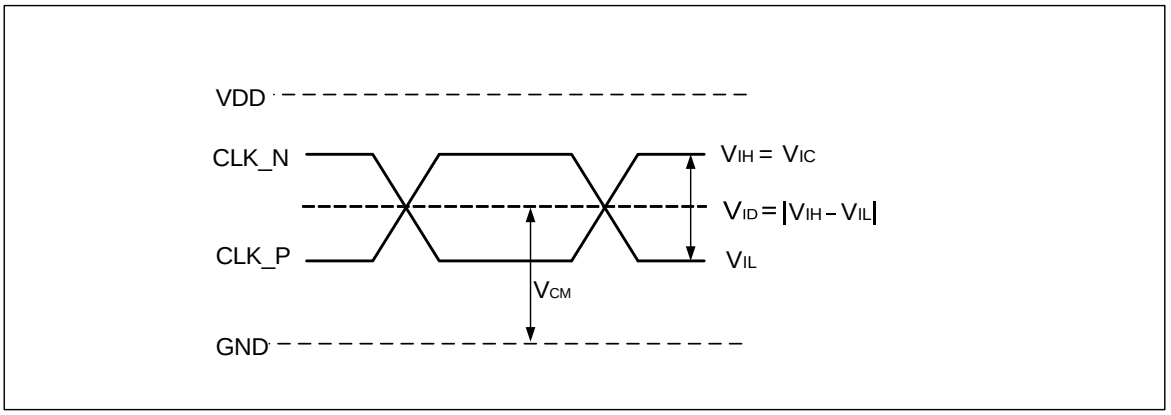


Figure 5. Differential Input Level

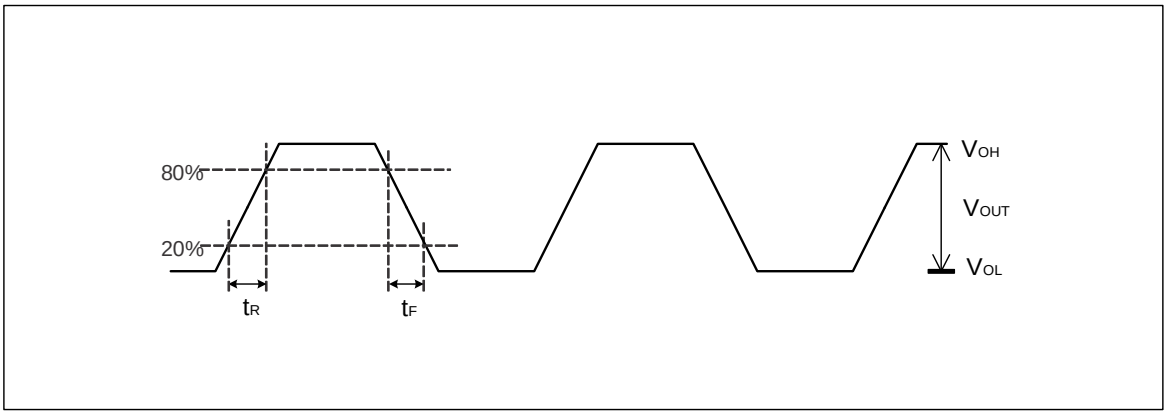


Figure 6. LVCMOS Output Voltage, and Rise and Fall Times

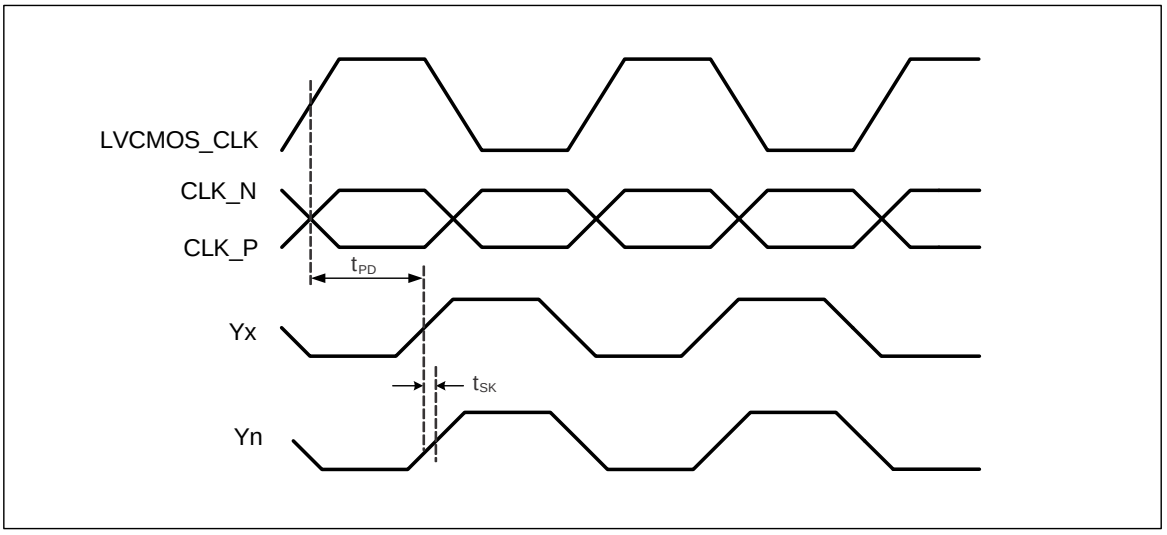


Figure 7. Differential and Single-Ended Output Skew and Propagation Delay

Output Enable

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in ***Figure 8.***

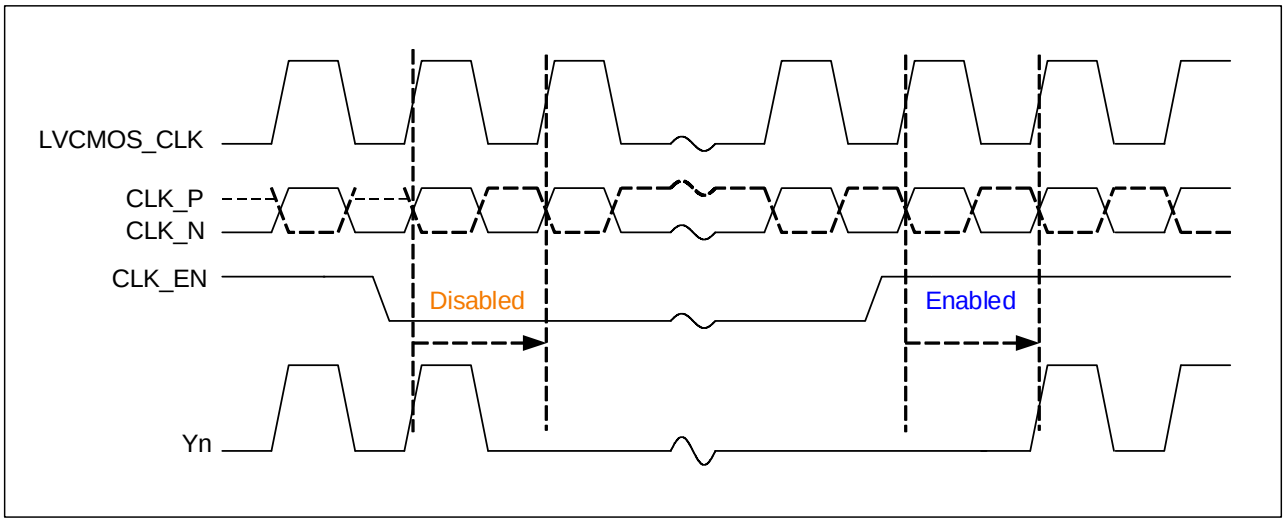


Figure 8. Clock Enable Timing

Application Information

Typical Applications

Refer to the following sections for output clock and input clock interface circuits.

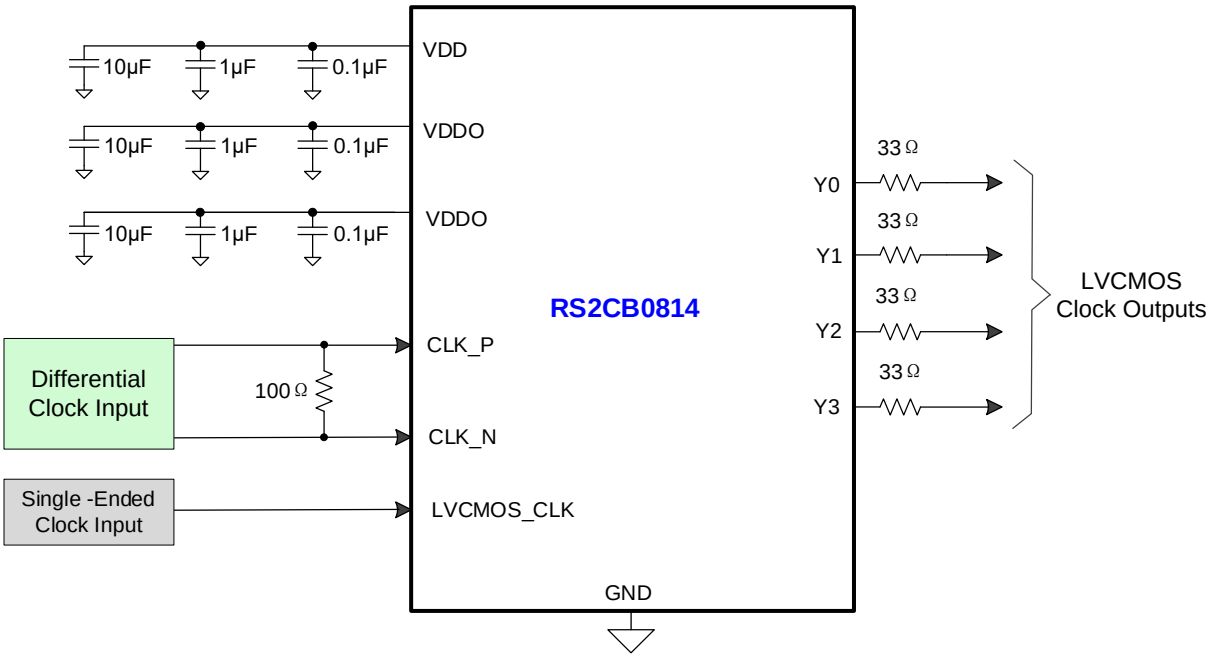


Figure 2. Typical Application Circuit

Input Clock Interface Circuits

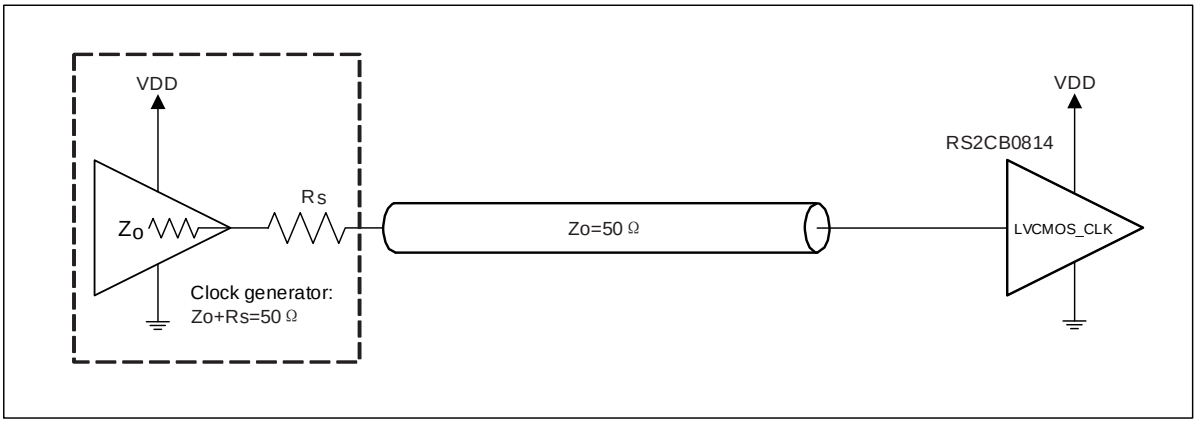


Figure 3. LVCMOS_CLK Input Configuration

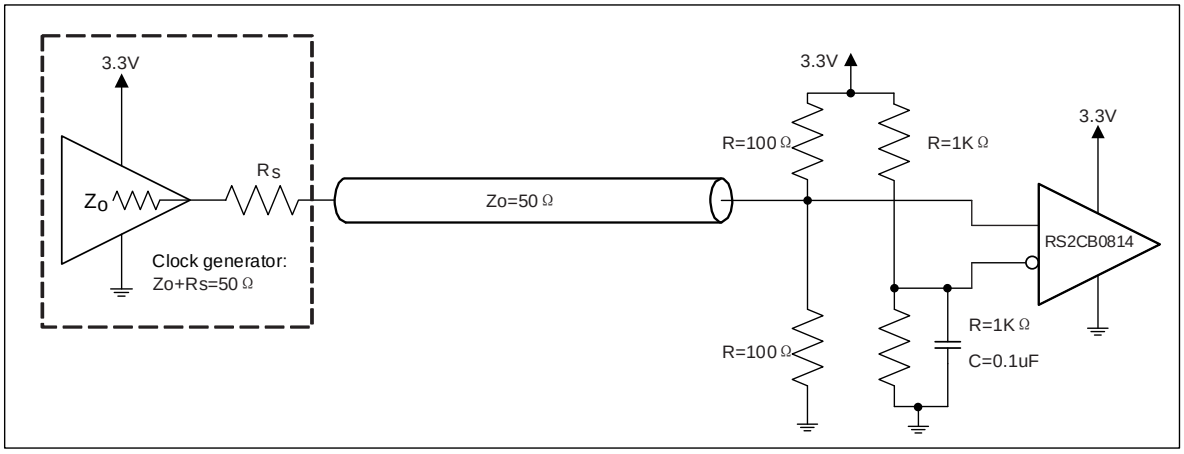


Figure 4. Single-Ended/LVCMOS Input DC Configuration

● Power Supply Filtering

It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is very critical to applications.

Use of filter capacitors eliminates the low-frequency noise from power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them very close to the power supply pins and lay out traces with short loops to minimize inductance. RSM recommends to adding as many high- frequency (for example, 0.1µF) bypass capacitors as there are supply pins in the package.

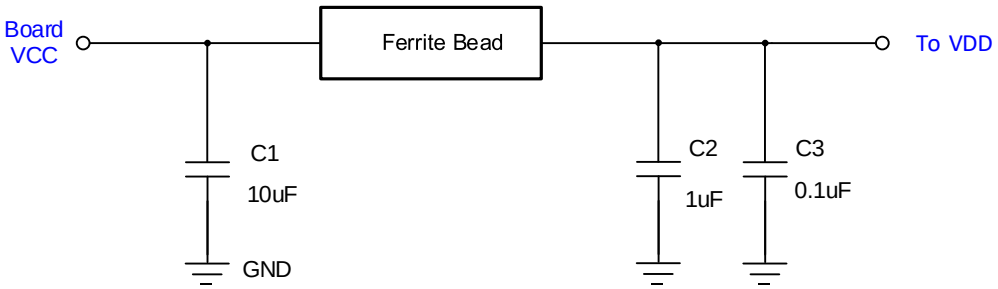
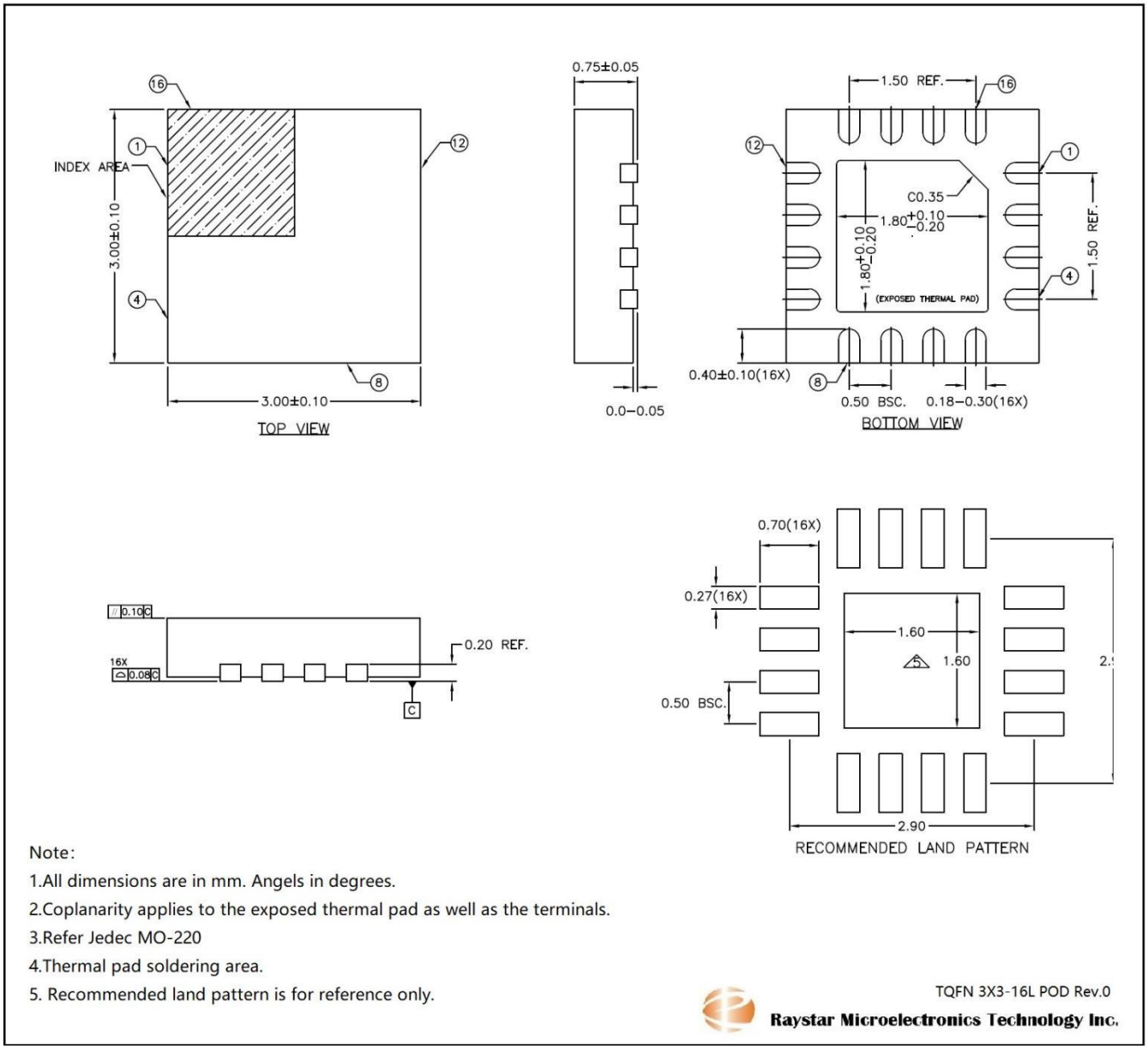


Figure 5. Power-Supply Decoupling

Package Information

TQFN-16L



Note:

1.All dimensions are in mm. Angels in degrees.

2.Coplanarity applies to the exposed thermal pad as well as the terminals.

3.Refer Jedec MO-220

4.Thermal pad soldering area.

5. Recommended land pattern is for reference only.

TQFN 3X3-16L POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary release	2026/01/09
1.0	Release	2026/06/27