## Features

- Ultra-Low Jitter 5 LVCMOS Output Clock Buffer
- 12kHz to 20MHz additive phase jitter: <30fs RMS at 156.25MHz
- Operates DC to 200MHz
- Crystal Input: 10 to 50MHz
- Universal Input: LVPECL,LVDS,HCSL,SSTL,LVCMOS and LVTTL
- Output Skew: < 6ps
- Distributes One Clock Input to Two Banks
- Spread-spectrum tolerant
- Low Propagation Delay
- -40 to +85°C, 3.3V,2.5V Core Power Supply
- 3.3V,2.5V,1.8V and 1.5V Output Power Supply
- VDDO can't be greater than VDD (VDDO≤ VDD)
- QFN-24L 4.0mm x 4.0mm

## Applications

- General-Purpose Applications
- Networking
- Medical electronics
- Portable Test and Measurement

## Description

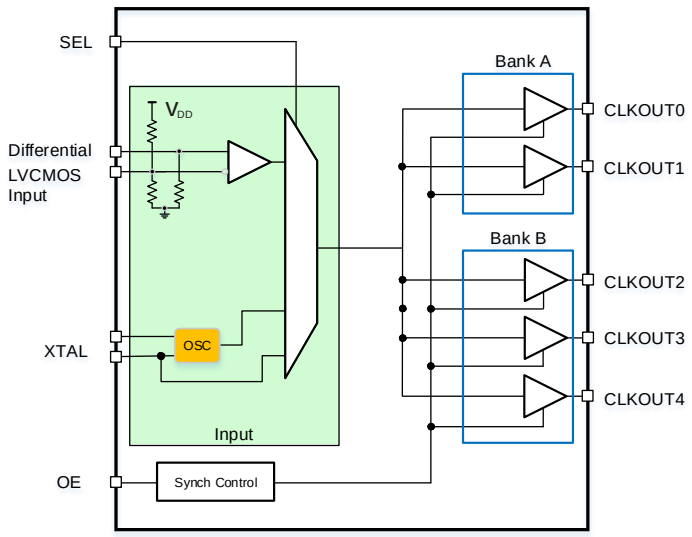
The RS2CB00105 device is a high-performance, low-skew clock buffer intended for low-jitter clock/data distribution and level translation.
Two banks provide five ultra-low jitter and high PSRR clocks from a differential, single-ended, or crystal input.
The RS2CB00105 operates from a 3.3V/2.5V core supply and 2 independent 3.3V/2.5V/1.8V/1.5V output supplies.
Core power supply, Bank A supply, and Bank B supply can be configured to different voltages which can increase the design flexibility of power supply and LVCMOS output amplitude.

## Ordering Information

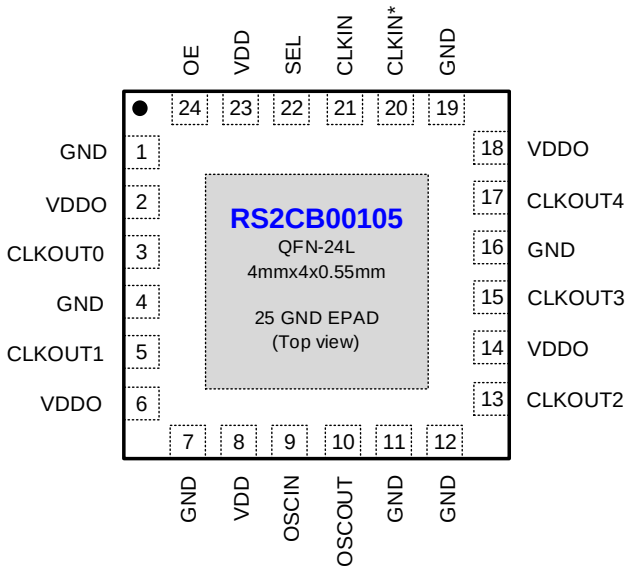
| Part Number | Package | Description |
|---|---|---|
| RS2CB00105ZU | QFN-24L | 4.0 × 4.0 mm, 0.5mm pitch |

Notes:
[1] E = Pb-free and Green

## Block Diagram



## Pin Configuration




**Pin Assignments for QFN-24L Package – Top View**

## Pin Description

**Table 1. Pin Descriptions**

| Pin Name | Number | Type | Description | Notes |
|---|---|---|---|---|
| VDD | 8, 23 | Power | Power Supply for operating Core and Clock Input. | |
| VDDO | 2, 6 | Power | Power Supply for Bank A (CLKOUT0 and CLKOUT1) Clock Output. | |
| VDDO | 14, 18 | Power | Power Supply for Bank B (CLKOUT2, CLKOUT3 and CLKOUT4) Clock Output. | |
| GND | 1, 4, 7, 11, 12, 16, 19 | GND | Ground pin. | |
| SEL | 22 | I, SE, PD | Clock Input Selection.<br>1 = Clock Input from OSCIN(Crystal Mode), 0 = Clock Input from CLKIN, CLKIN*. | 1 |
| OE | 24 | I, SE, PD | Output Enable.<br>1 = enable output, 0 = disable output. | 1 |
| OSCIN | 9 | I, SE | Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock. | |
| OSCOUT | 10 | O, SE | Output for crystal. Leave OSCOUT floating if OSCIN is driven by a single-ended clock. | |
| CLKIN* | 20 | I, DIF | Complementary clock input. Leave CLKIN* floating if CLKIN is driven by a single-ended clock. | |
| CLKIN | 21 | I, DIF, SE | True clock input or single-ended clock. | |

| Pin Name | Number | Type | Description | Notes |
|---|---|---|---|---|
| CLKOUT0 | 3 | O, SE | LVCMOS Output 0. | 2 |
| CLKOUT1 | 5 | O, SE | LVCMOS Output 1. | 2 |
| CLKOUT2 | 13 | O, SE | LVCMOS Output 2. | 3 |
| CLKOUT3 | 15 | O, SE | LVCMOS Output 3. | 3 |
| CLKOUT4 | 17 | O, SE | LVCMOS Output 4. | 3 |
| EPAD | 25 | GND | Connect EPAD to ground. | |

1. CMOS control input with internal pull-down resistor.
2. Clock output belongs to Bank A.
3. Clock output belongs to Bank B.

### Table 2. Signal Types

| Term | Description |
|---|---|
| I | Input |
| O | Output |
| PD | Pull-down |
| PU | Pull-up |
| SE | Single-ended |
| DIF | Differential |
| Power | Power |
| GND | Ground |

### Table 3. Input Selection

| SEL | SELECTED INPUT |
|---|---|
| 0 | CLKIN, CLKIN* |
| 1 | OSCIN (Crystal Mode) |

### Table 4. Output Enable

| OE | Output |
|---|---|
| 0 | Disabled (Hi-Z) |
| 1 | Enabled |

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CB00105 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 5. Absolute Maximum Ratings**

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | | -0.3 | | 3.6 | V | 1,2 |
| Output Supply Voltage | $V_{DDO}$ | | -0.3 | | 3.6 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.3 | | $V_{DD}$ +0.3 | V | |
| Lead Temperature (solder 4 s) | $T_L$ | | | | 260 | °C | |
| Storage Temperature | $T_S$ | | -65 | | 150 | °C | |
| Junction Temperature | $T_J$ | Maximum operating junction temperature. | | | 125 | °C | |
| Input ESD Protection | ESD | Human Body Model. | 2500 | | | V | |
| | | Charged-device Model | 1000 | | | V | |

1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.

## Recommended Operating Conditions

**Table 6. Recommended Operating Conditions**

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | | 2.375 | 2.5 | | V | |
| | | | | 3.3 | 3.45 | | |
| Output Supply Voltage | $V_{DDO}$ | | 1.425 | 1.5 | $V_{DD}$ | V | 1 |
| | | | | 1.8 | $V_{DD}$ | | |
| | | | | 2.5 | $V_{DD}$ | | |
| | | | | 3.3 | $V_{DD}$ | | |
| Operating Temperature | $T_A$ | | -40 | 25 | 85 | °C | |

1. $V_{DDO}$ can't be greater than $V_{DD}$ ($V_{DDO} \leq V_{DD}$).

## Current Consumption

2.375V ≤ VDD ≤ 3.45V, 1.425V ≤ VDDO ≤ VDD, -40°C ≤ TA ≤ 85°C, Differential inputs. Typical values represent most likely parametric norms at VDD = VDDO = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured. Test conditions : CL = 5pF in parallel with 50Ω unless otherwise stated.

**Table 8. Current Consumption**

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| Core Current | $I_{VDD}$ | No CLKIN | | 16 | 25 | mA | |
| | | $V_{DD}$=3.3V @100MHz | | 24 | | | |
| | | $V_{DD}$=2.5V @100MHz | | 20 | | | |
| Each Output Current | $I_{VDDO[N]}$ | OE=High, $V_{DDO}$=3.3V @100MHz | | 7 | | mA | |
| | | OE=High, $V_{DDO}$=2.5V @100MHz | | 5 | | | |
| | | OE=High, $V_{DDO}$=1.8V @100MHz | | 4 | | | |
| | | OE=High, $V_{DDO}$=1.5V @100MHz | | 4 | | | |
| | | OE=Low | | 0.1 | | | |
| Total Current with Loads on all outputs | $I_{VDD}$ + $I_{VDDO}$ | OE=High @100MHz | | 48 | | mA | |
| | | OE=High @200MHz | | 55 | | | |
| | | OE=Low | | 16 | | | |

## Input Characteristics

2.375V ≤ $V_{DD}$ ≤ 3.45V, 1.425V ≤ $V_{DDO}$ ≤ $V_{DD}$, -40°C ≤ TA ≤ 85°C, Differential inputs. Typical values represent most likely parametric norms at $V_{DD}$ = $V_{DDO}$ = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured. Test conditions : $F_{Input}$ = 100MHz, $C_L$ = 5pF in parallel with 50Ω unless otherwise stated.

**Table 9. Input Characteristics**

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (OE, SEL0, SEL1)** | | | | | | | |
| Input Low Voltage | $V_{IL}$ | $V_{DD}$=2.5V | | | 0.4 | V | |
| | | $V_{DD}$=3.3V | | | 0.4 | | |
| Input High Voltage | $V_{IH}$ | $V_{DD}$=2.5V | 1.3 | | | | |
| | | $V_{DD}$=3.3V | 1.6 | | | | |
| Input Low Current | $I_{IL}$ | | -5 | | 5 | uA | |
| Input High Current | $I_{IH}$ | | | | 50 | | |
| **CLKIN/CLKIN* INPUT** | | | | | | | |
| Input Frequency | $F_{IN}$ | Differential or Single-Ended Input | | | 200 | MHz | 3 |
| Input High Current | $I_{IH}$ | $V_{CLKIN}$ = $V_{DD}$ | | | 20 | uA | |
| Input Low Current | $I_{IL}$ | $V_{CLKIN}$ = 0V | -20 | | | | |
| Input High Voltage | $V_{IH}$ | | | | $V_{DD}$ | V | |
| Input Low Voltage | $V_{IL}$ | | 0 | | | | |
| Differential Input Swing | $V_{SW\_DIF}$ | CLKIN Driven Differentially | 0.15 | | 1.5 | V | |
| Differential Input Common Mode Voltage | $V_{CM}$ | $V_{SW\_DIF}$ = 150mV | 0.5 | | $V_{DD}$ - 1.2 | V | 2 |

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | $V_{SW\_DIF}$ = 350mV | 0.5 | | $V_{DD}$ - 1.1 | | |
| | | $V_{SW\_DIF}$ = 800mV | 0.5 | | $V_{DD}$ - 0.9 | | |
| Single-Ended Input Swing | $V_{SW\_SE}$ | | 0.3 | | 2 | $V_{PP}$ | 1 |
| **OSCIN/OSCOUT INPUT** | | | | | | | |
| OSCIN Input Frequency | $F_{OSCIN}$ | Single-Ended Input | | | 200 | MHz | 3 |
| Crystal Input Frequency | $F_{XTAL}$ | Fundamental Mode Crystal<br>ESR < 200 Ω ($F_{XTAL}$ ≤ 30 MHz )<br>ESR < 120 Ω ($F_{XTAL}$ > 30 MHz ) | 10 | | 50 | MHz | 3,4 |
| Shunt Capacitance | $C_{OSCIN}$ | | | 1 | | pF | |
| Input High Voltage | $V_{IH}$ | Single-Ended Input | | | 2.5 | V | |

1. Parameter is specified by design, not tested in production.
2. When using differential signals with $V_{CM}$ outside of the acceptable range for the specified $V_{SW\_DIF}$, the clock must be AC coupled.
3. Specified by characterization.
4. The ESR requirements stated are what is necessary in order to ensure that the Oscillator circuitry has no start up issues. However, lower ESR values for the crystal might be necessary in order to stay below the maximum power dissipation requirements for that crystal.

## Output Characteristics

2.375V ≤ $V_{DD}$ ≤ 3.45V, 1.425V ≤ $V_{DDO}$ ≤ $V_{DD}$, -40°C ≤ TA ≤ 85°C, Differential inputs. Typical values represent most likely parametric norms at $V_{DD}$ = $V_{DDO}$ = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured. Test conditions : $F_{Input}$ = 100MHz, $C_L$ = 5pF in parallel with 50Ω unless otherwise stated.

**Table 10. Output Characteristics**

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| Output Skew | $t_{SK(O)}$ | Measured between outputs(CLKOUTm to CLKOUTn) | | 6 | 25 | ps | 2 |
| Propagation Delay CLKIN to CLKOUT | $t_{PD}$ | $C_L$ = 5 pF, $R_L$ = 50 Ω<br>$V_{DD}$ = 3.3 V; $V_{DDO}$ = 3.3 V | 0.85 | 1.4 | 2.2 | ns | |
| | | $C_L$ = 5 pF, $R_L$ = 50 Ω<br>$V_{DD}$ = 2.5 V; $V_{DDO}$ = 1.5 V | 1.1 | 1.8 | 2.8 | | |
| Part-to-Part Skew | $t_{SK(PP)}$ | $C_L$ = 5 pF, $R_L$ = 50 Ω<br>$V_{DD}$ = 3.3 V; $V_{DDO}$ = 3.3 V | | | 350 | ps | 2,3 |
| | | $C_L$ = 5 pF, $R_L$ = 50 Ω<br>$V_{DD}$ = 2.5 V; $V_{DDO}$ = 1.5 V | | | 600 | | |
| Output Frequency | $F_{OUT}$ | | | | 200 | MHz | 4 |
| Rise/Fall Time | $t_R$ / $t_F$ | $V_{DD}$ = 2.5 V, $V_{DDO}$ = 1.5 V, $C_L$ = 10 pF | | 210 | | ps | 5 |
| | | $V_{DD}$ = 2.5 V, $V_{DDO}$ = 1.8 V, $C_L$ = 10 pF | | 230 | | | |
| | | $V_{DD}$ = 3.3 V, $V_{DDO}$ = 1.8 V, $C_L$ = 10 pF | | 250 | | | |
| | | $V_{DD}$ = 2.5 V, $V_{DDO}$ = 2.5 V, $C_L$ = 10 pF | | 275 | | | |
| | | $V_{DD}$ = 3.3 V, $V_{DDO}$ = 3.3 V, $C_L$ = 10 pF | | 315 | | | |
| Output High Voltage | $V_{OH}$ | | $V_{DDO}$-0.1 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | | 0.1 | V | |
| Output Resistance | $R_{CLKOU}$ | | | 50 | | ohm | |

1. AC Parameters for CMOS are dependent upon output capacitive loading.
2. Parameter specification is only valid for equal loading of all outputs.
3. Part-to-Part skew is calculated as the difference between the fastest and slowest $t_{PD}$ across multiple devices.
4. Specified by characterization.
5. 20%~80%.

## Additive Jitter Characteristics

**Table 11. Additive Jitter Characteristics**

Characterized using RS2CB00105 Performance when VDD= 3.3V. Outputs not under test are terminated to 50Ω.

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|---|
| Additive phase jitter | $t_{jitter}$ | 12 kHz to 5 MHz, $f_{out}$ = 50 MHz | | 50 | | fs rms | 1 |
| | | 12 kHz to 20 MHz, $f_{out}$ = 156.25 MHz | | 30 | | | |

1. CMOS input slew rate ≥ 2 V/ns,CL = 5 pF.

## Typical Characteristics

$V_{DD}$ = $V_{DDO}$ = 3.3V, TA = 25°C, $C_L$ = 5pF, CLKIN driven differentially, input slew rate ≥ 2V/ns.

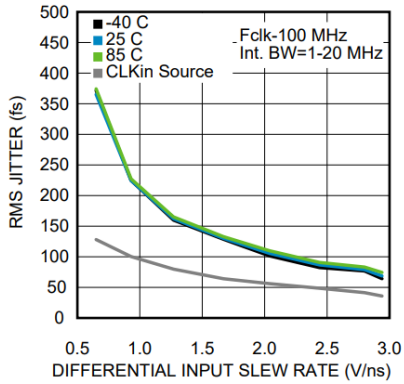



**Figure 1. RMS Jitter vs. CLKin Slew Rate @ 100 MHz**

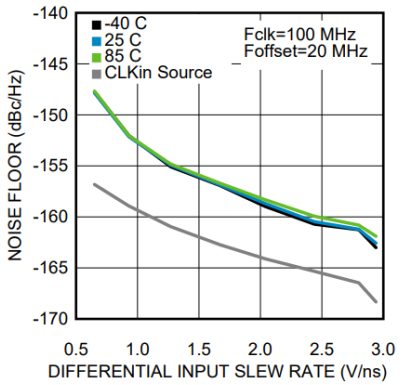
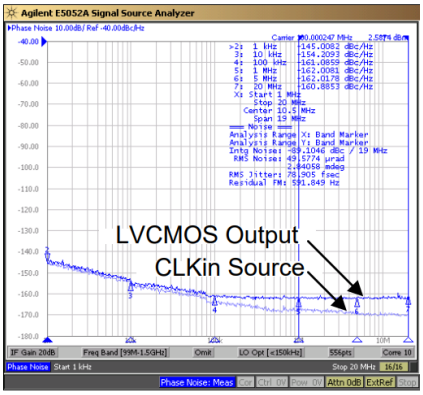



**Figure 2. Noise Floor vs. CLKin Slew Rate @ 100 MHz**




Test conditions: LVCMOS Input, slew rate ≥ 2 V/ns, $C_L$ = 5 pF in parallel with 50 Ω, BW = 1 MHz to 20 MHz

**Figure 3. LVCMOS Phase Noise @ 100 MHz**

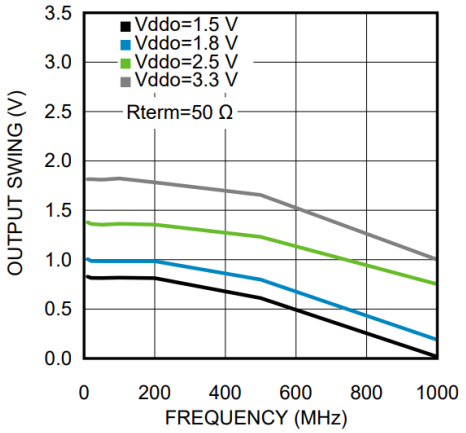



**Figure 4. LVCMOS Output Swing vs. Frequency**

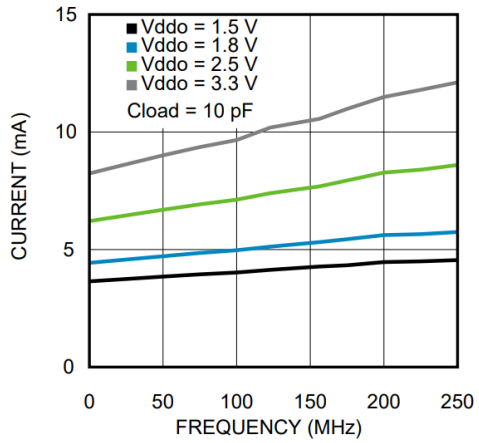



**Figure 5. Iddo per Output vs Frequency**

# Feature Description

## $V_{DD}$ and $V_{DDO}$ Power Supplies

Separate core and output supplies allow the output buffers to operate at the same supply as the $V_{DD}$ core supply (3.3V or 2.5 V) or from a lower supply voltage (3.3V, 2.5V, 1.8V, or 1.5V). Compared to single-supply operation, dual supply operation enables lower power consumption and output-level compatibility.

Bank A (CLKOUT0 and CLKOUT1) and Bank B (CLKOUT2 to CLKOUT4) may also be operated at different $V_{DDO}$ voltages, provided neither $V_{DDO}$ voltage exceeds $V_{DD}$.

**NOTE**

1.Care should be taken to ensure the $V_{DDO}$ voltage does not exceed the $V_{DD}$ voltage to prevent turning-on the internal ESD protection circuitry.

2.**DO NOT DISCONNECT OR GROUND ANY OF THE $V_{DDO}$ PINS** because the $V_{DDO}$ pins are internally connected within an output bank.

# Clock Input

### CLKIN/CLKIN*

The RS2CB00105 has a differential input (CKLIN/CLKIN*) which can be driven single-ended or differentially. It can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, or other differential and single ended signals that meet the input requirements in *Input Characteristics* and when using differential signals with $V_{CM}$ outside of the acceptable range for the specified $V_{SW\_DIF}$, the clock must be AC coupled. Refer to *Clock Input* for more details on driving the RS2CB00105 inputs.

In the event that a Crystal mode is not selected and the CLKIN pins do not have an AC signal applied to them, Table 13 following will be the state of the outputs.

**Table 13. CLKIN Input vs. Output States**

| CLKIN | CLKIN* | Output State |
|---|---|---|
| Open | Open | Logic Low |
| Logic Low | Logic Low | Logic Low |
| Logic High | Logic Low | Logic High |
| Logic Low | Logic High | Logic Low |

### OSCIN/OSCOUT

The RS2CB00105 has a crystal oscillator which will be powered up when OSCIN is selected. Alternatively, OSCIN may be driven by a single ended clock, up to 200 MHz, instead of a crystal. Refer to *Crystal Interface* for more information. If Crystal mode is selected and the pins do not have an AC signal applied to them, Table 14 will be the state of the outputs. If Crystal mode is selected an open state is not allowed on OSCIN, as the outputs may oscillate due to the crystal oscillator circuitry.

**Table 14. OSCIN Input vs. Output States**

| OSCIN | Output State |
|---|---|
| Open | Not Allowed |
| Logic Low | Logic High |
| Logic High | Logic Low |

## Clock Output

The RS2CB00105 has 5 LVCMOS outputs.

**Output Enable Pin**

When the output enable pin is held High, the outputs are enabled. When it is held Low, the outputs are held in a Low state as shown in Table 4.

The OE pin is synchronized to the input clock to ensure that there are no runt pulses. When OE is changed from Low to High, the outputs will initially have an impedance of about 400Ω to ground until the second falling edge of the input clock and starting with the second falling edge of the input clock, the outputs will buffer the input. If the OE pin is taken from Low to High when there is no input clock present, the outputs will either go high or low and stay a that state; they will not oscillate. When the OE pin is taken from High to Low the outputs will be Low after the second falling edge of the clock input and then will go to a Disabled (Hi-Z) state starting after the next rising edge.

**Using Less than Five Outputs**

Although the RS2CB00105 has 5 outputs, not all applications will require all of these. In this case, the unused outputs should be left floating with a minimum copper length to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

**NOTE**

1.For best soldering practices, the minimum trace length should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins.This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

# Applications

## Clock Input

The RS2CB00105 has a differential input (CLKIN/CLKIN*) that can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, and other differential and single ended signals that meet the input requirements specified in *Input Characteristics*. The device can accept a wide range of signals due to its wide input common mode voltage range ($V_{CM}$) and input voltage swing ($V_{SW\_DIF}$)/dynamic range. AC coupling may also be employed to shift the input signal to within the $V_{CM}$ range.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have a high slew rate of 2V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection.

While it is recommended to drive the CLKIN/CLKIN* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKIN pins listed in the *Input Characteristics*. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. The CLKIN input has an internal bias voltage of about 1.4V, so the input can be AC coupled as shown in Figure 6. The output impedance of the LVCMOS driver plus Rs should be close to 50Ω to match the characteristic impedance of the transmission line and load termination.

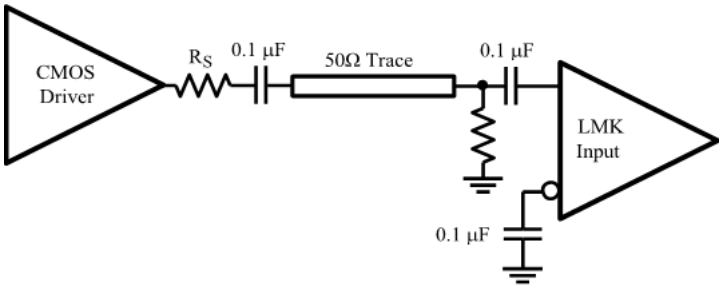



**Figure 6. Preferred Configuration: Single-Ended LVCMOS Input, AC Coupling**

A single-ended clock may also be DC coupled to CLKIN as shown in Figure 7. A 50Ω load resistor should be placed near the CLKIN input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKIN, CLKIN* should be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage should be within the specified input common voltage ($V_{CM}$) range. This can be achieved using external biasing resistors in the kΩ range ($R_{B1}$ and $R_{B2}$) or another low- noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

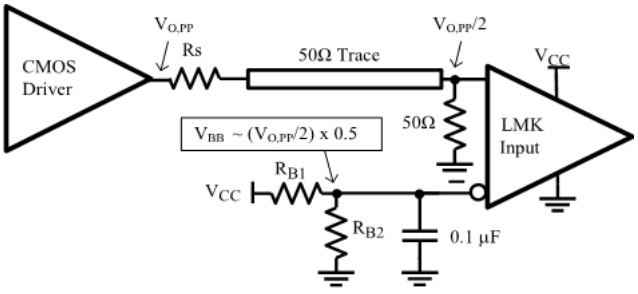



**Figure 7. Single-Ended LVCMOS Input, DC Coupling With Common Mode Biasing**

If the crystal oscillator circuit is not used, it is possible to drive the OSCIN input with an single-ended external

clock as shown in Figure 8. The input clock should be AC coupled to the OSCIN pin, which has an internally generated input bias voltage, and the OSCOUT pin should be left floating. While OSCIN provides an alternative input to multiplex an external clock, it is recommended to use either differential input (CLKIN) since it offers higher operating frequency, better common mode, improved power supply noise rejection, and greater performance over supply voltage and temperature variations.

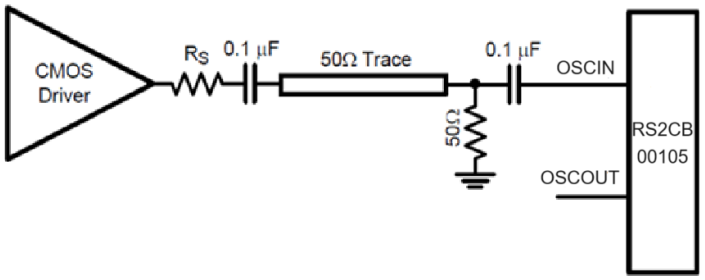



**Figure 8. Driving OSCIN With a Single-Ended External Clock**

## Clock Output

The RS2CB00105 LVCMOS driver output impedance (Ro) is nominally 50 ohms and well-matched to drive a 50 ohm transmission line (Zo), as shown as below. If driving a transmission line with higher characteristic impedance than 50 ohms, a series resistor (Rs) should be placed near the driver to provide source termination, where Rs = Zo – Ro.

The RS2CB00105 has two output banks, Bank A and Bank B, which are separately powered by independent VDDO supply pins. The VDDO supply pins for Bank A and Bank B are not connected together internally, and may be supplied with different voltages. This allows the RS2CB00105 outputs to easily interface to multiple receivers with different input threshold or input supply voltage (VDDI) requirements without the need for additional voltage divider networks.

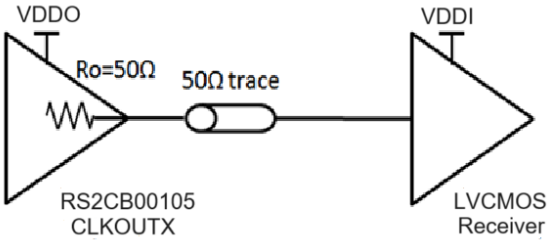



**Figure 9. RS2CB00105 Output Termination**

## Crystal Interface

The RS2CB00105 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 15.

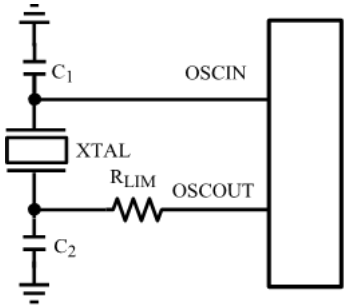



**Figure 15. Crystal Interface**

The value of capacitor and resistor depend on the crystal. Each crystal is specified with a load capacitance and resistor is used to avoid over driving the crystal.

The example crystal specifications are given in Table 15.

**Table 15. Example 25-MHz Crystal Electrical Specifications**

| NO. | Item | Symbol | Electrical Specification | | | |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | Units |
| 1 | Nominal Frequency | F0 | | 25 | | MHz |
| 2 | Mode of Vibration | | | Fundamental | | |
| 3 | Frequency Tolerance | ΔF/F0 | –15 | | 15 | ppm |
| 4 | Load Capacitance | CL | | 9 | | pF |
| 5 | Drive Level | DL | | 100 | 300 | μW |
| 6 | Equivalent Series Resistance | R1 | | 9 | 50 | Ω |
| 7 | Shunt Capacitance | C0 | | 2.1 ± 15% | | pF |
| 8 | Motional Capacitance | C1 | | 9.0 ± 15% | | fF |
| 9 | Motional Inductance | L | | 4.6 ± 15% | | mH |
| 10 | Frequency Stability | TC | –20 | | 20 | ppm |
| 11 | C0/C1 Rate | | | | 250 | |

Based on the OSCIN shunt capacitance and stray capacitance, C1 and C2 are chosen as 6.8pF to make the load capacitance (CL) to be 9pF. Suggested value of RLIM is 1.5kΩ.

# Power Supply Recommendations

## Power Supply Filtering

It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

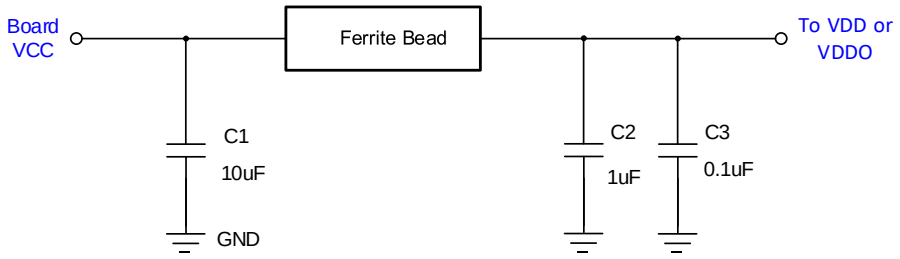
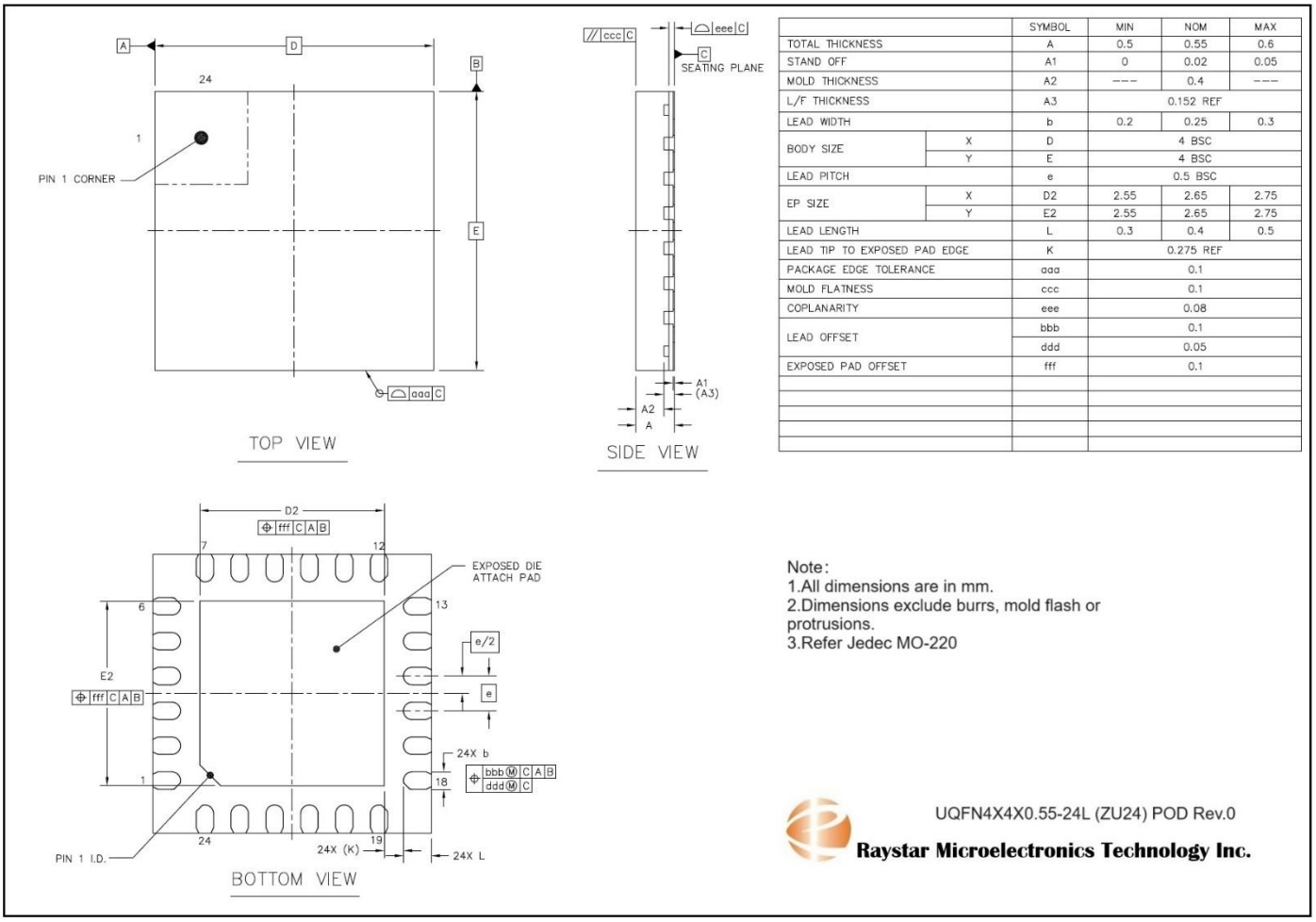



**Figure 16. Power-Supply Decoupling**

# Package Information

## QFN-24L




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.5 | 0.55 | 0.6 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.4 | --- |
| L/F THICKNESS | | A3 | | 0.152 REF | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | | 4 BSC | |
| | Y | E | | 4 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | D2 | 2.55 | 2.65 | 2.75 |
| | Y | E2 | 2.55 | 2.65 | 2.75 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.275 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

UQFN4X4X0.55-24L (ZU24) POD Rev.0
**Raystar Microelectronics Technology Inc.**

## Revision History

| Revision | Description | Date |
|---|---|---|
| 0.9 | 1. Preliminary release | 2024/06/19 |
| 1.0 | 1. Initial release | 2026/06/09 |