Features

- 3.3V Supply Voltage
- Crystal/CMOS Input: 25 MHz
- Four Differential Low-Power HCSL Outputs with On-Chip Termination
- Default Z_{OUT} = 85Ω
- Two reference CMOS Outputs
- Programmable Slew Rate and Output Amplitude for Each Output
- Selectable 0%, -0.3%, or -0.5% Spread on Differential Outputs
- Differential Output-To-Output Skew <60ps
- Very-Low Jitter Outputs a Differential phase Jitter
  - < 0.3ps RMS, SSC off
  - < 1.5ps RMS, SSC on
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device
- TQFN-32L package
- -40 to +125°C temperature operation
- AEC-Q100 qualified, Automotive Grade 1support; PPAP capable, and manufactured in IATF 16949 certified facilities
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Applications

- PCI-e system
- High-performance Computing
- Switch/Router
- Gigabit Ethernet
- OTN Equipment
- Network Line Cards
- Data Center/Storage

Description

The RS2CG282Q is a 2-output differential Low-Power HCSL Outputs and 2-CMOS outputs, very-low-power PCIe Gen1~Gen7 clock generator.

It uses a 25MHz crystal or CMOS reference as an input to generate the 100MHz low-power differential LP-HCSL outputs with on-chip terminations and 2 channels 25MHz LVCMOS buffered reference outputs are provided to serve as a low-noise reference for other circuitry.

It uses RSM's proprietary PLL design to achieve very-low jitter that meets PCIe Gen1/~Gen7 requirements. It also provides various options, such as different slew rate and amplitude through SMBUS, so users can easily configure the device to get the optimized performance for their individual boards. The device also supports selectable spread spectrum options to reduce EMI for various applications.

Order information

Part Number	Package	Description
RS2CG282QZHE	TQFN-32L	5x5x0.75mm
RS2CG282QZLBE	QFN-32L	4x4x0.85mm

Functional Block Diagram

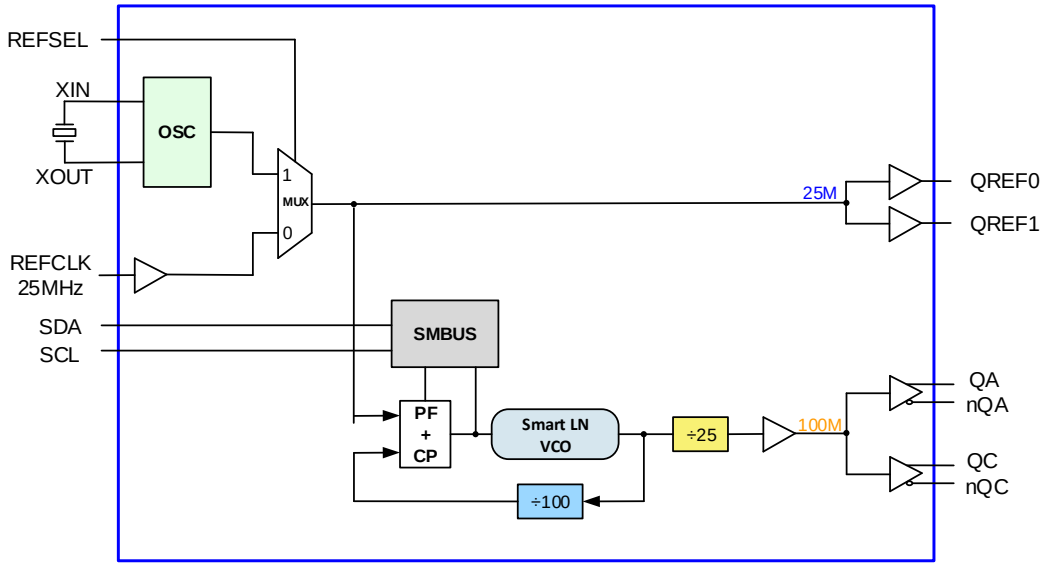

Figure 1. RS2CG282Q Block Diagram

Pin Configuration

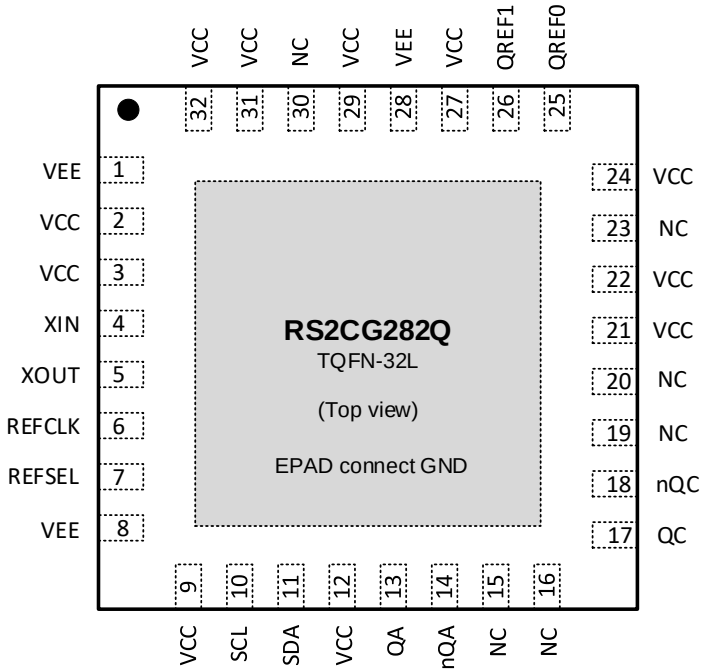

Figure 2. Pin assignment

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 8, 28	V_{EE}	Power		Negative supply pins (GND).
2, 3, 9, 12, 21,22,24,27, 29,31,32	V_{CC}	Power		Power supply Pins 2,27 – power supply connection for the 25MHz LVCMOS outputs Pin 3 – power supply connection for the crystal oscillator Pin 9,12,21,22,24 – power supply connection for the LP-HCSL differential outputs Pins 29 – power supply connection for the divider Pin 31,32 – power supply connection for the PLL
25,26	QREF0, QREF1	Output		Single-ended outputs. 3.3V LVCMOS/LVTTL reference levels.
4,5	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
6	REFCLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
7	REFSEL	Input	Pullup	Reference select pin. When HIGH, selects crystal. When LOW, selects REFCLK. LVCMOS/LVTTL interface levels.
10,11	SCL, SDA	I/0		SMBUS communication
23,30	NC			No connect.
13,14	QA, nQA	Output		Differential output pair. LP-HCSL interface levels.
15,16	NC			No connect.
17,18	QC, nQC	Output		Differential output pair. LP-HCSL interface levels.
19,20	NC			No connect.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
C_{IN}	Input Capacitance		Crystal Not Included		2		pF
C_{PD}	Power Dissipation Capacitance (per output)	QREF [0:1]	V_{CC} = 3.6V		6		pF
R_{PU}	Input Pullup Resistor				51		kΩ
R_{PD}	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QREF [0:1]			33		Ω

Table 3. REFSEL Function

REFSEL	Input Source
0	REFCLK
1(default)	XIN, XOUT

Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, VDDxx .....–0.5V to +4.6V
Input Voltage .....–0.5V to VDD+0.5V, not exceed 4.6V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 4000V
Max Junction Temperature…….....+125ºC

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
T_A	Ambient air temperature	-40		125	°C

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DC Electrical Characteristics

Table 4. Power Supply DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
VCC	Power Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No Load			200	mA

Table 5. LVCMOS DC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{IH}	Input High Voltage	REFSEL	2		VCC + 0.3	V
		REFCLK	VCC - 0.4			V
V_{IL}	Input Low Voltage	REFSEL	-0.3		0.8	V
		REFCLK			0.4	V

Table 6. LVCMOS DC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C.

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
I_{IH}	Input High Current	REFCLK	VCC = VIN = 3.6V			150	µA
		REFSEL	VCC = VIN = 3.6V			5	µA
I_{IL}	Input Low Current	REFCLK	VCC = 3.6V, VIN = 0V	-5			µA
		REFSEL	VCC = 3.6V, VIN = 0V	-150			µA
V_{OH}	Output High Voltage;		VCC = 3.3V ± 0.3V	2.3			V
V_{OL}	Output Low Voltage;		VCC = 3.3V ± 0.3V			0.8	V

Table 7. LP-HCSL DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{OH}	Output High Voltage		660		850	mV
V_{OL}	Output Low Voltage		-150		150	mV
Vomax	Output Maximum Voltage			820	1150	mV
Vomin	Output Minimum Voltage		-300	-42		mV
Voc	Output Cross Voltage		250	380	550	mV

Table 8. Crystal Characteristics

Parameter	Test Conditions	MIN	TYP	MAX	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 9. LP-HCSL AC Characteristics, Vcc= 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
f_{IN}	Input Frequency			25		MHz
f_{OUT}	Output Frequency	LP-HCSL		100		MHz
T_{jc-c}	Cycle to cycle Jitter			20	60	ps
tsk(o)	Output Skew; NOTE 2, 3	Measured on the Rising Edge			50	ps
t_R / t_F	Slew rate	+/-150mV window		3		V/ns
ODC	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

Table 10. AC Characteristics for Single Side Band Power Levels (LP-HCSL Outputs), VCC = 3.3V ± 0.3V, VEE = 0V, TA = 25°C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
tjPHASE	Integrated Phase Jitter (RMS)	PCIe Gen1 (2.5 GT/s)	15	35	86	ps
		PCIe Gen2 Hi Band (5.0 GT/s)	0.4	0.6	3.0	ps
		PCIe Gen2 Lo Band (5.0 GT/s)	0.2	0.3	3.1	ps
		PCIe Gen3 (8.0 GT/s)	0.15	0.2	1.0	ps
		PCIe Gen4 (16.0 GT/s)	0.15	0.2	0.4	ps
		PCIe Gen5 (32.0 GT/s)	0.06	0.08	0.15	ps
		PCIe Gen6 (64.0 GT/s)	0.03	0.05	0.1	ps
		PCIe Gen7 (128.0 GT/s)	0.01	0.02	0.067	ps

Table 11. LVCMOS AC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C.

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
f_{IN}	Input Frequency				25		MHz
f_{OUT}	Output Frequency				25		MHz
tjit	RMS Phase Jitter (Random)		25MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 5MHz		0.140		ps
$t_{sk(o)}$	Output Skew;	QREF [0:1]	Measured on the Rising Edge			50	ps
PSNR	Power Supply Noise Reduction	Pin 40, (V_{CC})	From DC to 6.25MHz		-80		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%		1.0	1.5	ns
ODC	Output Duty Cycle			45		55	%

Table 12. AC Characteristics for Single Side Band Power Levels (LVCMOS Outputs), VCC = 3.3V ± 0.3V, VEE = 0V, TA = 25°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
φN(1k)	Single-side band phase noise, 1kHz from Carrier	25MHz		-137		dBc/Hz
φN(10k)	Single-side band phase noise, 10kHz from Carrier			-153		dBc/Hz
φ(100k)	Single-side band phase noise, 100kHz from Carrier			-162		dBc/Hz
φN(1M)	Single-side band phase noise, 1MHz from Carrier			-163		dBc/Hz
φN(5M)	Single-side band phase noise, 5MHz from Carrier			-163		dBc/Hz

SMBus Serial Data Interface

RS2CG282Q is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below. Read and write block transfers can be stopped after any complete byte transfer

Table 13. Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	0	0/1

Table 14. How to Write

1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit		8 bit	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	……	Data Byte (N+X-1)	Ack	Stop bit

Table 15. How to Read

1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	8 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Add.	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bit	1 bit	1 bit
……..	Data Byte (N+X-1)	NAck	Stop bit

Table 16. Output Enable Control 0

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7			RW			1
Bit 6			RW			1
Bit 5			RW			1
Bit 4			RW			1
Bit 3	OE_OUTA		RW	Disable Output	Enable Output	1
Bit 2			RW			1
Bit 1	OE_OUTC		RW	Disable Output	Enable Output	1
Bit 0			RW			1

Table 17. Output status Control 1

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SLEW RATE OF HCSL	HCSL SLEW RATE CONTROL	RW	Slow setting	Fast setting	0
Bit 6	STOP1	HCSL stop mode control	RW	00=low/low; 01=hiz/hiz; 10=high/low; 11=low/high		0
Bit 5	STOP0		RW			0
Bit 4	HCSL PD	HCSL PD MODE	RW	Normal	PD	0
Bit 3						0
Bit 2						0
Bit 1						0

Bit 0	REF HIZ	Output REF CMOS HIZ MODE	RW	Normal	HIZ	0

Table 18. Reserved

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 19. Reserved

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 20. Reserved

Byte 4	Name		Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 21. Reserved

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 22. Reserved

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 23. Reserved

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW	Pin Low	Pin High	0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 24. Vendor/Revision Identification Control

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	Rev A = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	Vendor ID	R	RSM = 0011		0
Bit 2	VID2		R			0
Bit 1	VID1		R			1
Bit 0	VID0		R			1

Table 25. Device ID Control

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	DID7		R			0
Bit 6	DID6		R			0
Bit 5	DID5	Device ID	R			0
Bit 4	DID4		R			0
Bit 3	DID3		R			0
Bit 2	DID2		R			1
Bit 1	DID1		R			1
Bit 0	DID0		R			1

Table 26. Byte Count Control

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	BC5	Writing to this register configures how many bytes will be read back	RW	Default value is 8		0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Table 27. Reserved

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 28. Reserved

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 29. Reserved

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 30. Reserved

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 31. Reserved

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 32. Reserved

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

Table 33. Reserved

Byte 17	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 34. PWRGD Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			1
Bit 5	Reserved		RW			0

Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 35. Reserved

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

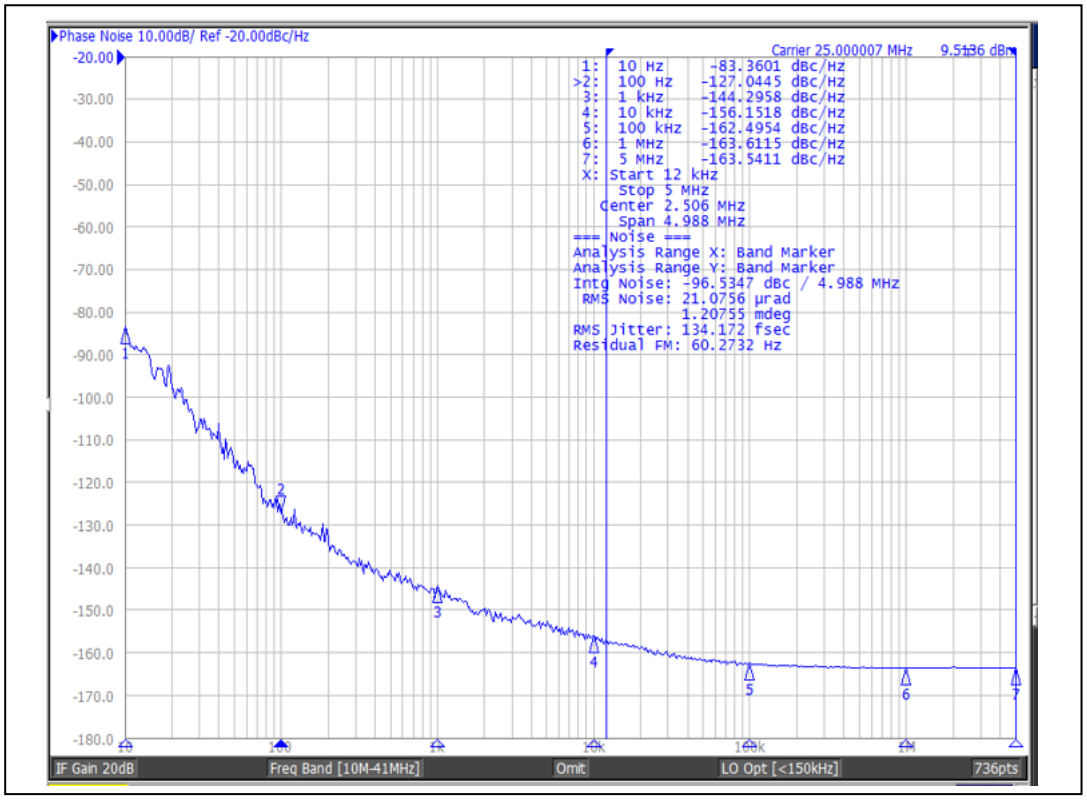
Table 36. SSC Control

Byte 20	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			1
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

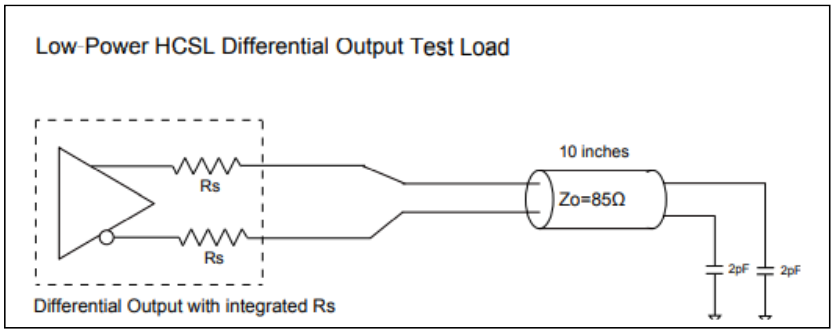
Table 37. SSC and EFUSE Control

Byte 21	Name	Control Function	Type	0	1	Default
Bit 7	SSC_PD	SSC block power down valid if CG is SSC mode	RW	Normal	Power down	0
Bit 6	SSC_EN_SW1	SSC_EN SW control	RW	00 = SSC off 01 = -0.3% SS 10 = -0.3% SS 11 = -0.5% SS		0
Bit 5	SSC_EN_SW0					0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved	Write not allowed	RW	00 = ACCESS0 / ACCESS0 01 = RE / PEB 10 = OUTPUT1 / ACCESS1 11 = OUTPUT0 / ADDR0		0
Bit 0	Reserved		RW			0

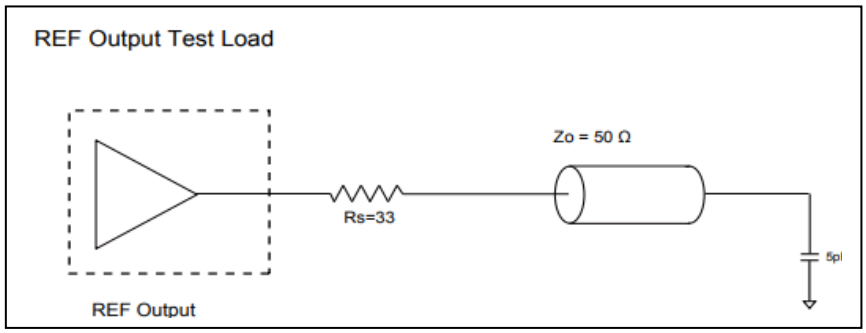
Plots 25MHz LVCMOS Clock (12k to 5MHz)



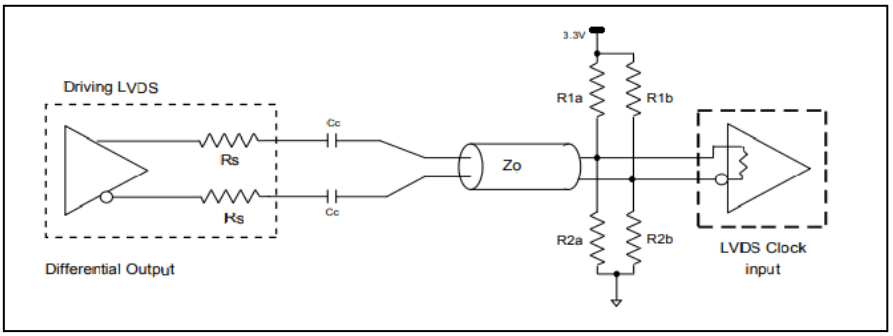
Low-Power HCSL Test Circuit



CMOS REF Test Circuit



Differential Output Driving LVDS



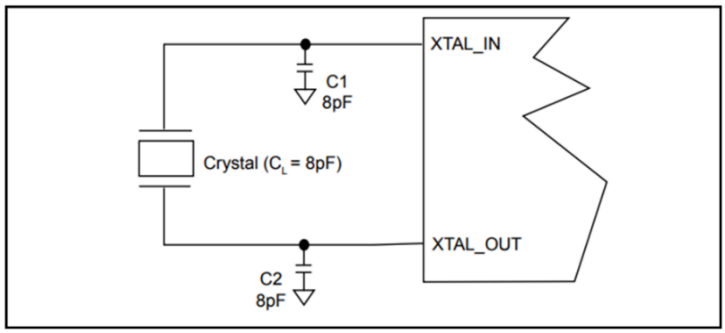
Alternate Differential Output Terminations (Zo = 85Ω)

Component	Receiver with Termination	Receiver without Termination	Unit
R1a, R1b	10,000	130	Ω
R2a, R2b	5600	64	Ω
C_C	0.1	0.1	uF
V_{CM}	1.2	1.2	V

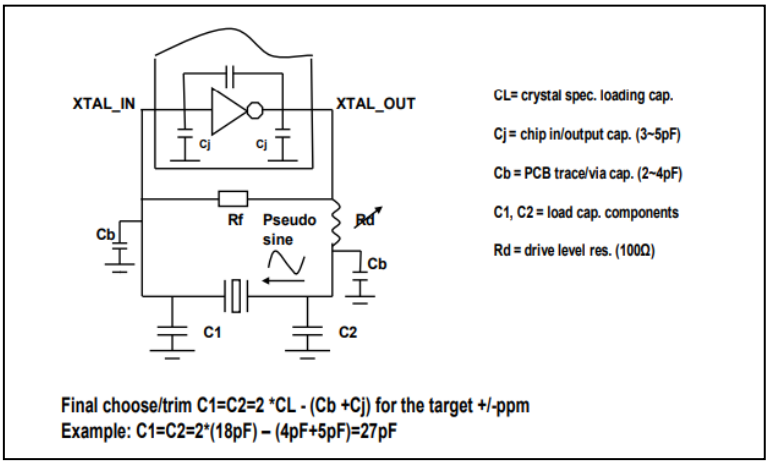
Crystal Circuit Connection

The following diagram shows RS2CG282Q crystal circuit connection with a parallel crystal. For the CL=8pF crystal, it is suggested to use C1=8pF and C2=8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit

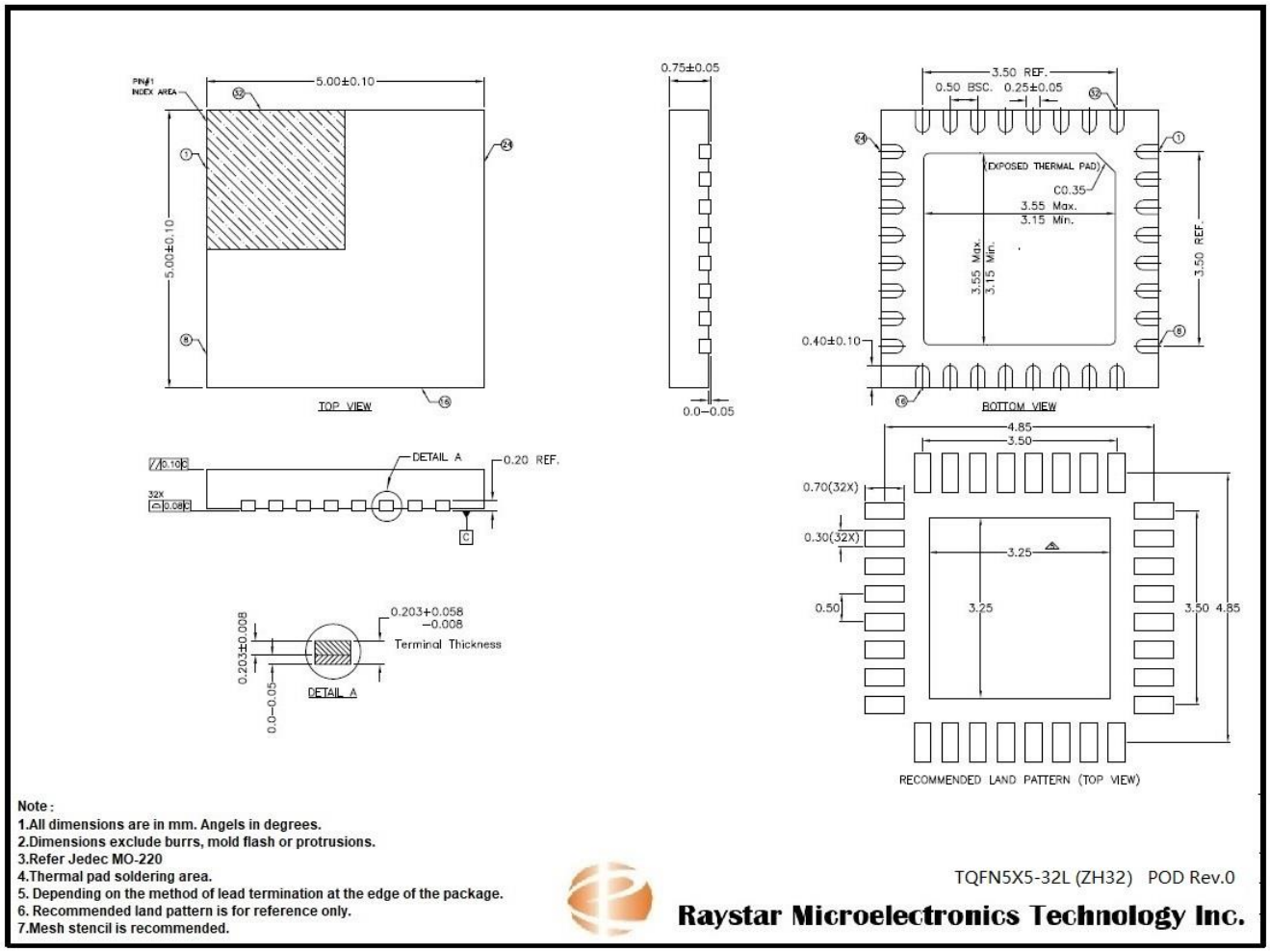


Crystal Capacitor Calculation



Package Information

TQFN-32L

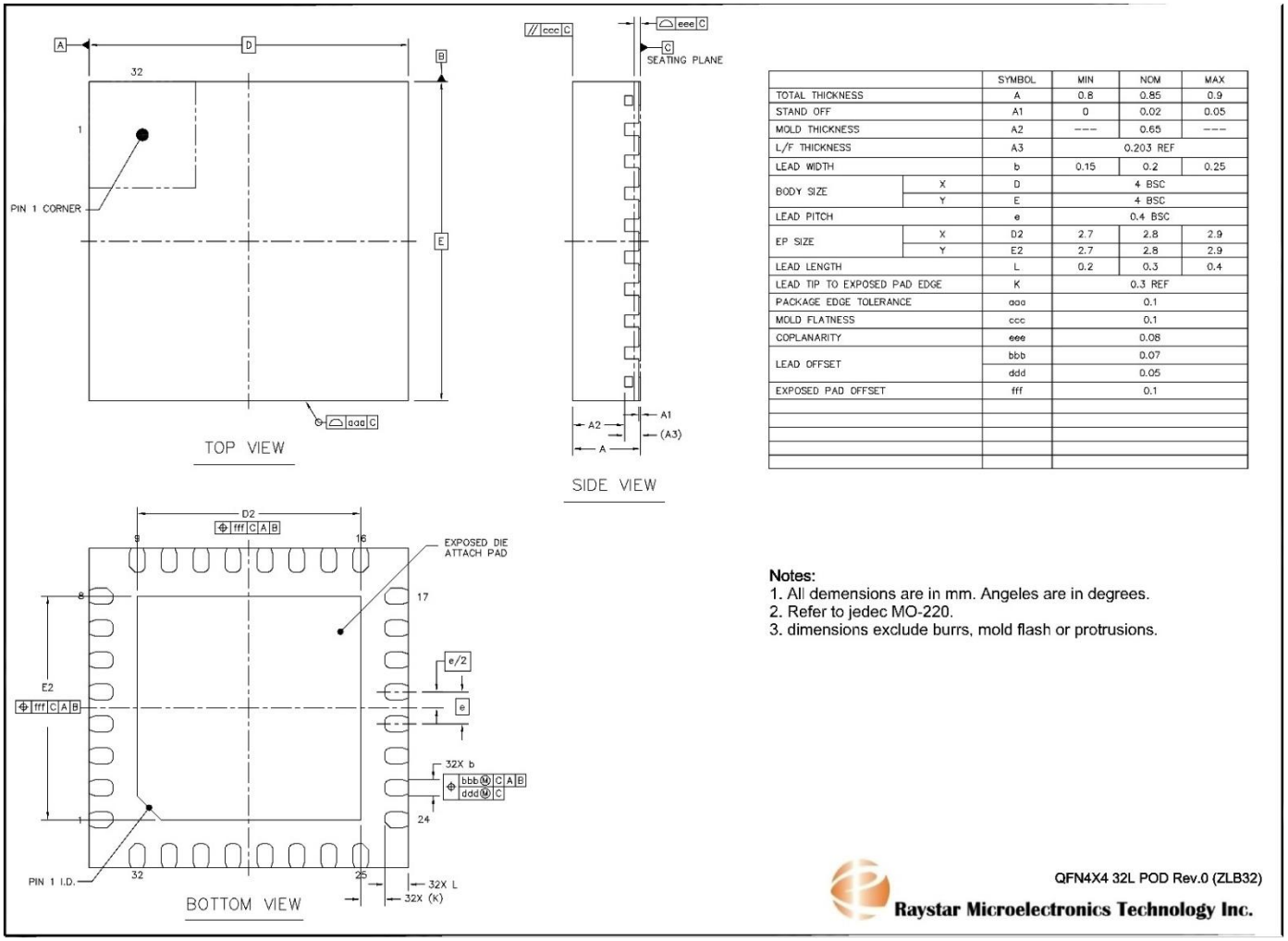


Note :
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220
4.Thermal pad soldering area.
5. Depending on the method of lead termination at the edge of the package.
6. Recommended land pattern is for reference only.
7.Mesh stencil is recommended.

TQFN5X5-32L (ZH32) POD Rev.0

Raystar Microelectronics Technology Inc.

QFN-32L (4x4mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Notes:
1. All demensions are in mm. Angeles are in degrees.
2. Refer to jedec MO-220.
3. dimensions exclude burrs, mold flash or protrusions.

QFN4X4 32L POD Rev.0 (ZLB32)
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary release.	2024/12/18
1.0	1. Add PCIe 7.0 Jitter data 2. Add Part Number RS2CG282QZLBE	2026/03/24