Features

- 1.8/3,3 V Supply Voltage
- Crystal/CMOS input: 25 MHz
- 4 Differential low power HCSL outputs with on-chip termination
- Individual output enable
- Reference CMOS output
- Programmable slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Selectable 0%, -0.25% or -0.5% spread on differential outputs
- Strapping pins or SMBus for configuration
- 3.3V Tolerant SMBus interface support
- Very low jitter outputs
  - Differential cycle-to-cycle jitter <50ps
  - Differential output-to-output skew <60ps
  - PCIe Gen1~Gen7 compliant
  - CMOS REFOUT phase jitter is < 200fs RMS
- Packaging (Pb-free & Green):
  - 32-lead 5×5mm TQFN

Applications

- Cloud/High-performance Computing
- nVME Storage
- Networking
- PCIe switch

Description

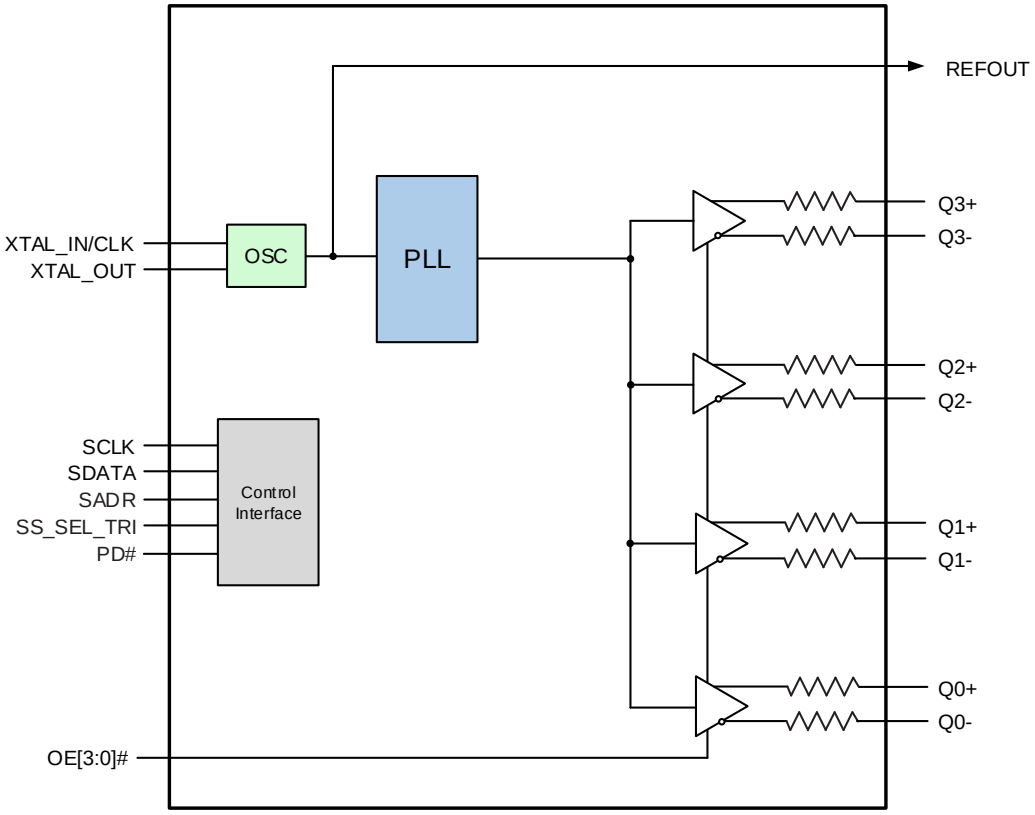
The RS2CG1834 is a 4-output very low power PCIe Gen1~ Gen7 clock generator. It uses 25MHz crystal or CMOS reference as an input to generate the 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 32 external resistors and make layout easier. An additional buffered reference output is provided to serve as a low noise reference for other circuitry.

It uses Raystar' proprietary PLL design to achieve very low jitter that meets PCIeGen1~Gen7 requirements. It also provides various options such as different slew rate and amplitude through strapping pins or SMBUS so that users can configure the device easily to get the optimized performance for their individual boards. The device also supports selectable spread-spectrum options to reduce EMI for various applications.

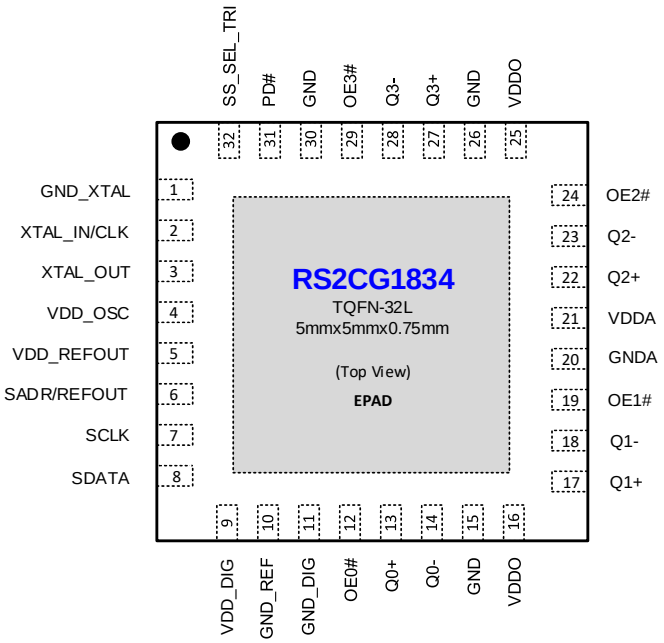
Ordering Information

Part Number	Package	Description
RS2CG1834ZH	TQFN-32L	5 x 5 x 0.75 mm,0.5mm Pitch

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	GND_XTAL	Power		Ground for oscillator circuit
2	XTAL_IN/CLK	Input		Crystal input or CMOS reference input
3	XTAL_OUT	Output		Crystal output
4	VDD_OSC	Power		Power supply for oscillator circuitry, nominal 1.8/3.3V
5	VDD_REFOUT	Power		Power supply for buffered CMOS output
6	SADR/REFOUT	Input/ Output	CMOS	Latch to select SMBus Address or 1.8 LVCMOS REFOUT. This pin has an internal pull-down
7	SCLK	Input	CMOS	SMBUS clock input, 3.3V tolerant
8	SDATA	Input/ Output	CMOS	SMBUS Data line, 3.3V tolerant
9	VDD_DIG	Power		Power supply for digital circuitry, nominal 1.8/3.3V
10	GND_REF	Power		Ground for REFOUT
11	GND_DIG	Power		Ground for digital circuitry
12	OE0#	Input	CMOS	Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	Q0+	Output	HCSL	Differential true clock output
14	Q0-	Output	HCSL	Differential complementary clock output
15,26,30	GND	Power		Ground
16, 25	VDDO	Power		Power supply for differential outputs

Pin #	Pin Name	Type		Description
17	Q1+	Output	HCSL	Differential true clock output
18	Q1-	Output	HCSL	Differential complementary clock output
19	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pull- down.
20	GNDA	Power		Ground for analog circuitry
21	V_{DDA}	Power		Power supply for analog circuitry
22	Q2+	Output	HCSL	Differential true clock output
23	Q2-	Output	HCSL	Differential complementary clock output
24	OE2#	Input	CMOS	Active low input for enabling Q2 pair. This pin has an internal pull- down. 1 =disable outputs, 0 = enable outputs
27	Q3+	Output	HCSL	Differential true clock output
28	Q3-	Output	HCSL	Differential complementary clock output
29	OE3#	Input	CMOS	Active low input for enabling Q3 pair. This pin has an internal pull- down. 1 =disable outputs, 0 = enable outputs
31	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
32	SS_SEL_TRI	Input	Tri-level	Latched select input to select spread spectrum amount at initial power up 1 = -0.5% spread, M = -0.25%, 0 = Spread Off

SMBus Address Selection Table

	SADR	Address	+Read/Write Bit
State of SADR on first application of PD#	0	1101000	X
	1	1101010	X

Power Management Table

PD#	SMBus OE bit	OEn#	Qn+	Qn-
0	X	X	Low	Low
1	1	0	Running	Running
1	1	1	Low	Low
1	0	X	Low	Low

PD#	SMBus Byte3 [4]	REFOUT
0	X	X
1	0	Hiz
1	1	Running

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CG1834 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Supply Voltage	V_{DDX}				3.63	V	1
Input High Voltage	V_{IH}				VDD+0.5	V	2
Input Low Voltage	V_{IL}		-0.5			V	
Storage Temperature	T_S		-65		150	°C	
Junction Temperature	T_J	Maximum operating junction temperature.			125	°C	
Input ESD Protection	ESD	Human Body Model.			2000	V	

1. Operation over these conditions is neither implied nor guaranteed.
2. Maximum VIH is not to exceed maximum VDD.

Recommend Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	MIN	TYP	MAX	Units
VDDA VDDO VDD_REFOUT VDD_DIG	Power Supply Voltage		1.71	1.8/3.3	3.63	V
IDDA	Analog Power Supply Current	All outputs active @100MHz		12	15	mA
IDDO	Power Supply Current for Outputs	All outputs active @100MHz		28	35	mA
IDDA_WL	Analog Power Supply Wake-on- LAN[1] Current	Q outputs off, REF output running		0.4	1	mA
IDDO_WL	Power Supply Wake-on-LAN*1* Current for Outputs	Q outputs off, REF output running		0.04	0.1	mA
IDDA_PD	Analog Power Supply Power Down[2] Current	All outputs off		0.4	1	mA
IDDO_PD	Power Supply Current Power Down[2] for Outputs	All outputs off		0.0005	0.1	mA
TA	Ambient Temperature	Industrial grade	–40		125	°C

Note:

1. Wake-on-LAN mode: PD# = '0' Byte 3, bit 5 = '1'
2. Power down mode: PD# = '0' Byte 3, bit 5 = '0'

Input Electrical Characteristics

Symbol	Parameters	Conditions	MIN	TYP	MAX	Units
R_{pu}	Internal pull up resistance			120		KΩ
R_{dn}	Internal pull down resistance			120		KΩ
C_{XTAL}	Internal capacitance on X_IN and X_OUT pins			5		pF
L_{PIN}	Pin inductance				7	nH

Crystal Characteristic

Parameters	Description	MIN	TYP	MAX	Units
OSC mode	Mode of Oscillation		Fundamental		
FREQ	Frequency		25		MHz
ESR[1]	Equivalent Series Resistance			50	Ω
Cload	Load Capacitance		8		pF
Cshunt	Shunt Capacitance			7	pF
	Drive Level			300	uW

Note:

1. ESR value is dependent upon frequency of oscillation

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	MIN	TYP	MAX	Units
V_{DDSMB}	Nominal bus voltage		1.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.6	V
		SMBus, V_{DDSMB} < 3.3V			0.6	
$I_{SMBSINK}$	SMBus sink current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			400	kHz
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

Spread Spectrum Characteristic

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	MIN	TYP	MAX	Units
f_{MOD}	SS Modulation Frequency	Triangular modulation	30	31.6	33	kHz

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	MIN	TYP	MAX	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	SS_SEL_TRI	0.4V_{DD}	0.5V_{DD}	0.55V_{DD}	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25 V_{DD}	V
I_{IH}	Input High Current	Single-ended inputs, V_{IN} = V_{DD}			30	uA
I_{IL}	Input Low Current	Single-ended inputs, V_{IN} = 0V	-30			uA
I_{IH}	Input High Current	Single-ended inputs with pull up / pull down resistor, V_{IN} = V_{DD}			220	uA
I_{IL}	Input Low Current	Single-ended inputs with pull up / pull down resistor, V_{IN} = 0V	-220			uA
V_{OH}	Output High Voltage	REFOUT, except SMBus; I_{OH} = -2mA	V_{DD} -0.45			V
V_{OL}	Output Low Voltage	REFOUT, except SMBus; I_{OH} = 2mA			0.45	V
R_{OUT}	CMOS Output impedance			20		Ω
C_{IN}	Input Capacitance		1.5		5	pF

LVCMOS AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	MIN	TYP	MAX	Units
f_{INPUT}	Input Frequency	XTAL_IN/CLK		25		MHz
t_{RIN}	Input rise time	Single-ended inputs			5	ns
t_{FIN}	Input fall time	Single-ended inputs			5	ns
t_{STAB}	Clock stablization	From Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1.8	ms
t_{OELAT}	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion	1		3	clocks
t_{PDLAT}	PD# de-assertion	Differential outputs enable after PD# de-assertion		20	300	us
t_{PERIOD}	REFOUT clock period	REFOUT, assume input is at 25MHz		40		ns
f_{ACC}	REFOUT frequency accuracy [1]	REFOUT, long term accuracy to input		0		ppm
t_{SLEW}	REFOUT slew rate [1]	Byte 3 = 1F, 20% to 80% of V_{DDREF}	0.6	1	1.6	V/ns
		Byte 3 = 5F, 20% to 80% of V_{DDREF}	0.75	1.4	2.2	V/ns
		Byte 3 = 9F, 20% to 80% of V_{DDREF}	0.85	1.7	2.7	V/ns
		Byte 3 = DF, 20% to 80% of V_{DDREF}	1.0	1.8	2.9	V/ns
t_{DC}	REFOUT Duty Cycle [1]	VT = VDD /2 V, driven by a Xtal	45	50	55	%

LVCMOS AC Characteristics (Cont.)

Symbol	Parameters	Condition	MIN	TYP	MAX	Units
t_{DCDIS}	REFOUT Duty Cycle Distortion	$V_T = V_{DD}/2$ V, driven by an external source	0	2	4	%
t_{JITCC}	REFOUT cycle-cycle jitter	$V_T = V_{DD}/2$ V, driven by a Xtal		19.1	250	ps
t_{JITPH}	REFOUT phase jitter	12kHz to 5MHz, RMS, driven by a Xtal		0.63	1.5	ps
t_{JITN}	Noise floor	1kHz offset, driven by a Xtal		-129.8	-105	dBc
		10kHz offset to Nyquist, driven by a Xtal		-143.6	-115	dBc

Note:
1. Guaranteed by design and characterization, not 100% tested in production

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	MIN	TYP	MAX	Units
V_{OH}	Output Voltage High [1]	Statistical measurement on single-ended signal using oscilloscope math function	660	784	850	mV
V_{OL}	Output Voltage Low [1]		-150		150	mV
V_{OMAX}	Output Voltage Maximum [1]	Measurement on single ended signal using absolute value		816	1150	mV
V_{OMIN}	Output Voltage Minimum [1]		-300	-42		mV
V_{OSWING}	Output Swing Voltage [1,2,3]	Scope averaging off	300	1634		mV
V_{OC}	Output Cross Voltage [1,2,4]		250	430	550	mV
DVOC	V_{OC} Magnitude Change [1,2,5]			12	140	mV

Note:
1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge
5. The total variation of all Vcross measurements in any particular system. This is a subset of Vcross_min/max allowed.

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	MIN	TYP	MAX	Units
f_{OUT}	Output Frequency			100		MHz
t_{RF}	Slew rate [1,2,3]	Scope averaging on fast setting	2	2.3	4	V/ns
		Scope averaging on slow setting	1.1	1.9	2.9	V/ns
DtRF	Slew rate matching [1,2,4]	Scope averaging on		3		%
t_{DC}	Duty Cycle [1,2]	Measured differentially, PLL Mode	45	50	55	%
t_{SKEW}	Output Skew [1,2]	Averaging on, V_T = 50%		43	60	ps
t_{jc-c}	Cycle to cycle jitter [1,2]			42	50	ps
$t_{STARTUP}$	Start up time				10	ms
t_{LOCK}	PLL lock time				20	ms

Symbol	Parameters	Condition	MIN	TYP	MAX	Units
tjPHASE	Integrated phase jitter (RMS) 1,5,6	PCIe Gen1 (2.5 GT/s)	15	35	86	ps
		PCIe Gen2 Hi Band (5.0 GT/s)	0.4	0.6	3.0	ps
		PCIe Gen2 Lo Band (5.0 GT/s)	0.2	0.3	3.1	ps
		PCIe Gen3 (8.0 GT/s)	0.15	0.2	1.0	ps
		PCIe Gen4 (16.0 GT/s)	0.15	0.2	0.4	ps
		PCIe Gen5 (32.0 GT/s)	0.06	0.08	0.15	ps
		PCIe Gen6 (64.0 GT/s)	0.03	0.05	0.1	ps
		PCIe Gen7 (128.0 GT/s)	0.015	0.03	0.05	ps

Note:
1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. It is measured using a +/-75mV window centered on the average cross point
5. See http://www.pcisig.com for complete specs
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}

Differential Output Clock Periods - Spread Spectrum Disabled [1, 2]

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	-SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+SSC Short-term Avg.Max	-c2c jitter AbsPer Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns

Differential Output Clock Periods - Spread Spectrum Enabled [1, 2]

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	-SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+SSC Short-term Avg.Max	-c2c jitter AbsPer Max	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns

Note:
1. Guaranteed by design and characterization, not 100% tested in production
2. All long term accuracy and clock period specifications are guaranteed assuming REF is trimmed to 25.00MHz

SMBus Interface Information

Write Operation

- Controller (host) sends a start bit
- Controller (host) sends the write address
- RSM clock will acknowledge
- Controller (host) sends the beginning byte location = N
- RSM clock will acknowledge
- Controller (host) sends the byte count = X
- RSM clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- RSM clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

Write Operation			
Controller (Host)			**RSM (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stop bit		

Read Operation

- Controller (host) will send a start bit
- Controller (host) sends the write address
- RSM clock will acknowledge
- Controller (host) sends the beginning byte location = N
- RSM clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- RSM clock will acknowledge
- RSM clock will send the data byte count = X
- RSM clock sends Byte N+X-1
- RSM clock sends Byte 0 through Byte X (if X(H) was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Read Operation			
Controller (Host)			**RSM (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat start		
Slave Address			
RD	Read		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stop bit		

SMBus Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	SADR	0	1/0

Note: SMBus address is latched on SADR pin

Byte 0: Output Enable Register [1]

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved		RW	1		
6	Q3_OE	Q3 output enable	RW	1	Low/Low	Enabled
5	Q2_OE	Q2 output enable	RW	1	Low/Low	Enabled
4	Reserved		RW	1		
3	Q1_OE	Q1 output enable	RW	1	Low/Low	Enabled
2	Reserved		RW	1		
1	Q0_OE	Q0 output enable	RW	1	Low/Low	Enabled
0	Reserved		RW	1		

Note:

1. A low on these bits will override the OE# pins and force the differential outputs to Low/Low states

Byte 1: SS Readback and Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	SSENRB1	SS Enable Readback Bit1	R	Latch	'00' for SS_SEL_TRI = '0', '01' for SS_SEL_TRI = 'M', '11' for SS_SEL_TRI = '1'	
6	SSENRB0	SS Enable Readback Bit0	R	Latch		
5	SSEN_SWCTR	Enable SW control of SS	RW	0	Values in B1[7:6] control SS amount	Values in B1[4:3] control SS amount
4	SSENSW1	SS enable SW control Bit1	RW[1]	0	'00' = SS off, '01' = -0.25% SS, '10' = Reserved, '11' = -0.5% SS	
3	SSENSW0	SS enable SW control Bit0	RW[1]	0		
2	Reserved			1		
1	Amplitude1	Control output applitude	RW	1	'00' = 0.6V, '01' = 0.7V, '10' = 0.8V, '11' = 0.9V	
0	Amplitude0		RW	0		

Note:

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved		RW	1		
6	SLEWRATECTR_Q6	Control slew rate of Q6	RW	1	Slow setting	Fast setting
5	SLEWRATECTR_Q5	Control slew rate of Q5	RW	1	Slow setting	Fast setting
4	Reserved		RW	1		
3	SLEWRATECTR_Q3	Control slew rate of Q3	RW	1	Slow setting	Fast setting
2	Reserved		RW	1		
1	SLEWRATECTR_Q1	Control slew rate of Q1	RW	1	Slow setting	Fast setting
0	Reserved		RW	1		

Byte 3: REF Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	REFSLEWRATE	Slew rate control for REF	RW	0	'00' = 0.9V/ns '01' = 1.3V/ns, '10' = 1.6V/ns, '11' = 1.8V/ns	
6			RW	1		
5	REF_PDSTATE	Wake-on-Lan enable for REF	RW	0	REF = 'Low'	REF = running
4	REF_OE	Output enable for REF	RW	1	REF = "Low'	REF = running
3	Reserved			1		
2	Reserved			1		
1	Reserved			1		
0	Reserved			1		

Byte 4: Reserved

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:0	Reserved					

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	Rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	RSM= 0001	
2	PVID3		R	0		
1	PVID3		R	0		
0	PVID3		R	1		

Byte 6: Device Type/Device ID Register

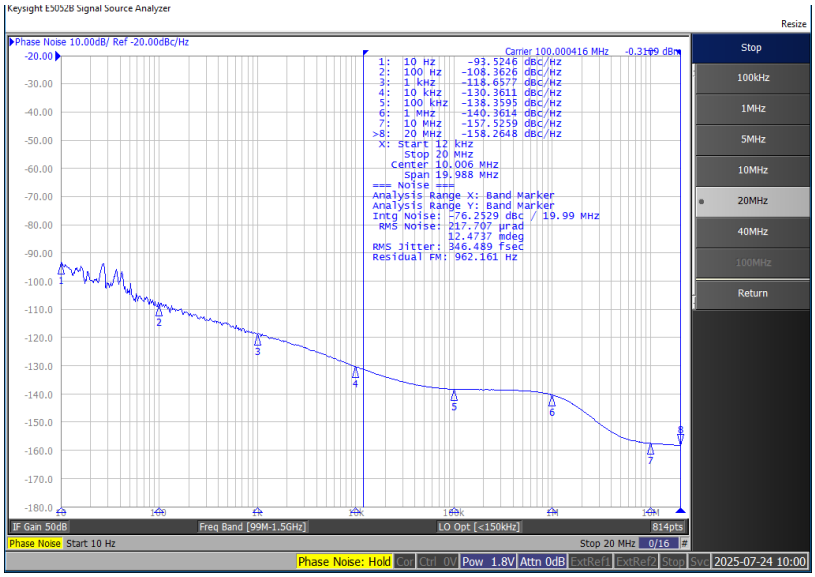
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DTYPE1	Device type	R	0	'00' = CG, '01' = ZDB, '10' = Reserve, '11' = ZDB	
6	DTYPE0		R	0		
5	DID5	Device ID	R	0	000100 binary, 04Hex	
4	DID4		R	0		
3	DID3		R	0		
2	DID2		R	1		
1	DID1		R	0		
0	DID0		R	0		

Byte 7: Byte Count Register

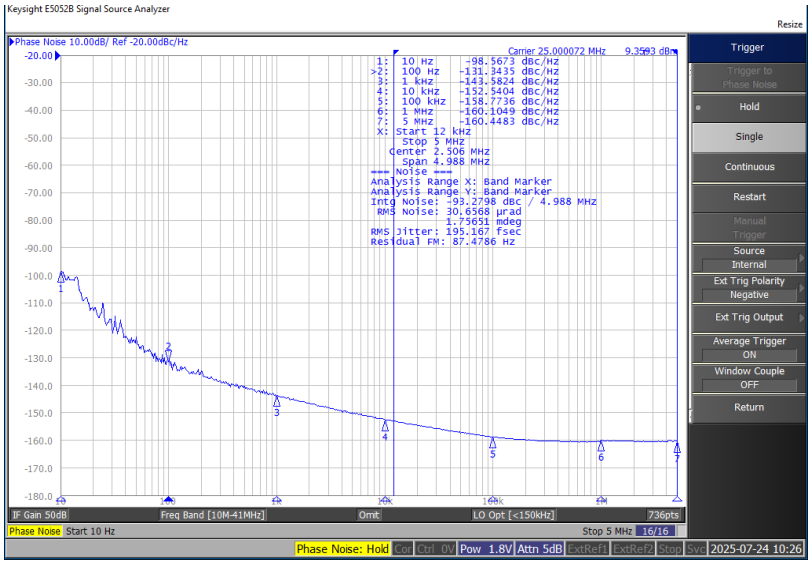
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Phase Jitter Parameter

100MHz HCSL Clock (12k to 20MHz)



25MHz CMOS Clock



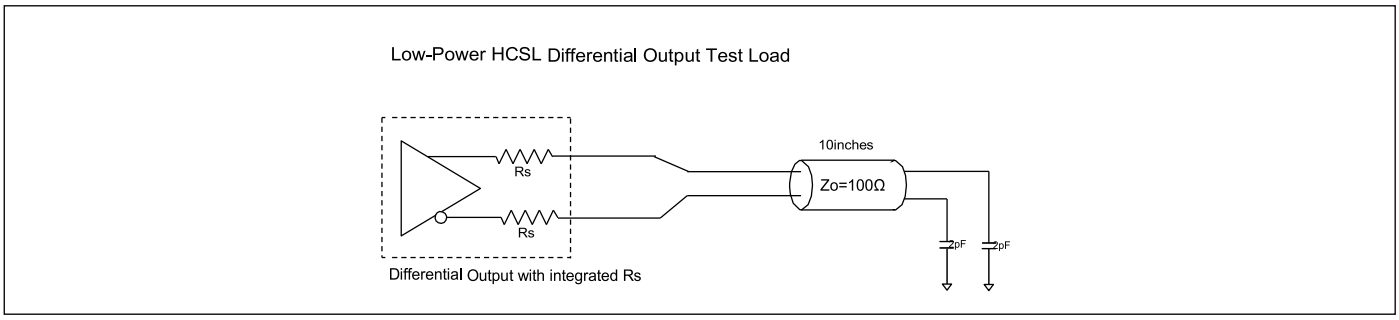


Figure 1. Low Power HCSL Test Circuit

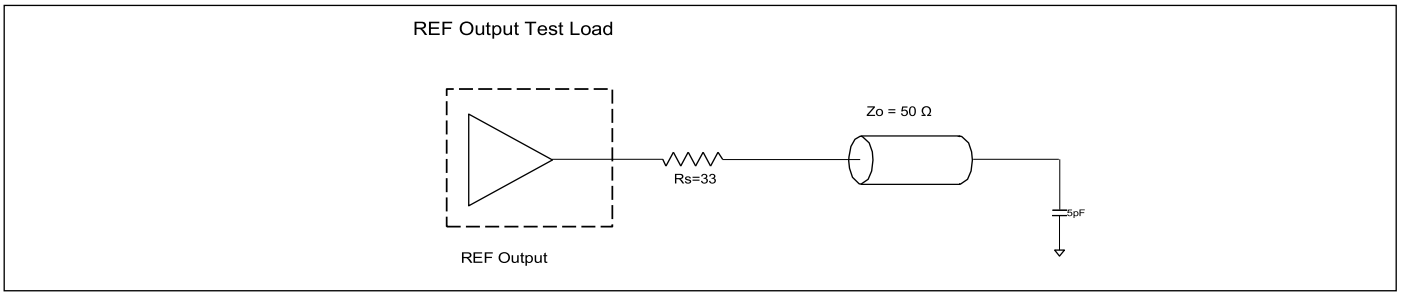


Figure 2. CMOS REF Test Circuit

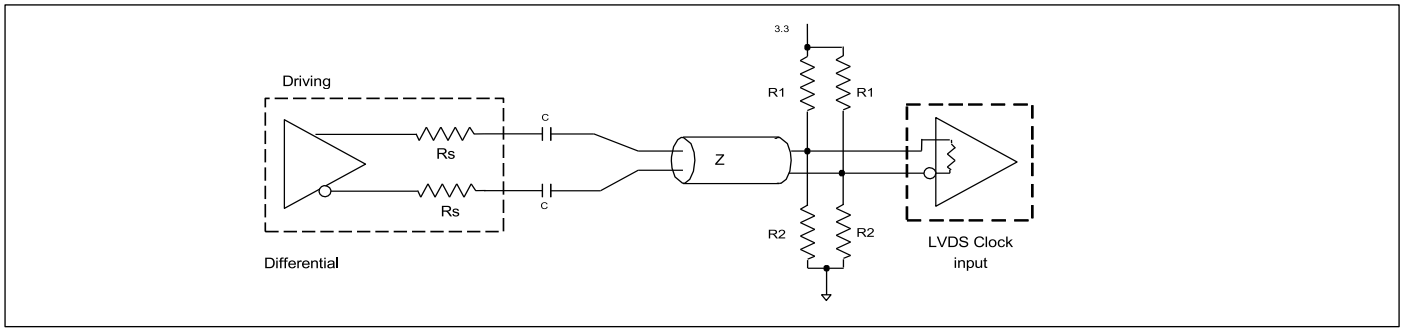


Figure 3. Differential Output driving LVDS

Alternate Differential Output Terminations

Component	Receiver with termination	Receiver without termination	Unit
R_{1a}, R_{1b}	10,000	140	Ω
R_{2a}, R_{2b}	5,600	75	Ω
C_C	0.1	0.1	uF
V_{CM}	1.2	1.2	V

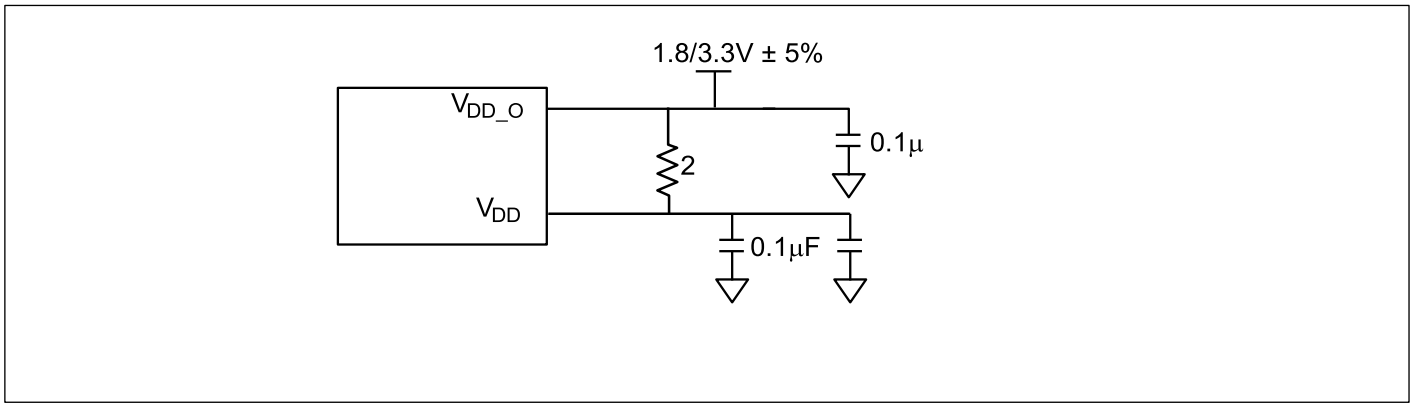


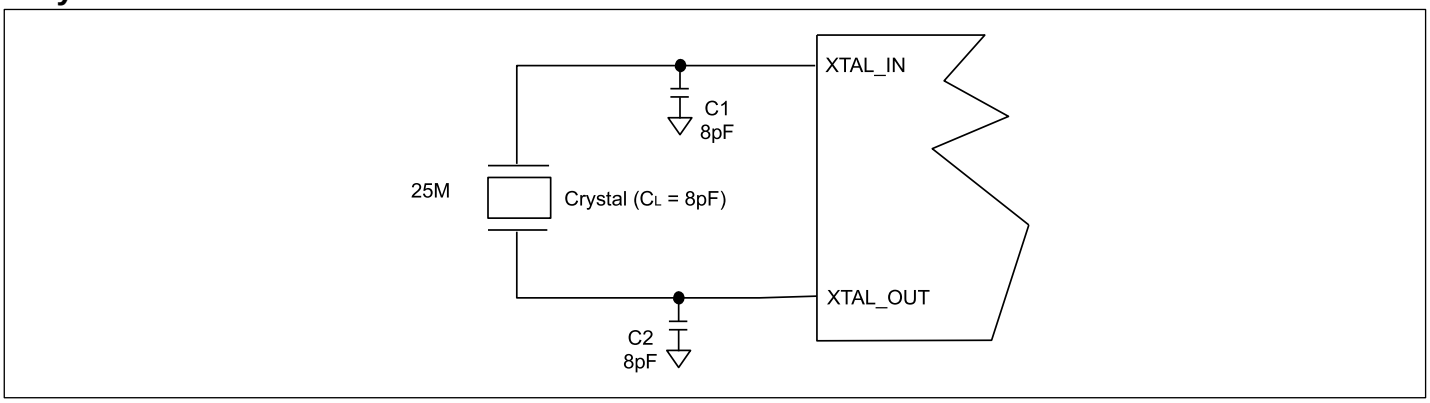
Figure 4. Power Supply Filter

Applications

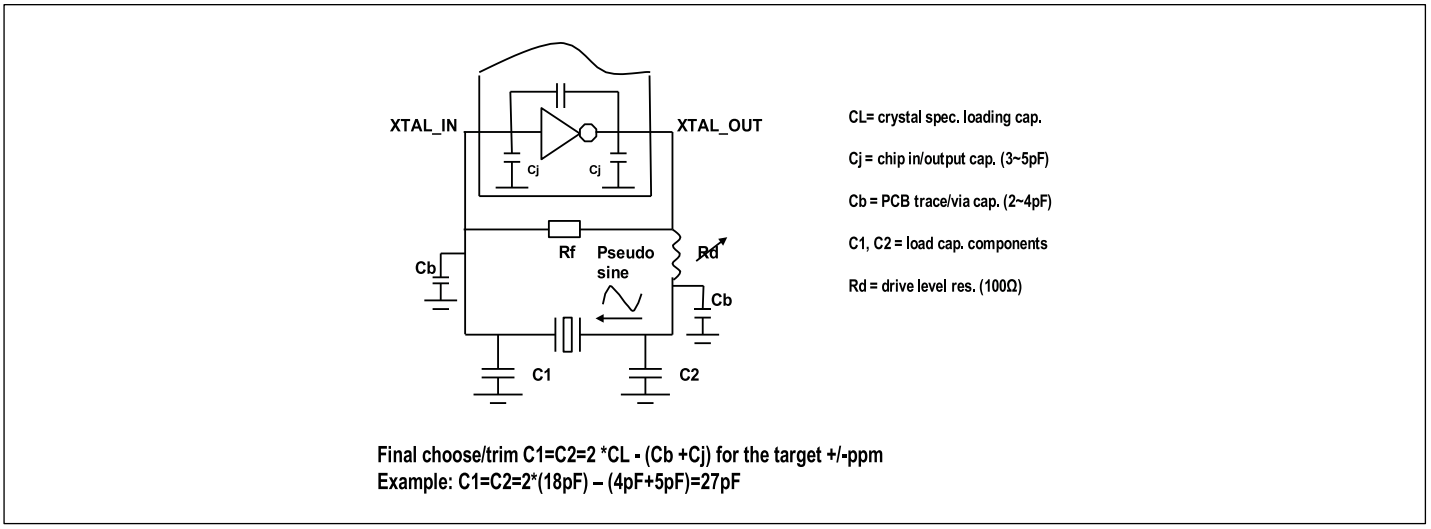
Crystal circuit connection

The following diagram shows RS2CG1834 crystal circuit connection with a parallel crystal. For the CL=8pF crystal, it is suggested to use C1=8pF, C2=8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit



Crystal Capacitor Calculation

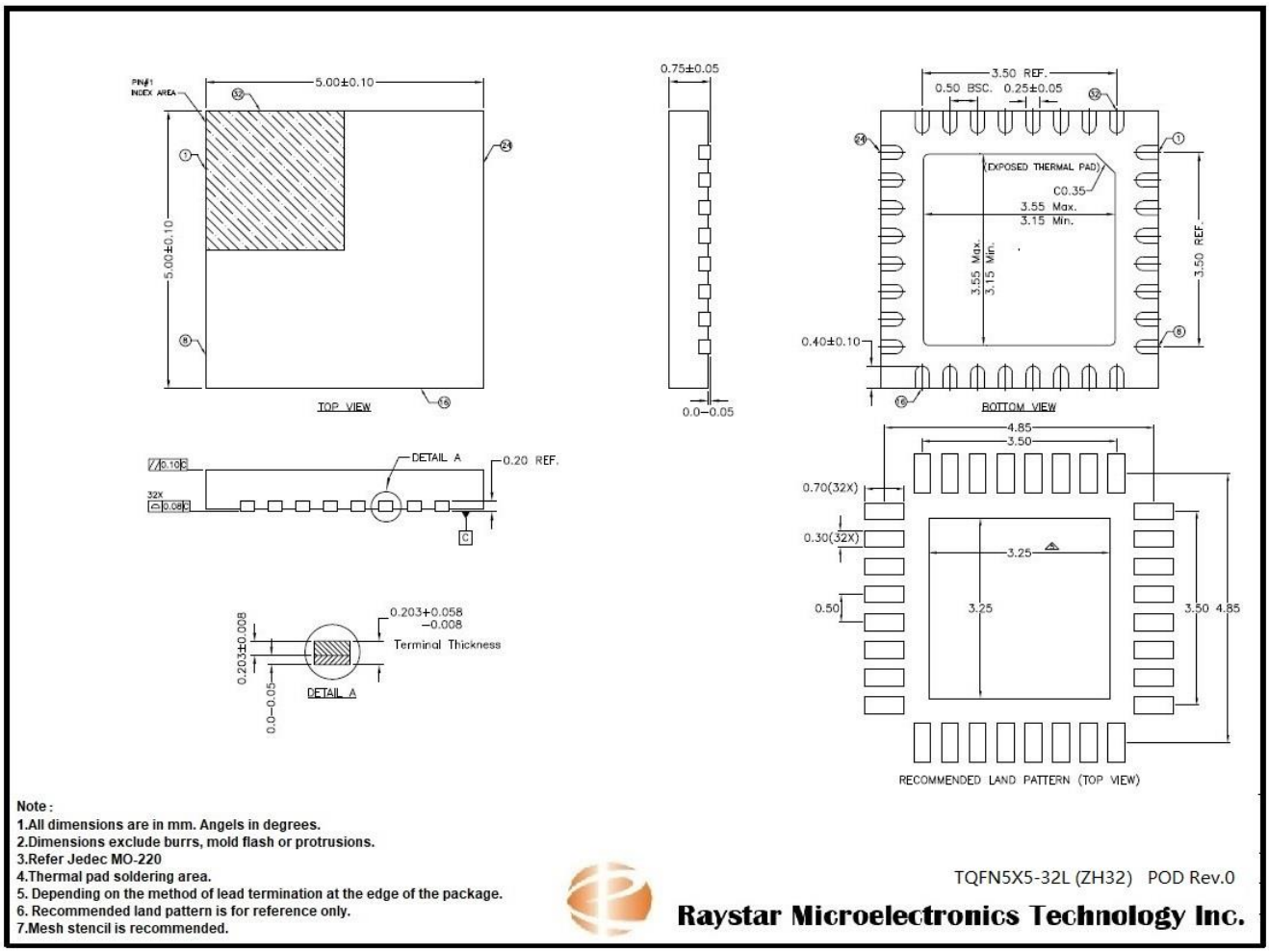


Recommended Crystal Specification

a) 25MHz, CL=8pF, +/-20ppm

Package Information

TQFN-32L (5x5mm)



Revision History

Revision	Description	Date
0.9	Preliminary release	2026/01/26
1.0	Initial release	2026/03/20