Features

- Six single-ended LVCMOS outputs, 30Ω output impedance
- Four LVPECL differential output pairs.
- One LVPECL (QA, nQA) output pair:156.25MHz
- One selectable LVPECL output pairs (QB, nQB): 100MHz 125MHz or 156.25MHz
- Two LP-HCSL output pairs: (QC, nQC and QD, nQD): 100MHz
- Selectable external crystal or single-ended input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- VCO frequency: 2.5GHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz – 20MHz): 0.256ps (Typ.)
- Power supply noise rejection PSNR: -80dB
- 3.3V supply voltage
- -40°C to 125°C ambient operating temperature
- AEC-Q 100 qualified, Automotive Grade 1 support; PPAP capable, and manufactured in IATF 16949 certified facilit
- Lead-free (RoHS 6) packaging

Applications

- PCI-e system
- Switch, Router
- 10Gb Ethernet network
- Communication system
- OTN
- Automotive infotainment

Description

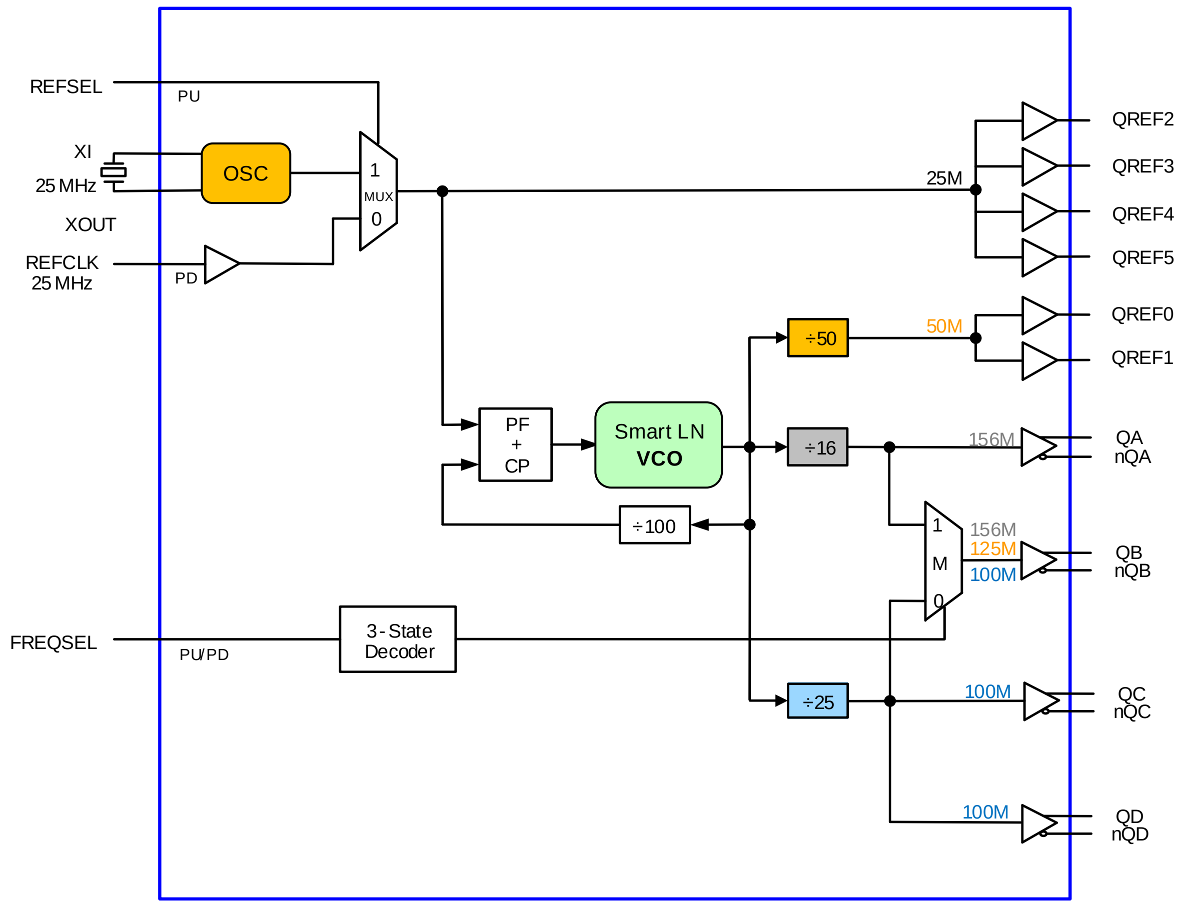
The RS2CG573Q is a PLL based clock Generator for use in Ethernet applications. The device has optimal high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. Using RSM's latest PLL technology, the RS2CG573Q achieves <0.3ps RMS phase jitter performance.

RS2CG573Q can synthesize 100MHz, 125MHz, 156.25MHz and a low frequency 50MHz CPU clock from a single device. Four LVCMOS outputs also serve as additional buffering of the 25MHz crystal reference.

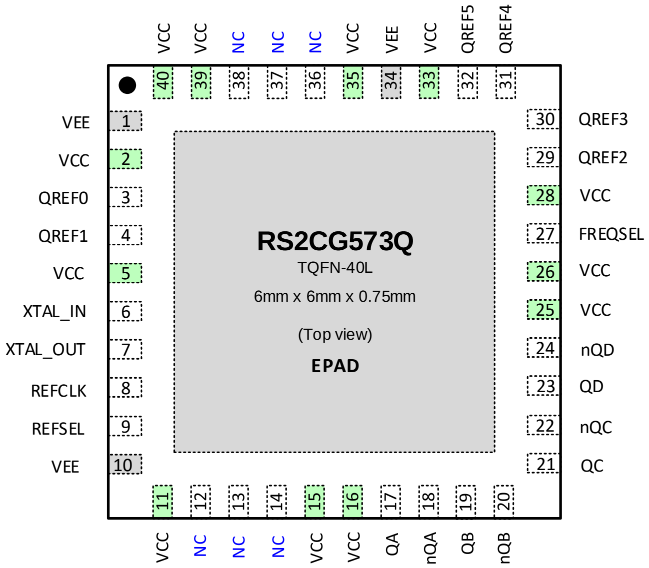
Order information

Part Number	Package	Description
RS2CG573QZDE	TQFN-40L	6mmX6mm

Functional Block Diagram



Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Type		Description
1, 10, 34	V_{EE}	Power		Negative supply pins.
2, 5, 11, 15, 16, 25,26, 28, 33,35, 39, 40	V_{CC}	Power		Pins 2, 28, 33 – power supply for the 25MHz LVCMOS outputs Pin 5 – power supply for the crystal oscillator Pins 11, 15, 26, 35 – power supply for the dividers and other core circuitry Pin 16 – power supply for the differential LVPECL outputs Pin 25 – power supply for the 50MHz LVCMOS output Pin 39 – power supply for the digital logic Pin 40 – power supply for the PLL
3, 4	QREF0, QREF1	Output		Single-ended outputs for 50MHz. 3.3V LVCMOS/LVTTL reference levels.
29,30,31,32	QREF2, QREF3, QREF4, QREF5	Output		Single-ended outputs for 25MHz. 3.3V LVCMOS/LVTTL reference levels.
6,7	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
8	REFCLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
9	REFSEL	Input	Pullup	Reference select pin. When HIGH, selects crystal. When LOW, selects REFCLK. LVCMOS/LVTTL interface levels.
12,13,14,36, 37,38	NC			No connect.
17, 18	QA, nQA	Output		156.25MHz differential output. LVPECL interface levels.
19, 20	QB, nQB	Output		100MHz,125MHz or 156.25MHz differential output. LVPECL interface levels.
21, 22	QC, nQC	Output		100MHz differential output. LP-HCSL interface levels.
23, 24	QD, QD0	Output		100MHz differential output. LP-HCSL interface levels.

Pin No.	Pin Name	Type		Description
27	FREQSEL	Input	Pullup	Frequency select pin. See Table. LVCMOS/LVTTL interface level.

Pin Characteristics

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
C_{IN}	Input Capacitance		Crystal Not Included		2		pF
C_{PD}	Power Dissipation Capacitance (per output)	QREF[0:5]	V_{CC} = 3.6V		6		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QREF[0:5]			30		Ω

Function Tables

REFSEL Function table

REFSEL	Input Source
0	REFCLK
1 (default)	OSC

FREQSEL Function Table

FREQSEL	Output Frequency (MHz)
	QB, nQB
0	100
M	125
1	156.25 (Default)

Absolute Maximum Ratings

Exposure to absolute Max rating conditions for extended periods may affect product reliability. Stresses beyond those listed under Absolute Max Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied.

Parameter	MIN	MAX	Units
Supply Voltage, V_{CC}	3	3.6	V
Inputs	-0.5	V_{CC} + 0.5	V
XTAL_IN	0	2	
Outputs, I_O (LVCMOS)	-0.5	V_{CC} + 0.5	V
Outputs, IO (LVPECL) Continuous Current Surge Current Surge Current		50 100	mA
Package Thermal Impedance, θJA		37.7	°C /W
Max Junction Temperature, T_{JMAX}		150	°C
Storage Temperature, T_{STG}	65	150	°C

Recommended Operating Condition

Symbol	Parameter	MIN	TYP	MAX	Units
T_A	Ambient air temperature	-40		125	°C
T_J	Junction temperature			125	°C

Note 1: It is the user's responsibility to ensure that device junction temperature remains below the Max allowed;
Note 2: All conditions in the table must be met to guarantee device functionality.
Note3: The device is verified to the Max operating junction temperature through simulation.

DC Electrical Characteristics

Power Supply DC Characteristics, V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
I_{EE}	Power Supply Current	No Load			250	mA

LVCMOS/LVTTL DC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
V_{IH}	Input High Voltage	REFSEL		2		V_{CC} + 0.3	V
		FREQSEL		V_{CC} - 0.4			V
V_{IL}	Input Low Voltage	REFSEL		-0.3		0.8	V
		FREQSEL				0.4	V
V_{IM}	Input Medium Voltage	FREQSEL		V_{CC}/2 - 0.1		V_{CC}/2 + 0.1	V
I_{IH}	Input High Current	REFCLK, FREQSEL	VCC = 3.6V VIN = 3.6V			150	µA
		REFSEL	VCC = 3.6V VIN = 3.6V			5	µA
I_{IL}	Input Low Current	REFCLK	VCC = 3.6V VIN = 0V	-5			µA
		REFSEL, FREQSEL	VCC = 3.6V VIN = 0V	-150			µA
V_{OH}	Output High Voltage; Note 1		V_{CC} = 3.3V ± 0.3V	2.3			V
V_{OL}	Output Low Voltage; Note 1		V_{CC} = 3.3V ± 0.3V			0.8	V

NOTE 1: Outputs terminated with 50Ω to VCC/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

LVPECL DC Characteristics, V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{OH}	Output High Voltage; Note 1		V_{CC} – 1.4		V_{CC} – 0.8	V
V_{OL}	Output Low Voltage; Note 1		V_{CC} – 2.0		V_{CC} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Note 1: Outputs terminated with 50ohm V_{CC} – 2V

Crystal Characteristics

Parameter	Test Conditions	MIN	TYP	MAX	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

LVPECL AC Characteristics, V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 125°

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
f_{IN}	Input Frequency				25		MHz
f_{OUT}	Output Frequency			100		156.25	MHz
tjit(θ)	RMS Phase Jitter (Random) Note 1		156.25MHz f_{OUT}, 25MHz crystal Integration Range:12kHz – 20MHz		0.233		ps
			125MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 20MHz		0.260		ps
			100MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 20MHz		0.28		ps
tsk(o)	Output Skew; Note 2, 3		Measured on the Rising Edge			40	ps
PSNR	Power Supply Noise Reduction	Pin40 (V_{CC})	From DC to 8MHz		-75		dB
		Pin40 (V_{CC})	From DC to 3MHz		-80		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		550	ps
ODC	Output Duty Cycle			48		52	%

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

Note 1: Refer to the Phase Noise Plot.

Note 2: This parameter is defined in accordance with JEDEC Standard 65.

Note 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints

AC Characteristics for Single Side Band Power Levels (LVPECL Outputs)
V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = 25°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	156.25MHz		-122		dBc/Hz
Φ_N (10k)	Single-side band phase noise, 10kHz from Carrier			-133		dBc/Hz
Φ_N (100k)	Single-side band phase noise, 100kHz from Carrier			-136		dBc/Hz
Φ_N (1M)	Single-side band phase noise, 1MHz from Carrier			-142		dBc/Hz
Φ_N (10M)	Single-side band phase noise, 10MHz from Carrier			-155		dBc/Hz
Φ_N (20M)	Single-side band phase noise, 20MHz from Carrier			-156		dBc/Hz
Φ_N (1k)	Single-side band phase noise, 1kHz from Carrier	125MHz		-125		dBc/Hz
Φ_N (10k)	Single-side band phase noise, 10kHz from Carrier			-135		dBc/Hz

Φ_N (100k)	Single-side band phase noise, 100kHz from Carrier			-138		dBc/Hz
Φ_N (1M)	Single-side band phase noise, 1MHz from Carrier			-144		dBc/Hz
Φ_N (10M)	Single-side band phase noise, 10MHz from Carrier			-155		dBc/Hz
Φ_N (20M)	Single-side band phase noise, 20MHz from Carrier			-156		dBc/Hz
Φ_N (1k)	Single-side band phase noise, 1kHz from Carrier	100MHz		-126		dBc/Hz
Φ_N (10k)	Single-side band phase noise, 10kHz from Carrier			-136		dBc/Hz
Φ_N (100k)	Single-side band phase noise, 100kHz from Carrier			-139		dBc/Hz
Φ_N (1M)	Single-side band phase noise, 1MHz from Carrier			-145		dBc/Hz
Φ_N (10M)	Single-side band phase noise, 10MHz from Carrier			-154		dBc/Hz
Φ_N (20M)	Single-side band phase noise, 20MHz from Carrier			-154		dBc/Hz

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

LVCMOS AC Characteristics, V_{CC} = 3.3V ± 0.3V, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
f_{IN}	Input Frequency			25		MHz
f_{OUT}	Output Frequency		25		50	MHz
tjit(θ)	RMS Phase Jitter (Random) NOTE 1	25MHz f_{OUT}, 25MHz crystal Integration Range:12kHz – 5MHz		0.2		ps
		50MHz f_{OUT}, 25MHz crystal Integration Range:12kHz – 5MHz		0.220		ps
tsk(o)	Output Skew; NOTE 2, 3 — QREF[0:5]	Measured on the Rising Edge			50	ps
PSNR	Power Supply Noise Reduction — Pin4,(V_{CC})	From DC to 6.25MHz		-80		dB
t_R / t_F	Output Rise/Fall Time	20% to 80%		700		ps
ODC	Output Duty Cycle		48		52	%

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

Note 1: Refer to the Phase Noise Plot.

Note 2: This parameter is defined in accordance with JEDEC Standard 65.

Note 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{CC}/2.

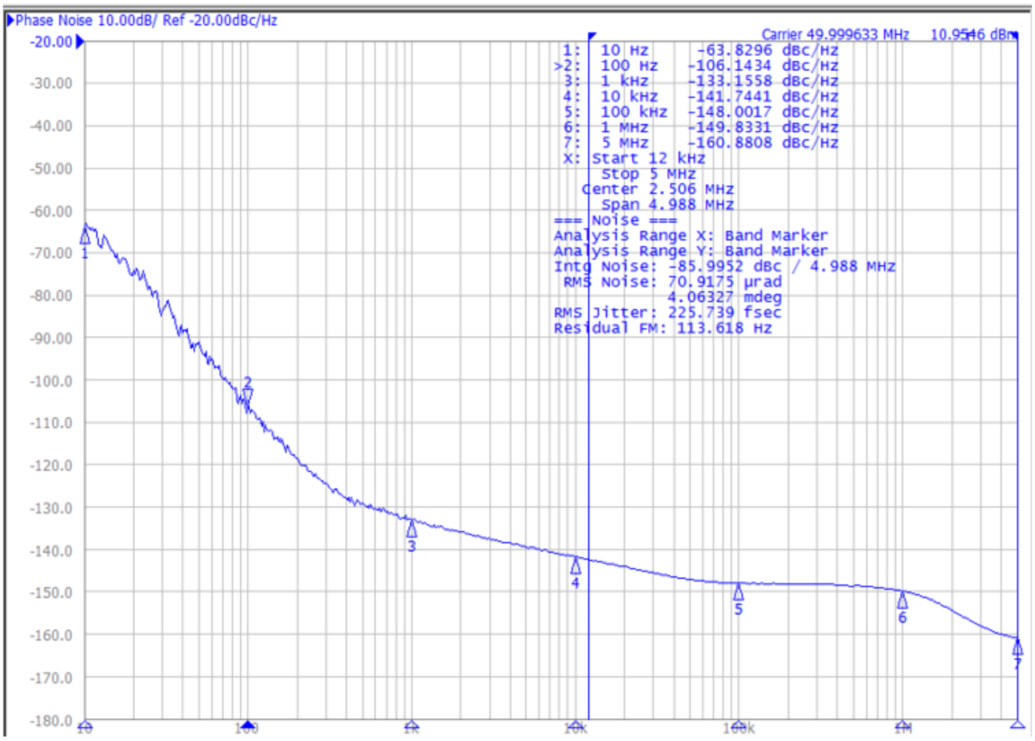
AC Characteristics for Single Side Band Power Levels (LVCMOS Outputs)

V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = 25°C

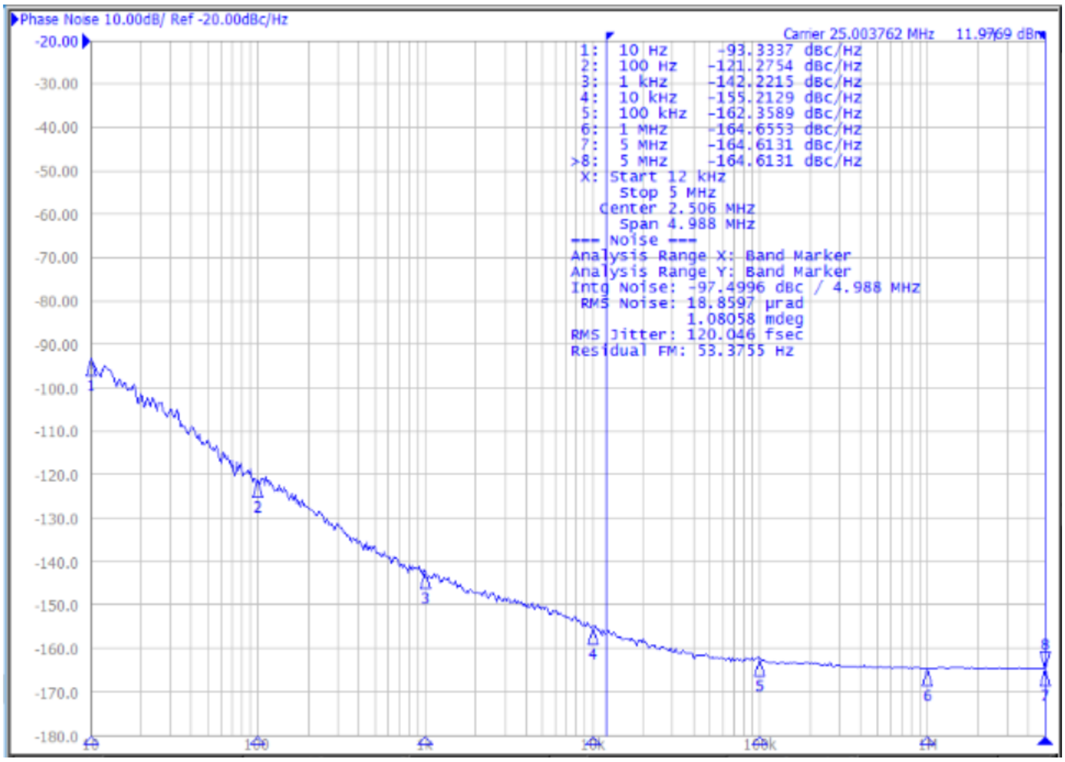
Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
Φ_N (1k)	Single-side band phase noise, 1kHz from Carrier	25MHz		-136		dBc/Hz
Φ_N (10k)	Single-side band phase noise, 10kHz from Carrier			-146		dBc/Hz
Φ_N (100k)	Single-side band phase noise, 100kHz from Carrier			-150		dBc/Hz
Φ_N (1M)	Single-side band phase noise, 1MHz from Carrier			-156		dBc/Hz
Φ_N (5M)	Single-side band phase noise, 5MHz from Carrier			-164		dBc/Hz
Φ_N (1k)	Single-side band phase noise, 1kHz from Carrier	50MHz		-133		dBc/Hz
Φ_N (10k)	Single-side band phase noise, 10kHz from Carrier			-141		dBc/Hz
Φ_N (100k)	Single-side band phase noise, 100kHz from Carrier			-148		dBc/Hz
Φ_N (1M)	Single-side band phase noise, 1MHz from Carrier			-149		dBc/Hz
Φ_N (5M)	Single-side band phase noise, 5MHz from Carrier			-160		dBc/Hz

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

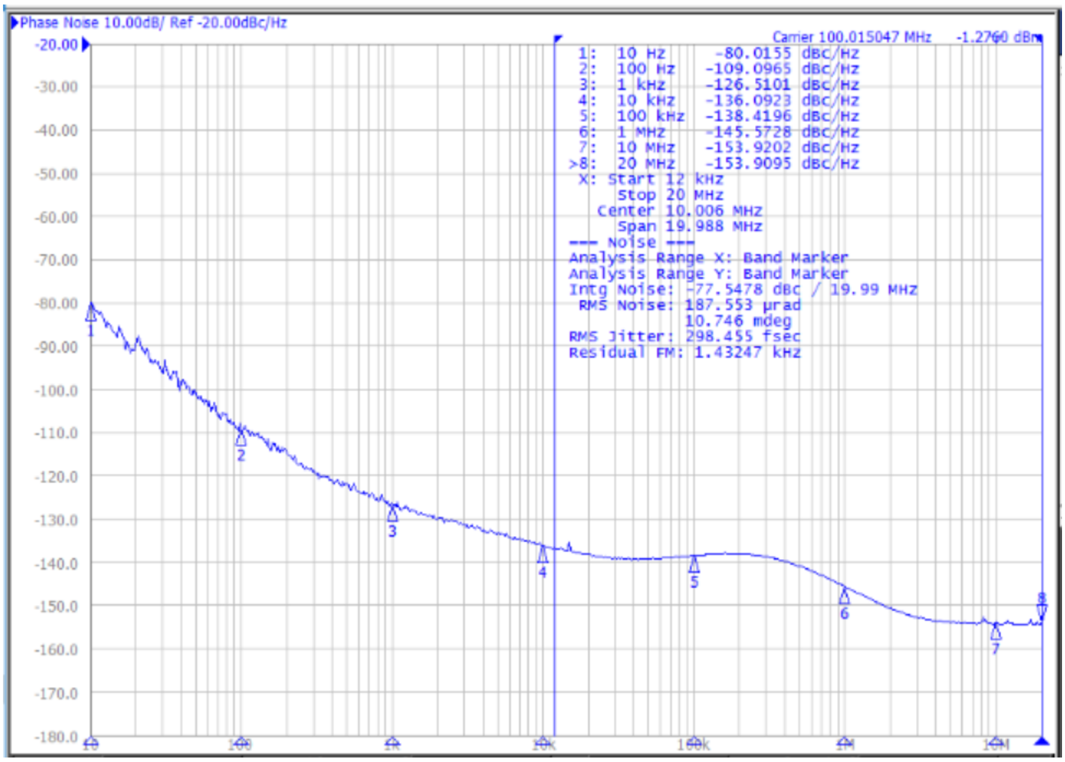
Typical Phase Noise at 50MHz (LVCMOS Output)



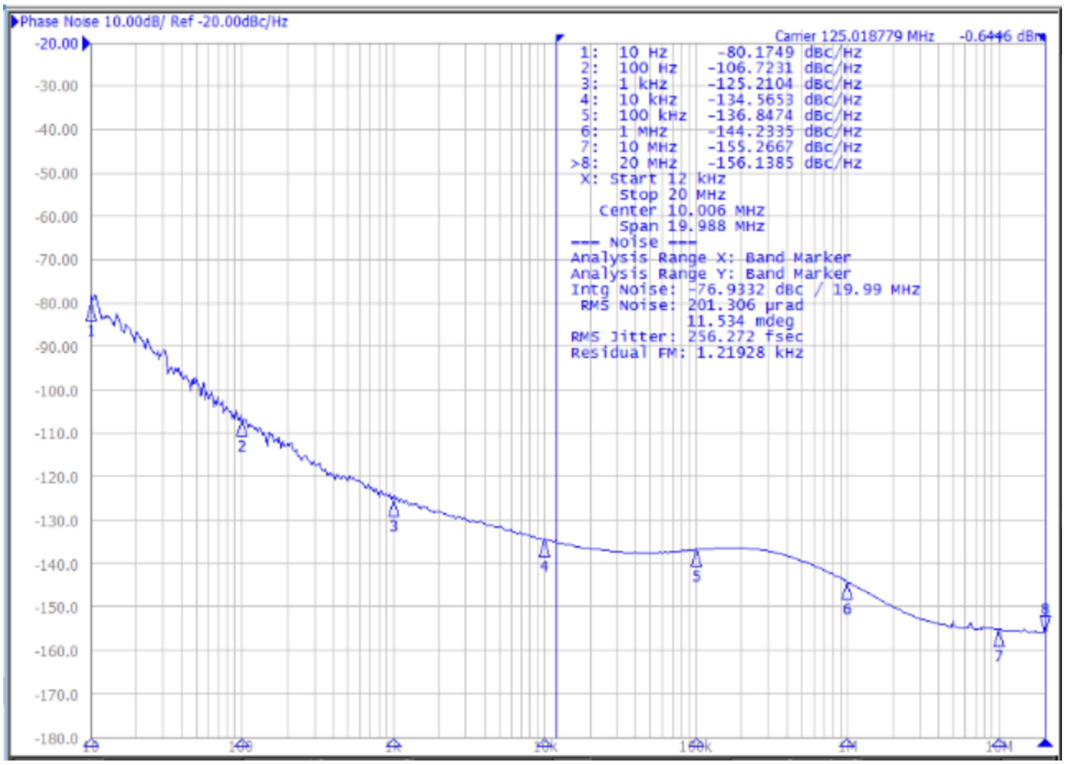
Typical Phase Noise at 25MHz (LVCMOS Output)



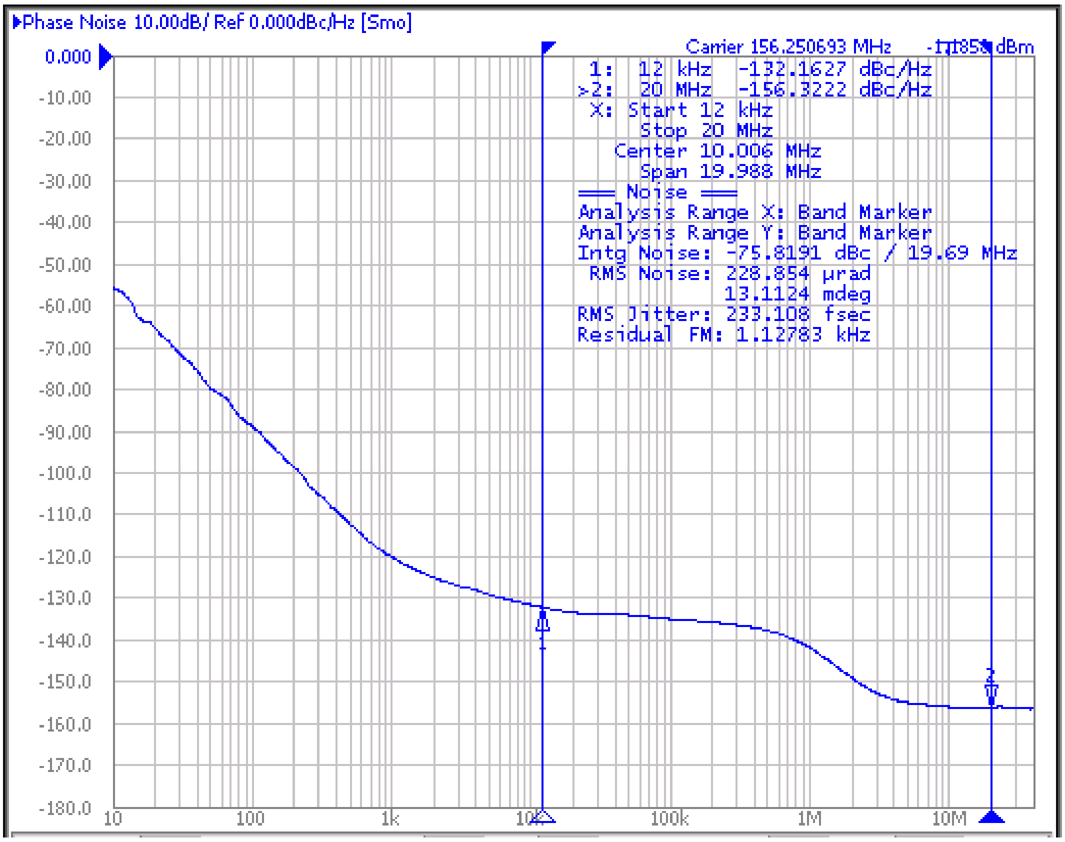
Typical Phase Noise at 100MHz (LVPECL Output)



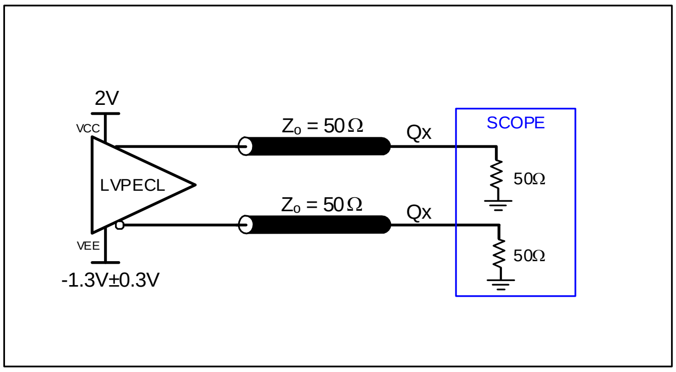
Typical Phase Noise at 125MHz (LVPECL Output)



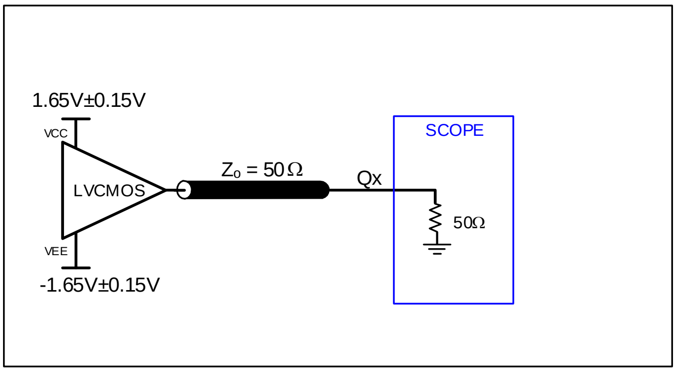
Typical Phase Noise at 156.25MHz (LVPECL Output)



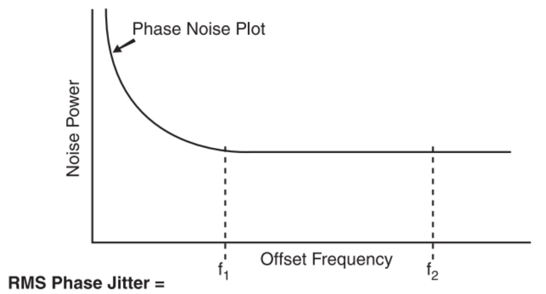
Parameter Measurement Information



LVPECL Output Load AC Test Circuit



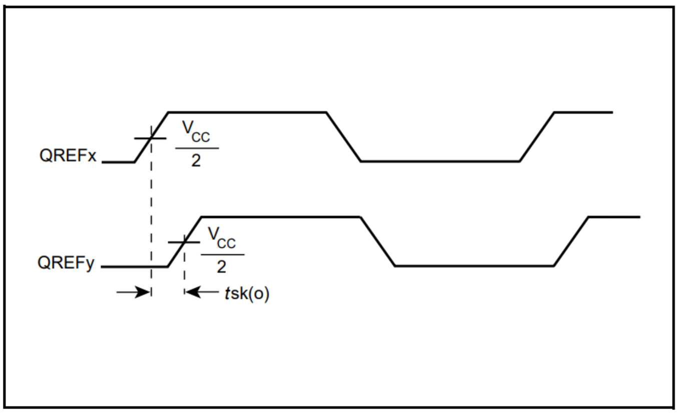
LVCMOS Output Load AC Test Circuit



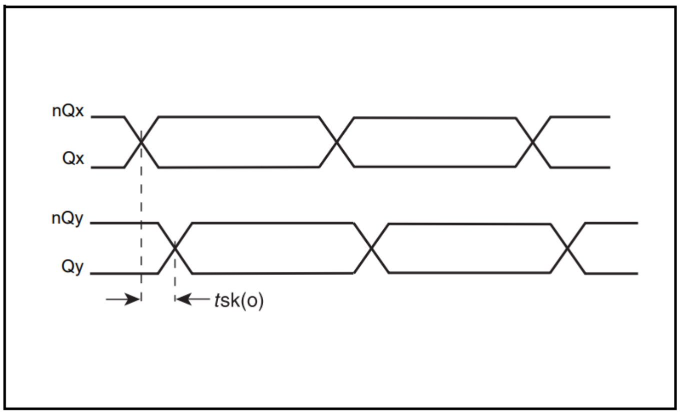
RMS Phase Jitter =

$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

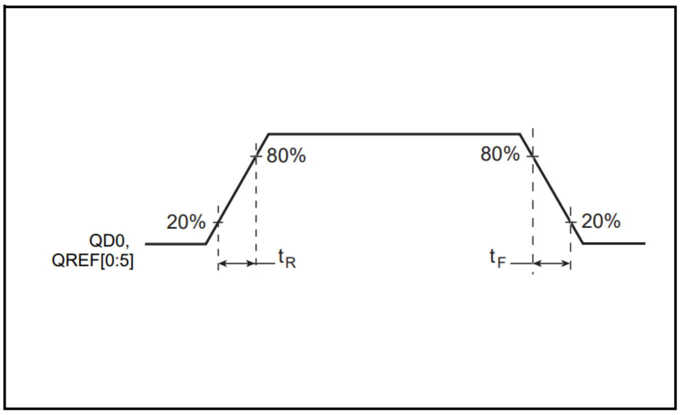
Phase Jitter



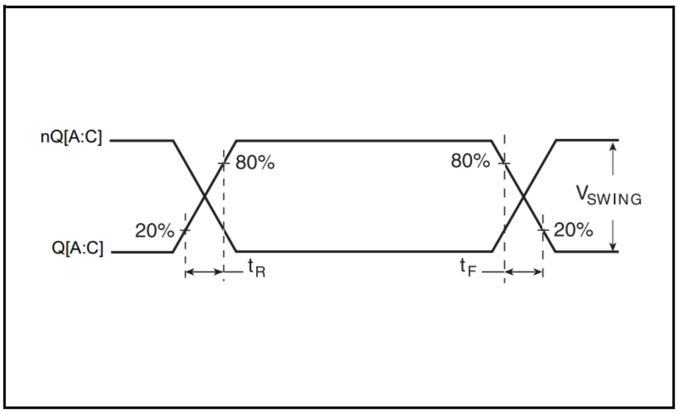
LVCMOS Output Skew



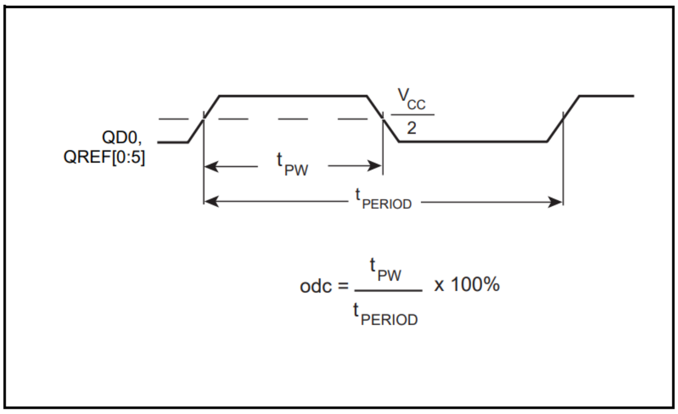
LVPECL Output Skew



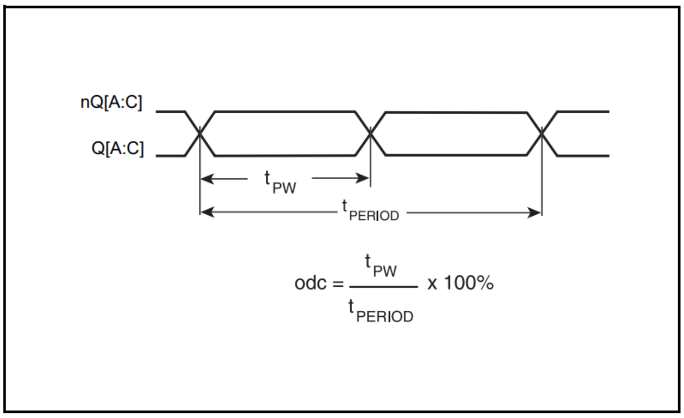
LVCMOS Output Rise/Fall Time



LVPECL Output Rise/Fall Time



LVCMOS Output Duty Cycle/Pulse Width/Period



LVPECL Output Duty Cycle/Pulse Width/Period

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ohm applications, R1 and R2 can be 100 . This can also be accomplished by removing R1 and making R2 50Ohm . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

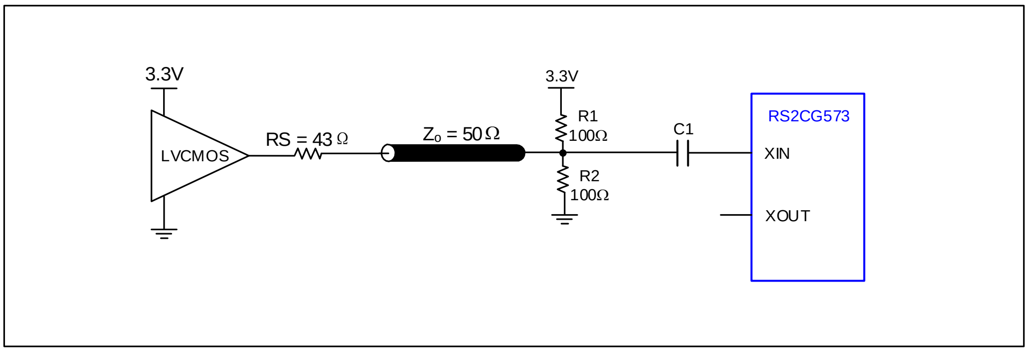
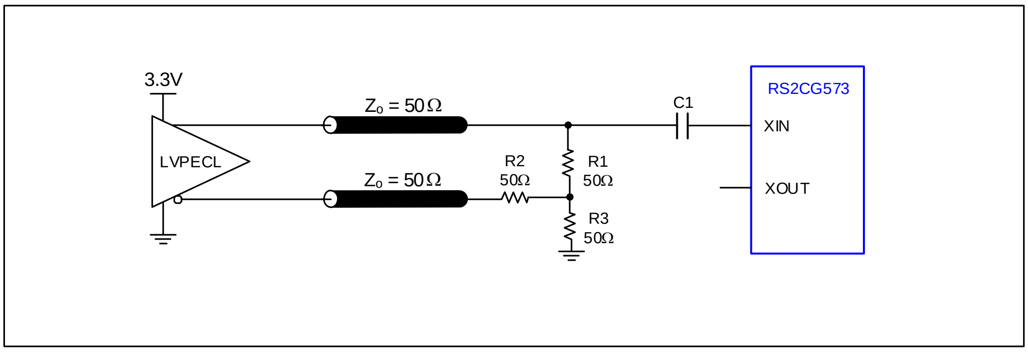


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

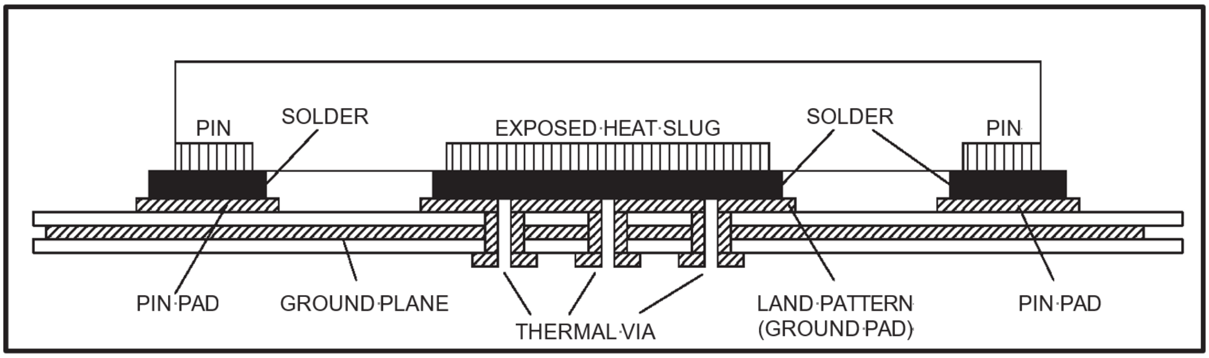


EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 2 P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ohm transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

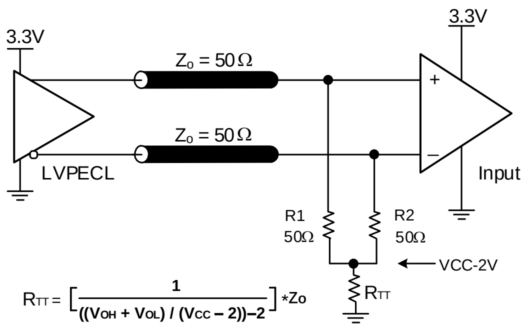


Figure 3A 3.3V LVPECL Output Termination

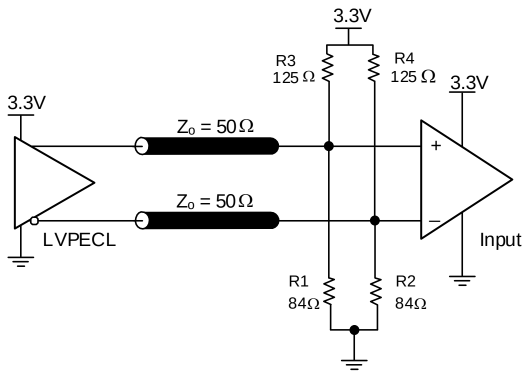


Figure 3B 3.3V LVPECL Output Termination

Recommendations for Unused Input and Output Pins

- **Inputs**

REFCLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REFCLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

- **Outputs**

LVCMOS Outputs

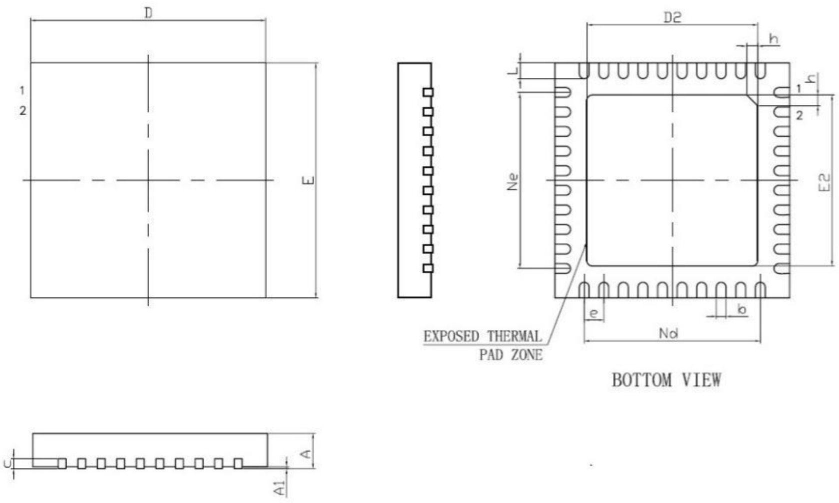
All unused LVCMOS output can be left floating. There should be no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated

Package information

TQFN-40L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	5. 90	6. 00	6. 10
D2	4. 10	4. 20	4. 30
e	0. 50BSC		
Ne	4. 50BSC		
Nd	4. 50BSC		
E	5. 90	6. 00	6. 10
E2	4. 10	4. 20	4. 30
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40
L/F载体尺寸 (MIL)	177*177		

Note:
1.All dimensions are in mm. Angels in degrees.
2.Coplanarity applies to the exposed thermal pad as well as the terminals.
3.Refer Jedec MO-220
4.Thermal pad soldering area.

TQFN6X6X0.75-0.5-40L (ZD40) POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary	2025/2/12
1.0	Initial release	2025/03/04
1.1	Update the block diagram	2026/06/05