Features

- 8 Low-power HCSL (LP-HCSL) outputs
- Integrated terminations eliminate up to 4 resistors per output pair
- Dedicated OE# pins support PCIe CLKREQ# function
- Selectable PLL bandwidths minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of PLL and bypass modes
- Spread spectrum compatible
- 100MHz and 133.33MHz PLL mode
- 1.8V operation voltage
- TQFN-48L-6x6mm

Applications

- SSD, microServers, WLAN Access points
- Cloud/High-performance Computing
- PCIe switch

Description

The RS2CB2318 is a 1.8V ultra-high performance zero delay and fanout buffers of RSM' full featured PCIe family support PCIe Gen7. It has integrated output terminations which can provide Zo = 100Ω or 85Ω for direct connection for 100Ω or 85Ω transmission lines. The device has 8 output enables for clock management support PCIe CLKREQ# function.
The family meets all published QPI/UPI, DB2000Q, DB1200ZL and PCIe Gen1-7 jitter specifications. with each output having an OE# pin to support the PCIe CLKREQ# function for low power states.

Key Specifications

- Fanout Buffer Mode additive phase jitter:
  - PCIe Gen7 CC, UPI > 20Gb/s < 20fs RMS
  - DB2000Q additive jitter < 39fs RMS
  - QPI/UPI 11.4GB/s < 40fs RMS
  - IF-UPI additive jitter < 70fs RMS
- ZDB Mode phase jitter:
  - PCIe Gen7 CC, UPI > 20Gb/s < 20fs RMS
  - QPI/UPI 11.4GB/s < 120fs RMS
  - IF-UPI additive jitter < 130fs RMS
  - Cycle-to-cycle jitter < 50ps
  - Output-to-output skew < 50ps

Ordering Information

Part Number	Package	Description	Differential Output Impedance (Ω)	Operation Temperature (℃)
RS2CB2318ZL	TQFN-48L	6mmx6mmx0.75mm 0.4mm pitch	85	-40~85
RS2CB2318-100ZL	TQFN-48L	6mmx6mmx0.75mm 0.4mm pitch	100	-40~85

Block Diagram

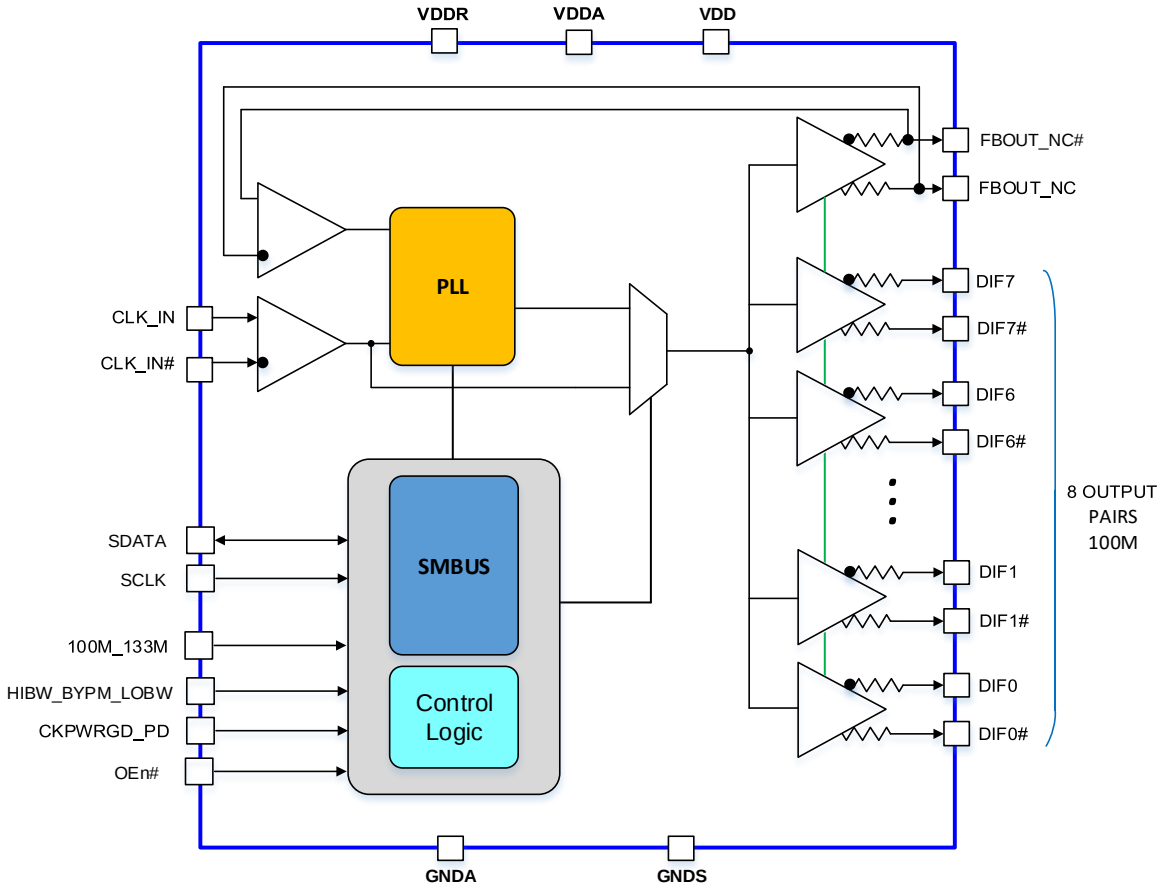


Figure 1. RS2CB2318 Block Diagram

Pin Configuration

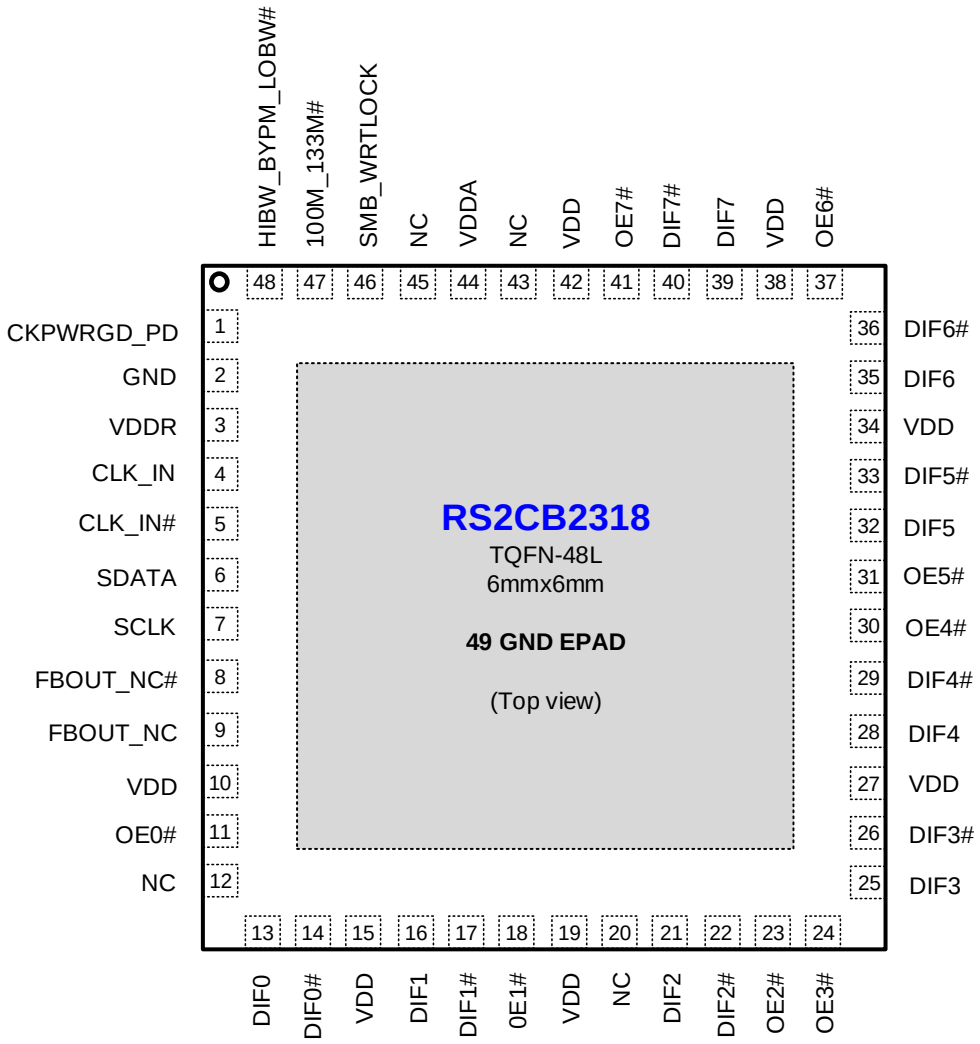


Figure 2. RS2CB2318 Pin Assignment for TQFN-48L

Pin Descriptions

No.	PIN NAME	TYPE	DESCRIPTION
1	CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
4	CLK_IN	IN	True Input for differential reference clock.
5	CLK_IN#	IN	Complementary Input for differential reference clock.
6	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
7	SCLK	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
8	FBOUT_NC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
9	FBOUT_NC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
11	OE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	DIF0	OUT	Differential true clock output
14	DIF0#	OUT	Differential Complementary clock output
16	DIF1	OUT	Differential true clock output
17	DIF1#	OUT	Differential Complementary clock output
18	OE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
21	DIF2	OUT	Differential true clock output
22	DIF2#	OUT	Differential Complementary clock output
23	OE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
24	OE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	DIF3	OUT	Differential true clock output
26	DIF3#	OUT	Differential Complementary clock output
28	DIF4	OUT	Differential true clock output
29	DIF4#	OUT	Differential Complementary clock output
30	OE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
31	OE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs

No.	PIN NAME	TYPE	DESCRIPTION
32	DIF5	OUT	Differential true clock output
33	DIF5#	OUT	Differential Complementary clock output
35	DIF6	OUT	Differential true clock output
36	DIF6#	OUT	Differential Complementary clock output
37	OE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
39	DIF7	OUT	Differential true clock output
40	DIF7#	OUT	Differential Complementary clock output
41	OE7#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
46	SMB_WRTLOCK	IN	This pin prevents SMBus writes when asserted. SMBus reads are not affected. This pin has an internal pull-down. 0 = SMBus writes allows, 1 = SMBus writes blocked.
47	100M_133M#	LATCHED IN	1.8V Input to select operating frequency. This pin has an internal pull-up resistor. See Frequency Selection (PLL Mode) table for definition.
48	HIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
3	VDDR	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
2	GND	GND	Ground Pin for VDDR
44	VDDA	PWR	power for the PLL core.
10,15,19, 27,34,38, 42	VDD	PWR	Power supply for differential outputs
12,20,43, 45	NC		No connection
49	GND	GND	Connect EPAD to ground

SMBus Address

Address	Read/Write bit
1101100	x

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On[1]
1	Running	1	0	Running	Running	On[1]
1	Running	1	1	Low	Low	On[1]

1. In ZDB Mode.

Frequency Select Table

100M_133M#	CLK_IN (MHz)	DIF[x]
1	100.00	CLK_IN
0	133M	CLK_IN

PLL Operating Mode

HiBW_BypM_LoBW#	MODE	PLL
0	PLL Lo BW	Running
M	Bypass	Off
1	PLL Hi BW	Running

Test Loads

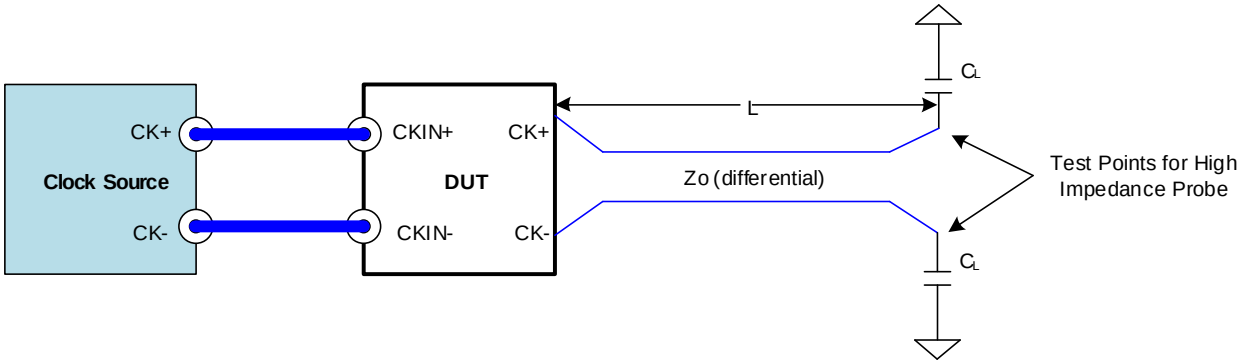


Figure 3. Test Load for AC/DC Measurements

Parameters for AC/DC Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Parameters Measured
SMA100B	RS2CB2318	Internal	85/100	25.4	2	AC/DC parameters

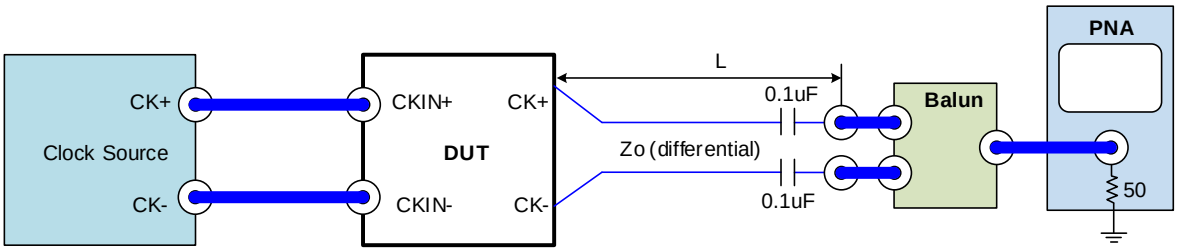


Figure 4. Test Load for Phase Jitter Measurements using Phase Noise Analyzer

Parameters for Phase Jitter Measurements using Phase Noise Analyzer

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Notes	Parameters Measured
SMA100B	RS2CB2318	Internal	85/100	25.4	N/A	Fanout Mode	PCIe, IF-UPI, DB2000Q
CK440	RS2CB2318	Internal	85/100	25.4		ZDB Mode	

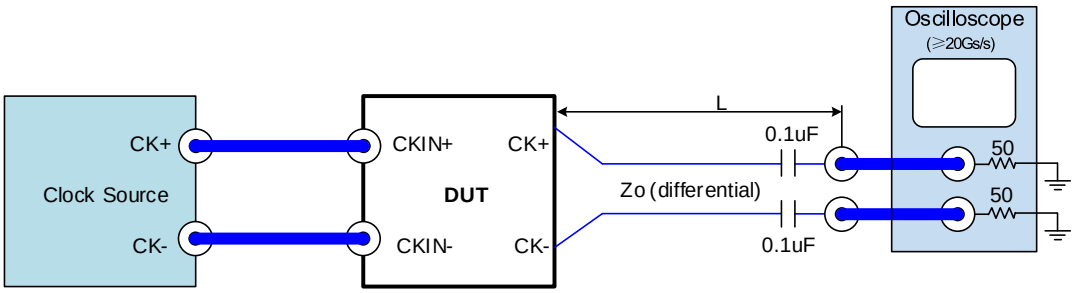


Figure 5. Test Load for Phase Jitter Measurements using Oscilloscope

Parameters for Phase Jitter Measurements using Oscilloscope

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Notes	Parameters Measured
SMA100B	RS2CB2318	Internal	85/100	25.4	N/A	Fanout Mode	QPI/UPI
CK440	RS2CB2318	Internal	85/100	25.4		ZDB Mode	

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage. These ratings, which are standard values for commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDxx	Applies to VDD, VDDA and VDDR	-0.5	-	1.9	V	1,2
Input Low Voltage	V_{IL}		GND-0.5	-	-	V	1
Input High Voltage	V_{IH}	Except for SMBus interface.	-0.5	-	V_{DD}+0.5V		1, 3
Input High Voltage	V_{IH}	SMBus clock and data pins			3.9V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD	Human Body Model	2000			V	1

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied nor guaranteed.
3. Not to exceed 3.9V.

Thermal Specifications

PARAMETER	SYMBOL	CONDITIONS	PACKAGE	TYP	UNITS
RS2CB2318 Thermal Resistance	θ_{JC}	Junction to case.	NDG48	19	°C/W
	θ_{Jb}	Junction to base.		0	°C/W
	θ_{JA0}	Junction to air, still air.		30	°C/W
	θ_{JA1}	Junction to air, 1 m/s air flow.		23	°C/W
	θ_{JA3}	Junction to air, 3 m/s air flow.		20	°C/W
	θ_{JA5}	Junction to air, 5 m/s air flow.		19	°C/W

AC/DC Electrical Characteristics

Clock Input Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Common Mode Voltage-CLK_IN	V_{COM}	Common Mode Input Voltage	150		900	mV	1
Input Swing-CLK_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate-CLK_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	VIN = VDD, VIN = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter-Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through +/-75mV window centered around differential zero.

Supply/Common Parameters

TA = TAMB, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	1.71	1.8	1.89	V	
Ambient Operating Temperature	T_{AMB}	Commercial range	-40	25	105	°C	
		Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75VDD	-	VDD + 0.3	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix)	0.4VDD	VDD/2	0.55VDD	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	GND - 0.3	-	0.8	V	
Input Current	I_{IN}	Single-ended inputs, VIN = GND, VIN = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs VIN = 0 V; Inputs with internal pull-up resistors VIN = VDD; Inputs with internal pull-down resistors	-50		50	uA	
Input Frequency	Fibyp	VDD = 1.8V, Bypass Mode.	1	-	400	MHz	2
	Fipll	VDD = 1.8V, 100MHz PLL Mode.	98.5	100.00	102.5	MHz	2
	Fipll	VDD = 1.8V, 133.33MHz PLL Mode. [3]	132	133.33	135	MHz	2
	Fipll	VDD = 1.8V, Bypass Mode.	1	-	400	MHz	2
ppm Error Contribution	ppm	ppm error contributed to input clock.		0		ppm	
Pin Inductance	Lpin				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except CLK_IN	1.5		5	pF	1
	C_{INCLK_IN}	CLK_IN differential clock inputs	1.5		2.7	pF	1,5
	C_{OUT}	Output pin capacitance			6	pF	1
CLK Stabilization	T_{STAB}	From VDD Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		1	1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# de-assertion	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2
SMBus Input Low Voltage	V_{ILSMB}	VDDSMB = 3.3V, see note 4 for VDDSMB < 3.3V			0.6	V	
SMBus Input High Voltage	V_{IHSMB}	VDDSMB = 3.3V, see note 5 for VDDSMB < 3.3V	1.5		3.6	V	4
SMBus Output Low Voltage	V_{OLSMB}	@ IPULLUP			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ VOL	4			mA	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Nominal Bus Voltage	V_{DDSMB}	Bus Voltage	1.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			400	kHz	6

1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing.
3. Time from de-assertion until outputs are > 200 mV.
4. For VDDSMB < 3.3V, VIHSMB > = 0.8xVDDSMB.
5. CLK_IN input.
6. The differential input clock must be running for the SMBus to be active.

Current Consumption

TA = TAMB, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	I_{DDA}	V_{DDA}, PLL Mode at 100MHz. [1]	-	37	45	mA
		V_{DDA}, Fanout Buffer Mode at 100MHz. [1]	-	4	5	mA
	I_{DD}	All other V_{DD} pins at 100MHz.	-	60	68	mA
Power Down Current	I_{DDAPD}	V_{DDA}, CKPWRGD_PD# = 0. [1]	-	3	4	mA
	I_{DDPD}	All other V_{DD} pins, CKPWRGD_PD# = 0.	-	1	2	mA

1. Includes V_{DDR}.

Low Power HCSL Outputs

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Specification Limits	UNITS
Slew Rate [1][2][3]	dV/dt	Scope averaging on.	2	3.1	4.3	1–4.5	V/ns
Slew Rate Matching [1][4][5]	ΔdV/dt	Single-ended measurement.	-	7.1	20	20	%
Maximum Voltage [5][6]	V_{max}	Measurement on single-ended signal using absolute value (scope averaging off).	700	787	850	150	mV
Minimum Voltage [5][6]	V_{min}		-150	-44	150	-300	
Crossing Voltage (abs) [1][5][7]	V_{cross_abs}	Scope averaging off.	300	369	450	250–550	mV
Crossing Voltage (var) [1][5][8]	Δ-V_{cross}	Scope averaging off.	-	19	50	140	mV

1. Confirmed by design and characterization, not 100% tested in production
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.
4. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
5. At default SMBus settings.
6. Includes previously separate values of +300mV overshoot and -300mV of undershoot.
7. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
8. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Output Duty Cycle, Jitter, Skew and PLL

TA = TAMB, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	2.7	4	MHz	1,5
		-3dB point in Low BW Mode	1	1.4	2	MHz	1,5
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain		1.1	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50.1	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-1	0.03	1	%	1,3
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2000	2500	2800	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-100	-4	100	ps	1,4
Skew, Output to Output	t_{sk3}	V_T = 50%		39	50	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		14	50	ps	1,2
		Additive Jitter in Bypass Mode		0.10	25	ps	1,2

1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
4. All outputs at default slew rate
5. The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

PCIe Phase Jitter – ZDB Mode

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Limits	UNITS
PCIe Phase Jitter, Low Bandwidth ZDB Mode (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s) [1][2]	-	2.30	5.46	86	ps (p-p)
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Hi Band (5.0 GT/s) [1][2]	-	0.08	0.13	3	ps (RMS)
		PCIe Gen 2 Lo Band (5.0 GT/s) [1][2]	-	0.07	0.12	3.1	
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s) [1][2]	-	0.042	0.068	1	
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s) [1][2][3][4]	-	0.042	0.068	0.5	
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s) [1][2][3][5][6]	-	0.016	0.024	0.15	
	$t_{jphPCIeG6-CC}$	PCIe Gen 6 (64.0 GT/s) [1][2][3][5][6]	-	0.015	0.022	0.1	
	$t_{jphPCIeG7-CC}$	PCIe Gen 7 (128.0 GT/s) [1][2][3][5][6]	-	0.01	0.02	0.067	
PCIe Phase Jitter, Low Bandwidth ZDB Mode (SRIS Architecture)	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (5.0 GT/s) [1][2][7]	-	0.78	1.35	N/A	ps (RMS)
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (8.0 GT/s) [1][2][7]	-	0.303	0.504		
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (16.0 GT/s) [1][2][7]	-	0.193	0.288		
	$t_{jphPCIeG5-SRIS}$	PCIe Gen 5 (32.0 GT/s) [1][2][7]	-	0.078	0.122		
	$t_{jphPCIeG6-SRIS}$	PCIe Gen 6 (64.0 GT/s) [1][2][7]	-	0.035	0.1		
	$t_{jphPCIeG7-SRIS}$	PCIe Gen 7 (128.0 GT/s) [1][2][7]	-	0.025	0.08		
PCIe Phase Jitter, High Bandwidth ZDB Mode (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s) [1][2]	-	4.26	7.03	86	ps (p-p)
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Hi Band (5.0 GT/s) [1][2]	-	0.15	0.25	3	ps (RMS)
		PCIe Gen 2 Lo Band (5.0 GT/s) [1][2]	-	0.08	0.12	3.1	
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s) [1][2]	-	0.076	0.126	1	
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s) [1][2][3][4]	-	0.0763	0.126	0.5	
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s) [1][2][3][5][6]	-	0.0266	0.041	0.15	
	$t_{jphPCIeG6-CC}$	PCIe Gen 6 (64.0 GT/s) [1][2][3][5][6]	-	0.015	0.022	0.1	
	$t_{jphPCIeG7-CC}$	PCIe Gen 7 (128.0 GT/s) [1][2][3][5][6]	-	0.01	0.02	0.067	
PCIe Phase Jitter, High Bandwidth ZDB Mode (SRIS Architecture)	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (5.0 GT/s) [1][2][7]	-	0.819	1.331	N/A	ps (RMS)
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (8.0 GT/s) [1][2][7]	-	0.312	0.480		
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (16.0 GT/s) [1][2][7]	-	0.217	0.284		
	$t_{jphPCIeG5-SRIS}$	PCIe Gen 5 (32.0 GT/s) [1][2][7]	-	0.084	0.118		
	$t_{jphPCIeG6-SRIS}$	PCIe Gen 6 (64.0 GT/s) [1][2][7]	-	0.035	0.1		
	$t_{jphPCIeG7-SRIS}$	PCIe Gen 7 (128.0 GT/s) [1][2][7]	-	0.025	0.08		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 7.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist

frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. This specification also applied to UPI data rates > 20Gb/s.
7. The PCI Express Base Specification 7.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. An additional consideration is the value for which to divide by √2. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by √2, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either 0.5ps RMS/√2 = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/√2 = 0.5ps RMS if the clock chip is near the clock input.

Additive PCIe Phase Jitter – Fanout Mode

TAMB = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Limits	UNITS
Additive PCIe Phase Jitter, Fanout Buffer Mode [8] (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s) [1][2]	-	0.9	1.4	86	ps (p-p)
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0GT/s) [1][2]	-	0.06	0.13	3	ps (RMS)
		PCIe Gen2 Lo Band (5.0 GT/s) [1][2]	-	0.04	0.07	3.1	ps (RMS)
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s) [1][2]	-	0.040	0.068	1	ps (RMS)
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s) [1][2][3][4]	-	0.040	0.068	0.5	ps (RMS)
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s) [1][2][3][5][6]	-	0.016	0.028	0.15	ps (RMS)
	$t_{jphPCIeG6-CC}$	PCIe Gen6 (64.0 GT/s) [1][2][3][5][6]	-	0.015	0.025	0.1	ps (RMS)
	$t_{jphPCIeG7-CC}$	PCIe Gen7 (128.0 GT/s) [1][2][3][5][6]	-	0.01	0.02	0.067	ps (RMS)
Additive PCIe Phase Jitter, Fanout Buffer Mode [8] (SRIS Architecture)	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (5.0 GT/s) [1][2][7]	-	0.100	0.151	N/A	ps (RMS)
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (8.0 GT/s) [1][2][7]	-	0.026	0.040		ps (RMS)
	$t_{jphPCIeG4-SRIS}$	PCIe Gen4 (16.0 GT/s) [1][2][7]	-	0.027	0.042		ps (RMS)
	$t_{jphPCIeG5-SRIS}$	PCIe Gen5 (32.0 GT/s) [1][2][7]	-	0.024	0.041		ps (RMS)
	$t_{jphPCIeG6-SRIS}$	PCIe Gen 6 (64.0 GT/s) [1][2][7]	-	0.023	0.04		ps (RMS
	$t_{jphPCIeG7-SRIS}$	PCIe Gen 7 (128.0 GT/s) [1][2][7]	-	0.023	0.04		ps (RMS

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 7.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-

SSC content.

4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. This specification also applied to UPI data rates > 20Gb/s.
7. The PCI Express Base Specification 7.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. An additional consideration is the value for which to divide by √2. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by √2, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either 0.5ps RMS/√2 = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/√2 = 0.5ps RMS if the clock chip is near the clock input.
8. Additive jitter for RMS values is calculated by solving for "b" where b = √(c2 - a2) and "a" is rms input jitter and "c" is rms output jitter.

Filtered Phase Jitter Parameters – QPI/UPI, IF-UPI and DB2000Q

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Limits	UNITS
Additive Phase Jitter, Fanout Mode	$t_{jphIF-UPI}$	IF-UPI, Lo-BW ZDB Mode [1][2][3]	-	0.10	0.13	1	ps (RMS)
		IF-UPI, Hi-BW ZDB Mode [1][2][3]	-	0.17	0.20	1	ps (RMS)
		IF-UPI, Fanout Mode [1][2][3]	-	0.06	0.07	1	ps (RMS)
	$t_{jphDB2000Q}$	DB2000Q, Fanout Mode [1][4]	-	22	25	80	fs (RMS)

1. Applies to all differential outputs, guaranteed by design and characterization. See Test Loads for measurement setup details. Legacy QPI and UPI specifications (100MHz or 133.33MHz clocking with data rates of 4.8Gb/s to 11.4Gb/s are automatically met in all operating modes when the PCI Gen5 CC requirements are met. See Table 12 and Table 13.
2. For RMS values, additive jitter is calculated by solving for "b" where b = √(c2 - a2), "a" is rms input jitter and "c" is rms total jitter.
3. Calculated from phase noise analyzer with Intel-specified brick-wall filter applied. This is an additive jitter specification regardless of buffer operating mode. The enhanced 9ZXL devices meet this specification in all operating modes.
4. Calculated from Intel-supplied clock jitter tool.

Phase Jitter Parameters – 12kHz to 20MHz

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Limits	UNITS
12kHz–20MHz Additive Phase Jitter, Fanout Buffer Mode [1][2][3]	$t_{jph12k-20MFOB}$	Fanout Buffer Mode, SSC OFF, 100MHz	-	102	125	N/A	fs (RMS)

1. Applies to all differential outputs, guaranteed by design and characterization. See Test Loads for measurement setup details.
2. 12kHz to 20MHz brick wall filter.
3. For RMS values, additive jitter is calculated by solving for "b" where b = √(c2 - a2), "a" is rms input jitter and "c" is rms total jitter.

SMBus Interface

Write Sequence

- Controller (host) sends a start bit
- Controller (host) sends the write address
- RS2CB2318 clock will **acknowledge**
- Controller (host) sends the beginning byte Location= N
- RS2CB2318 clock will **acknowledge**
- Controller (host) sends the byte count = X
- RS2CB2318 clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- RS2CB2318 clock will **acknowledge** each byte one at a time
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**RS2CB2318 (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stop bit		

Read Sequence

- Controller (host) will send a start bit
- Controller (host) sends the write address
- RS2CB2318 clock will **acknowledge**
- Controller (host) sends the beginning byte Location= N
- RS2CB2318 clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- RS2CB2318 clock will **acknowledge**
- RS2CB2318 clock will send the data byte count = X
- RS2CB2318 clock sends **Byte N+X-1**
- RS2CB2318 clock sends **Byte L through Byte X (if X(H) was written to Byte 7)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**RS2CB2318 (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat start		
Slave Address			
RD	Read		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not		
P	stop bit		

Byte 0: PLL Mode and Frequency Select Register

Byte 0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	PLL Operating Mode Readback 1	PLL Operating Mode Readback 0	Reserved	Reserved	Enable software control of PLL BW	PLLOperating Mode 1	PLL Operating Mode 0	Frequenc y Select Readback
Type	R	R			RW	RW	RW	R
0	00 = Low BW ZDB Mode	01 = Bypass (Fanout Buffer)			HW Latch	00 = Low BW ZDB Mode	01 = Bypass (Fanout Buffer)	133MHz
1	10 = Reserved	11 = High BW ZDB Mode			SMBus Control	10 = Reserved	11 = High BW ZDB Mode	100MHz
Name	PLL Rdbk[1]	PLL Rdbk[0]			PLL_SW_EN	PLL Mode[1]	PLL Mode[0]	100M_133M#
Default	Latch	Latch	0	0	0	1	1	Latch

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 5 via use of bits 2 and 1. A warm system reset is required if the user changes these bits. Bit 0 defaults to 1 on the 9ZXL06x2 devices.

Byte 1: Output Control Register 1

Byte 1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output Enable							
Type	RW							
0	Low/Low							
1	OE# Pin Control							
RS2CB2318 Name	DIF5_en	DIF4_en	DIF3_en	DIF2_en	Reserved	DIF1_en	DIF0_en	Reserved
RS2CB2318 Default	1	1	1	1	0	1	1	0

Byte 2: Output Control Register 2

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output _enable							
Type	RW							
0	Low/Low							
1	OE# Pin Control							
RS2CB2318 Name	Reserved	Reserved	Reserved	Reserved	Reserved	DIF7_en	Reserved	DIF6_en
RS2CB2318 Default	0	0	0	0	0	1	0	1

Byte 3: Reserved

Byte 4: Reserved

Byte 5: Revision and Vendor ID Register

Byte 5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Revision ID				Vendor ID			
Type	R	R	R	R	R	R	R	R
0	**A** rev = 0000				**RSM** = 0001			
1								
Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0
Default	0	0	0	0	0	0	0	1

Byte 6: Device ID Register

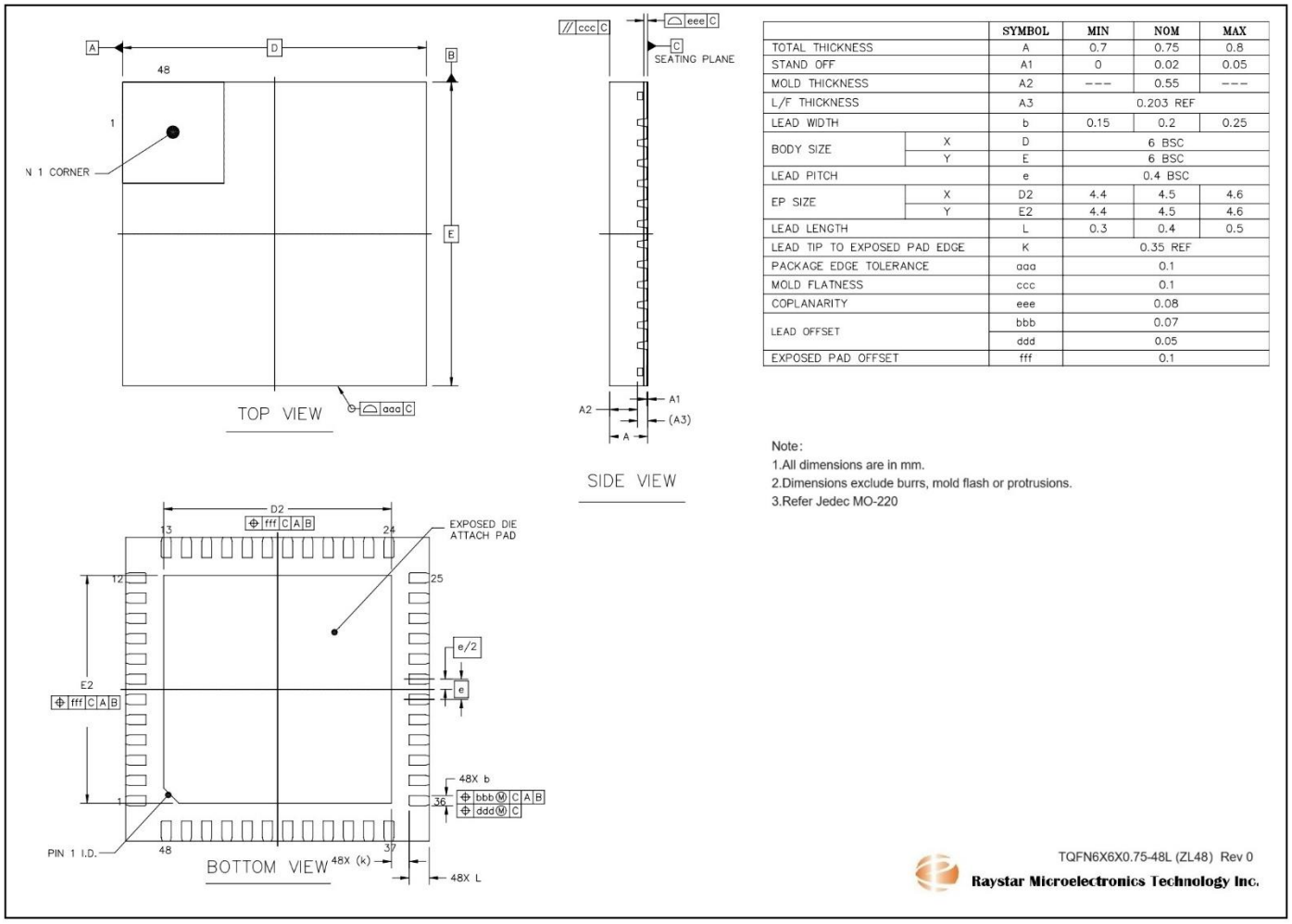
Byte 6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	N/A							
Type	R	R	R	R	R	R	R	R
0	Device ID							
1								
Name	DevID 7	DevID 6	DevID 5	DevID 4	DevID 3	DevID 2	DevID 1	DevID 0
RS2CB2318	**0hF6**							

Byte 7: Byte Count Register

Byte 7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Writing to this register configures how many bytes will be read back on a block read.				
Type				RW	RW	RW	RW	RW
0				Default value is 8.				
1								
Name				BC4	BC3	BC2	BC1	BC0
Default	0	0	0	0	1	0	0	0

Package Information

TQFN-48L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.4	4.5	4.6
	Y	E2	4.4	4.5	4.6
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TQFN6X6X0.75-48L (ZL48) Rev 0
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary	2025/02/20
1.0	Initial release	2025/12/11
1.1	Modify the VDDR and GND pin number error in Page 5 Add PCIe Gen7 Data	2026/03/09