Features

- One LVCMOS/LVTTL output
- Differential CLK/nCLK input pair
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS
- Output frequency: 200MHz (typical)
- Part-to-part skew: 500ps (maximum)
- Additive phase jitter, RMS: 0.21ps (typical), 3.3V output
- 3.3V/2.5V operating supply
- -40°C to 125°C ambient operating temperature
- AEC-Q100 qualified, Automotive Grade 1 support; PPAP capable, and manufactured in IATF 16949 certified facilities

Description

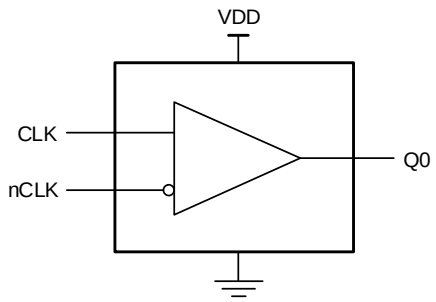
The RS83021Q is a 1-to-1 Differential-to-LVCMOS/ LVTTL Translator and a member of the family of High-Performance Clock Solutions. The differential input is highly flexible and can accept the following input types: LVPECL, LVDS, LVHSTL, SSTL, and HCSL. The small package makes this device ideal for use in applications with limited board space.

Order Information

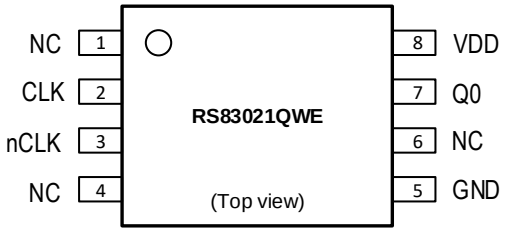
Part Number	Package	Description
RS83021QWE	SOP8	4.9mmx6mm
RS83021QTAE	SOT23-5	2.95mmx3.02mm

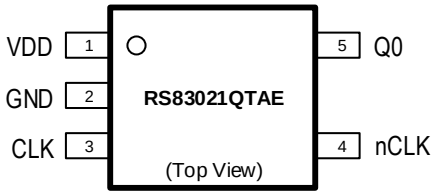
Notes
[1] E = Pb-free and Green

Block Diagram



Pin Configuration





Pin Descriptions

Number		Name	Type		Description
1, 4, 6		NC			No connect.
2	3	CLK	Input	Pulldown	Non-inverting differential clock input.
3	4	nCLK	Input	Pullup	Inverting differential clock input.
5	2	GND	Power		Power supply ground.
7	5	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	1	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Pin Characteristics

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.6V		23		pF
R_{OUT}	Output Impedance		5	7	12	Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	103°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C
HBM	3500V
CDM	1000V
LU	200mA

DC Electrical Characteristics

Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				20	mA

LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{OH}	Output High Voltage; NOTE 1	V_{DD} = 3.6V	2.6			V
		V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	V_{DD} = 3.6V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, *Output Load Test Circuit Diagrams.*

Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 125°C

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{DD} = 3.6V or 2.625V			5	µA
		CLK	V_{IN} = V_{DD} = 3.6V or 2.625V			150	µA
I_{IL}	Input Low Cureent	nCLK	V_{IN} = 0V, V_{DD} = 3.6V or 2.625V	-150			µA
		CLK	V_{IN} = 0V, V_{DD} = 3.6V or 2.625V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 125°C

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
f_{MAX}	Output Frequency			200		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \le 200$MHz	1.7	2.0	2.3	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz – 10MHz)		0.21		ps
t_R / t_F	Output Rise/Fall Time	0.8V to 2V	100	250	400	ps
odc	Output Duty Cycle	$f \le 166$MHz	45	50	55	%
		166MHz < $f \le$ 200MHz	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions.

Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$. NOTE 3:

This parameter is defined in accordance with JEDEC Standard 65.

AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 125°C

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
f_{MAX}	Output Frequency			200		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \le 350$MHz	1.9	2.2	2.5	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz – 10MHz)		0.21		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle	$f \le 250$MHz	45	50	55	%
		250MHz < $f \le$ 350MHz	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

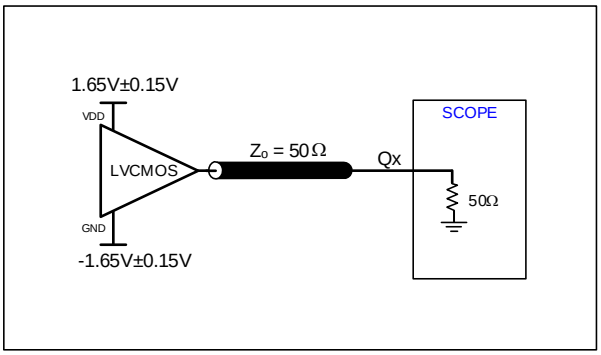
All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.

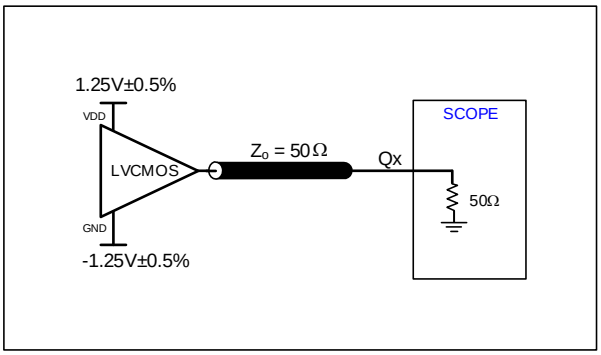
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

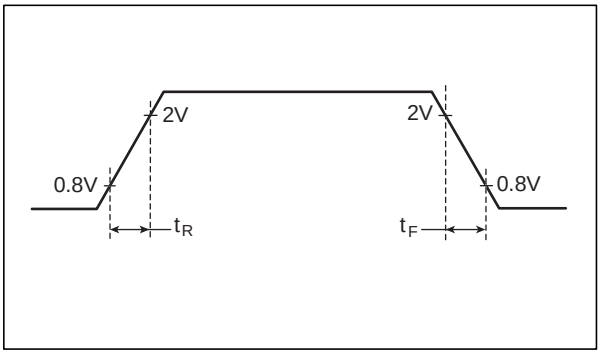
Parameter Measurement Information



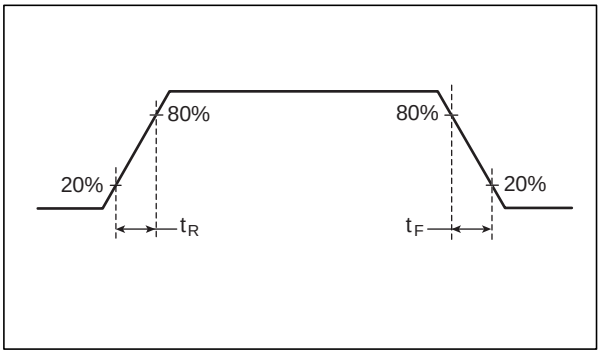
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



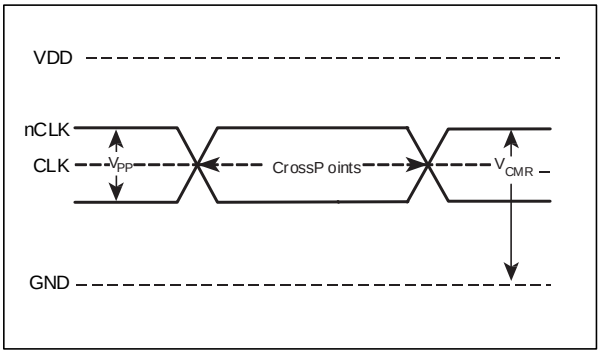
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



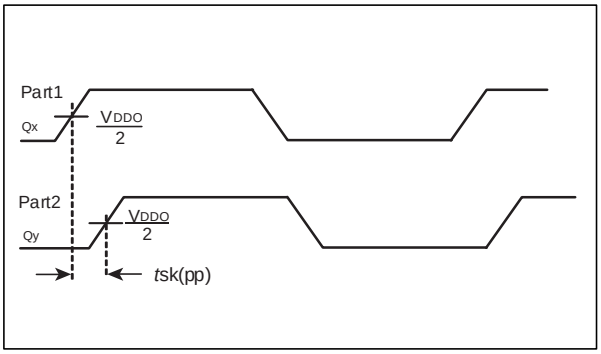
3.3V Output Rise/Fall Time



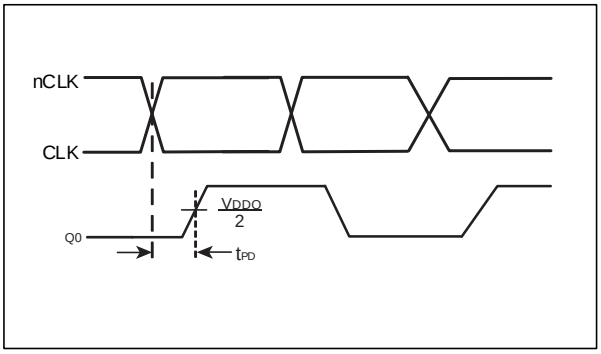
2.5V Output Rise/Fall Time



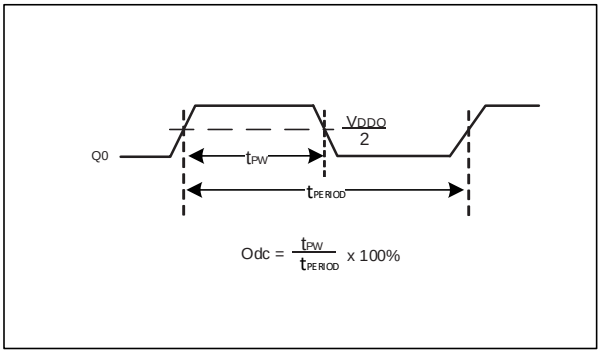
Differential Input Level



Part-to-Part Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

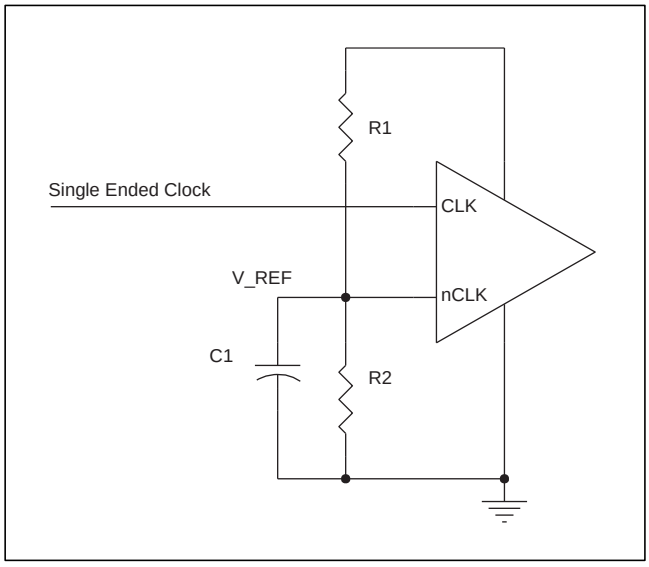
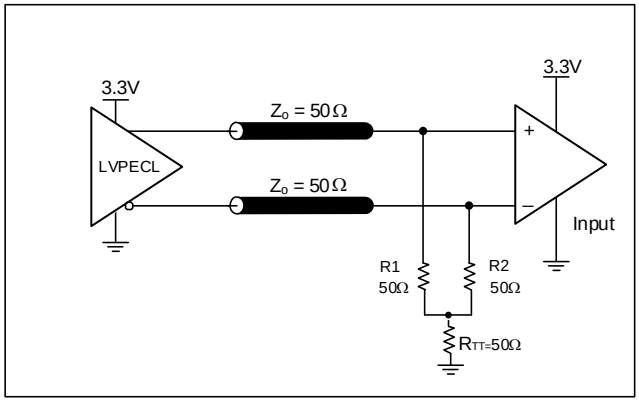


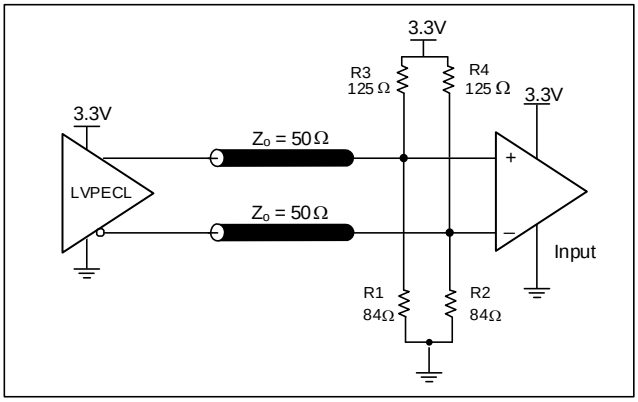
Figure 1. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

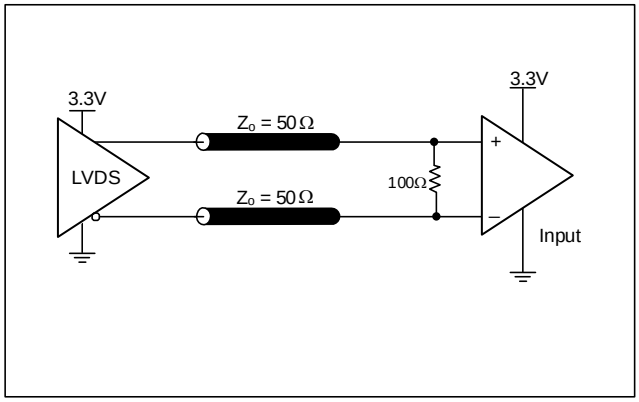
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2 to 5* show interface examples for the HiPerClockS CLK/nCLK input driven by LVDS, LVPECL, HCSL. The input interfaces suggested here are examples only.



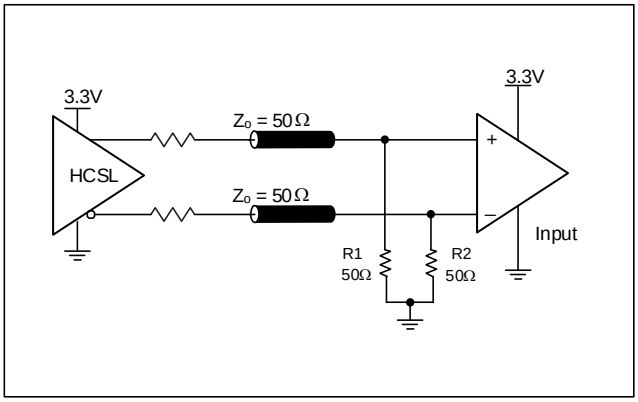
Input Driven by a 3.3V LVPECL Driver



Input Driven by a 3.3V LVPECL Driver



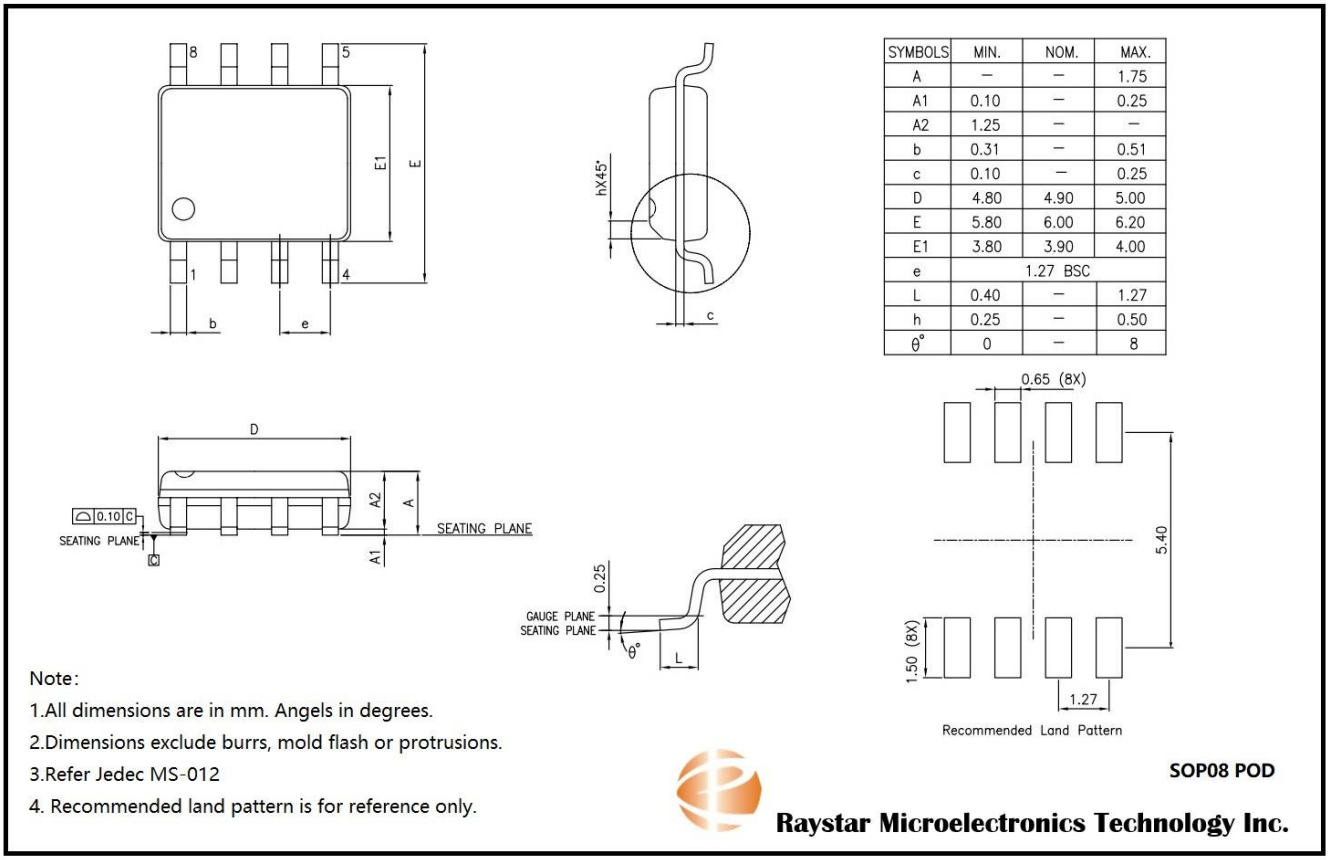
Input Driven by a 3.3V LVDS Driver



Input Driven by a 3.3V HCSL Driver

Package Information

SOP8



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

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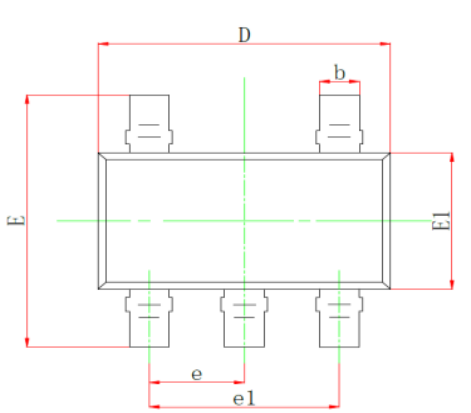
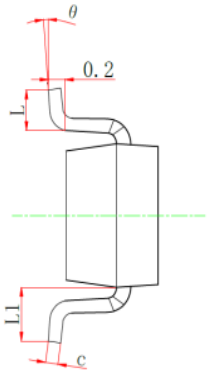
SOT23-5

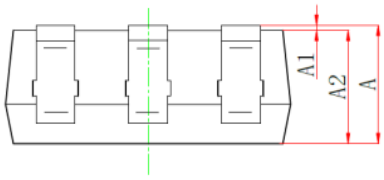


TOP VIEW
[顶视图]



SIDE VIEW
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC.)		0.037(BSC.)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°



BOTTOM VIEW
[背视图]

Note:
1. All dimensions are in mm. Angels in degrees.
2. Refer Jedec MO-187
3. Dimensions exclude burrs, mold flash or protrusions.

SOT23-5L POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V0.9	Preliminary Release	2025/07/17
V1.0	Initial release	2026/02/04