RS7LS4T774Q

4-Bit Dual-Supply Bus Transceiver With Configurable Voltage-Level Shifting and 3-State Outputs With Independent Direction Control Inputs

Features

- Each channel has an independent DIR control input
- Control inputs V_{IH}/V_{IL} levels are referenced to V_{CCA} voltage
- 1.1 V to 1.95 V on A Port and 1.65 V to 5.5 V on B Port
- I/Os are 2.5V tolerant (IOA) and 6.5V tolerant (IOB).
- I_{off} Supports partial power-down-mode operation
- Typical data rates
  - 380Mbps (1.8V to 3.3V translation)
  - 200Mbps (<1.8V to 3.3V translation)
  - 200Mbps (translate to 2.5V or 1.8V)
  - 150Mbps (translate to 1.5V)
  - 100Mbps (translate to 1.2V)
- Latch-up performance exceeds 100mA Per JESD 78, class II
- AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
- ESD Protection exceeds the following levels
  - ±4000V Human-body model
  - ±1000V Charged-device model

Applications

- Automotive Infotainment
- Advanced Driver Assistance Systems(ADAS)
- Telematics
- Personal electronic
- Industrial
- Enterprise
- Telecom

Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.1V to 1.95V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bi-directional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The RS7LS4T774Q is designed for asynchronous communication between data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports in the high-impedance mode. The device transmits data from the A bus to the B bus when the B outputs are activated, and from the B bus to the A bus when the A outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The RS7LS4T774Q is designed so that the control pins (DIR1, DIR2, DIR3, DIR4, and $\overline{OE}$) are supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

For a high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Since this device has CMOS inputs, it is very important to not allow them to float. If the inputs are not driven to either a high V_{CC} state, or a low-GND state, an undesirable larger than expected I_{CC} current may result. Since the input voltage settlement is governed by many factors (for example, capacitance, board-layout, package inductance, surrounding conditions, and so forth), ensuring that these inputs are kept out of erroneous switching states and tying them to either a high or a low level minimizes the leakage current.

Ordering Information

Part Number	Package	Description
RS7LS4T774QLE	TSSOP16	5mm × 6.4mm
RS7LS4T774QZPE	QFN16L	3.5mm x 2.5mm

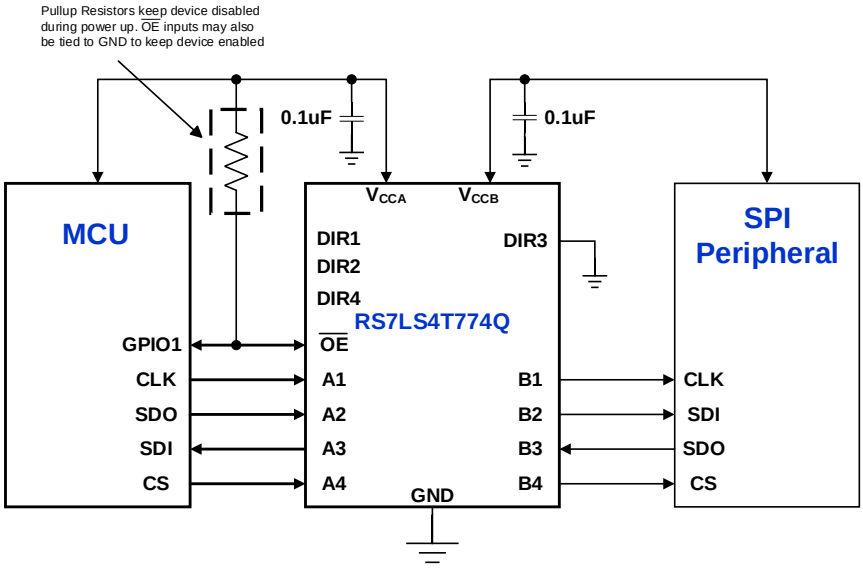

Figure 1. Typical Application Schematic

Pin Configuration

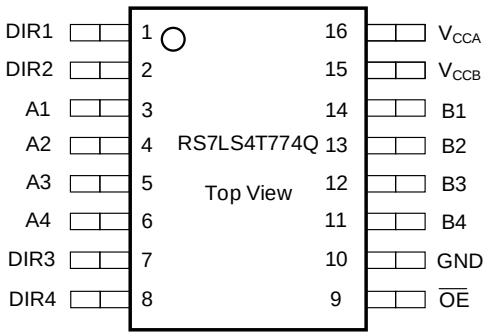

Figure 2. TSSOP16, Top View

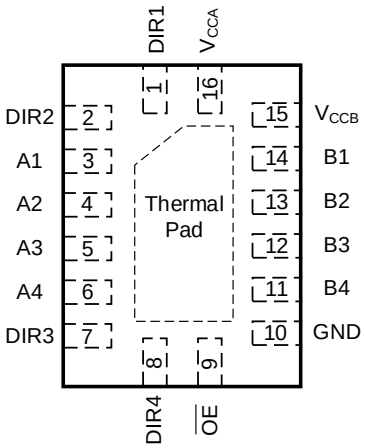

Figure 3. QFN16L, Top View

Table 1. Pin Functions

PINS		TYPE [1]	Description
NAME	No.		
DIR1	1	I	Direction-control input referenced to V_{CCA}, controls signal flow for the first (A1/B1) I/O channels.
DIR2	2	I	Direction-control input referenced to V_{CCA} , controls signal flow for the second (A2/B2) I/O channels.
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
DIR3	7	I	Direction-control input referenced to V_{CCA} , controls signal flow for the third (A3/B3) I/O channels.
DIR4	8	I	Direction-control input referenced to V_{CCA} , controls signal flow for the fourth (A4/B4) I/O channels.
$\overline{OE}$	9	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	10	—	Ground.
B4	11	I/O	Input/output B4. Referenced to V_{CCB}.
B3	12	I/O	Input/output B3. Referenced to V_{CCB}.
B2	13	I/O	Input/output B2. Referenced to V_{CCB}.
B1	14	I/O	Input/output B1. Referenced to V_{CCB}.
V_{CCB}	15	—	B-port supply voltage. 1.65V ≤ V_{CCB} ≤ 5.5V.
V_{CCA}	16	—	A-port supply voltage. 1.1V ≤ V_{CCA} ≤ 1.95V.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Symbol	Parameter		MIN	MAX	Unit
V_{CCA}	Supply voltage		–0.5	2.5	V
V_{CCB}	Supply voltage		-0.5	6.5	
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	2.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	2.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	2.5	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	-0.5	V_{CCA} + 0.5	V
		B port	-0.5	V_{CCB}+ 0.5	
I_{IK}	Input clamp current	VI< 0	–0.5	–50	mA
I_{OK}	Output clamp current	VO < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			+150	°C
T_{stg}	Storage temperature		-65	+150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

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ESD Ratings

Symbol	Parameter		Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

Symbol	Parameter		V_{CCI}	V_{CCO}	MIN	MAX	Unit
V_{CCA}	Supply voltage				1.1	1.95	V
V_{CCB}	Supply voltage				1.65	5.5	V
V_{IH}	High-level input voltage	Data inputs(4)	1.1V to 1.95V		V_{CCI} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 5.5V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.1V to 1.95V			V_{CCI} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 5.5V			0.8	
V_{IH}	High-level input voltage	Control Inputs (referenced to V_{CCA}) (5) (DIRx, $\overline{OE}$)	1.1V to 1.95V		V_{CCA} × 0.85		V
V_{IL}	Low-level input voltage	Control Inputs (referenced to V_{CCA}) (5) (DIRx, $\overline{OE}$)	1.1V to 1.95V			V_{CCA} × 0.35	V
V_I	Input voltage				0	V_{CCI}	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	V_{CCO}	
I_{OH}	High-level output current			1.1V to 1.3V		-3	mA
				1.4V to 1.6V		-6	
				1.65V to 1.95V		-8	
				2.3V to 2.7V		-9	
				3V to 5.5V		-12	
I_{OL}	Low-level output current			1.1V to 1.3V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 5.5V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				-40	125	℃

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CC}I values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		V_{CCA}	V_{CCB}	TA=25℃			-40℃~125℃			Unit
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100μA	V_I=V_{IH}	1.1V to 1.95V	1.65V to 5.5V	0		V_{CC}	V_{CCO} – 0.2			V
		I_{OH} = –3mA		1.2V	1.65V to 5.5V		0.95					
		I_{OH} = –6mA		1.5V	1.65V to 5.5V							
		I_{OH} = –8mA		1.8V	1.65V to 5.5V							
		I_{OH} = –12mA		1.95V	1.65V to 5.5V							
V_{OL}		I_{OH} = 100μA	V_I=V_{IL}	1.1V to 1.95V	1.65V to 5.5V							V
		I_{OH} = 3mA		1.2V	1.65V to 5.5V		0.25					
		I_{OH} = 6mA		1.5V	1.65V to 5.5V							
		I_{OH} = 8mA		1.8V	1.65V to 5.5V							
		I_{OH} = 12mA		1.95V	1.65V to 5.5V							
I_I	Control inputs	V_I=V_{CCA} or GND		1.1V to 1.95V	1.65V to 5.5V		±0.1	±0.25			±1	uA
I_{off}	A or B port	V_I or V_O = 0 to VCC		0V	0V to 5.5V		±0.1	±1			±5	uA
				0V to 1.95V	0V		±0.1	±1			±5	
I_{OZ}	A or B port	V_O = V_{CCO} or GND, V_I = V_{CCI} or GND, $\overline{OE}$=V_{IH}		1.95	5.5V		±0.5	±2.5			±5	uA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0		1.1V to 1.95V	1.65V to 5.5V						8	uA
				0V	0V to 5.5V				-2			
				0V to 1.95V	0V						8	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0		1.1V to 1.95V	1.65V to 5.5V						8	uA
				0V	0V to 5.5V						8	
				0V to 1.95V	0V				-2			
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0		1.1V to 1.95V	1.65V to 5.5V						16	uA
C_i	Control inputs	V_I = V_{CCA} or GND		1.95V	5.5V		2.5				4.5	pF
C_{io}	A or B port	V_I = V_{CCA} or GND		1.95V	5.5V		5				7	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation.

AC Electrical Characteristics

Switching Characteristics: VCCA = 1.2V ± 0.1V

See Figure 4 and Table 2 for test circuit and loading. See Figure 5 and Figure 6 for measurement waveforms.

Parameter	From	To	Test Conditions	V_{CCB}= 1.8V±0.1V		V_{CCB}= 2.5V±0.15V		V_{CCB}= 3.3V±0.2V		V_{CCB}= 5.5V±0.3V		Unit
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	T_A=25℃	1	4.5	1	4	0.5	4	0.5	4	ns
t_{PHL}				1	4	0.5	4.5	0.5	6	0.5	6	
t_{PLH}	B	A		1	6	1	6	1	6	1	6	
t_{PHL}				1	4.5	0.5	4	0.5	4	0.5	4	
t_{PZH}	$\overline{OE}$	A		1	8	1	8	1	8.5	1	8.5	
t_{PZL}				1.5	9	1	9	1	9	1	9	
t_{PZH}	$\overline{OE}$	B		1	6.5	1	9.5	0.5	30	0.5	30	
t_{PZL}				1	7	1	8.5	0.5	24	0.5	24	
t_{PHZ}	$\overline{OE}$	A		2	6.5	1.5	6.5	2	6.5	2	6.5	
t_{PLZ}				2.5	6.5	2	6.5	2	6.5	2	6.5	
t_{PHZ}	$\overline{OE}$	B		2	6	1.5	5	2	6.5	2	6.5	
t_{PLZ}				2.5	5.5	1.5	5	2	6	2	6	

Switching Characteristics: VCCA = 1.5V ± 0.1V

See Figure 4 and Table 2 for test circuit and loading. See Figure 5 and Figure 6 for measurement waveforms.

Parameter	From	To	Test Conditions	V_{CCB}= 1.8V±0.1V		V_{CCB}= 2.5V±0.15V		V_{CCB}= 3.3V±0.2V		V_{CCB}= 5.5V±0.3V		Unit
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	T_A=25℃	0.3	5.2	0.4	4.2	0.4	4.2	0.4	4.2	ns
t_{PHL}				0.3	5.2	0.4	4.2	0.4	4.2	0.4	4.2	
t_{PLH}	B	A		0.5	6	0.4	5.7	0.3	5.6	0.3	5.6	
t_{PHL}				0.5	6	0.4	5.7	0.3	5.6	0.3	5.6	
t_{PZH}	$\overline{OE}$	A		1.1	9.5	0.7	9.4	0.4	9.4	0.4	9.4	
t_{PZL}				1.1	9.5	0.7	9.4	0.4	9.4	0.4	9.4	
t_{PZH}	$\overline{OE}$	B		1.1	7.7	0.9	5.8	0.9	5.6	0.9	5.6	
t_{PZL}				1.1	7.7	0.9	5.8	0.9	5.6	0.9	5.6	
t_{PHZ}	$\overline{OE}$	A		1.5	10.2	1.3	10.2	1.6	10.2	1.6	10.2	
t_{PLZ}				1.5	10.2	1.3	10.2	1.6	10.2	1.6	10.2	
t_{PHZ}	$\overline{OE}$	B		1.9	9.1	1.4	7.4	1.2	7.6	1.2	7.6	
t_{PLZ}				1.9	9.1	1.4	7.4	1.2	7.6	1.2	7.6	

Switching Characteristics: VCCA = 1.8 V ± 0.15V

See Figure 4 and Table 2 for test circuit and loading. See Figure 5 and Figure 6 for measurement waveforms.

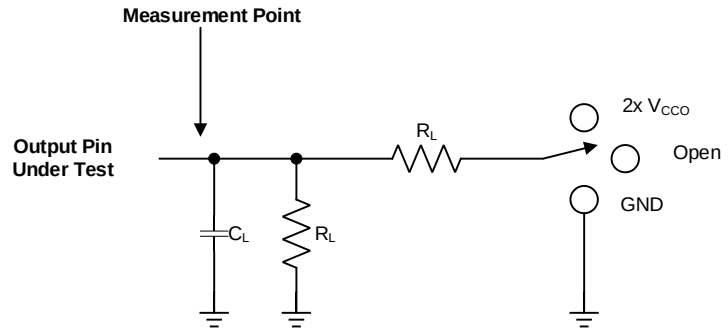
Parameter	From	To	Test Conditions	V_{CCB}= 1.8V±0.1V		V_{CCB}= 2.5V±0.15V		V_{CCB}= 3.3V±0.2V		V_{CCB}= 5.5V±0.3V		Unit
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	T_A=25℃	0.3	5.2	0.4	4.2	0.4	4.2	0.4	4.2	ns
t_{PHL}				0.3	5.2	0.4	4.2	0.4	4.2	0.4	4.2	
t_{PLH}	B	A		0.5	6	0.4	5.7	0.3	5.6	0.3	5.6	
t_{PHL}				0.5	6	0.4	5.7	0.3	5.6	0.3	5.6	
t_{PZH}	$\overline{OE}$	A		1.1	9.5	0.7	9.4	0.4	9.4	0.4	9.4	
t_{PZL}				1.1	9.5	0.7	9.4	0.4	9.4	0.4	9.4	
t_{PZH}	$\overline{OE}$	B		1.1	7.7	0.9	5.8	0.9	5.6	0.9	5.6	
t_{PZL}				1.1	7.7	0.9	5.8	0.9	5.6	0.9	5.6	
t_{PHZ}	$\overline{OE}$	A		1.5	10.2	1.3	10.2	1.6	10.2	1.6	10.2	
t_{PLZ}				1.5	10.2	1.3	10.2	1.6	10.2	1.6	10.2	
t_{PHZ}	$\overline{OE}$	B		1.9	9.1	1.4	7.4	1.2	7.6	1.2	7.6	
t_{PLZ}				1.9	9.1	1.4	7.4	1.2	7.6	1.2	7.6	

Parameter Measurement Information

Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- F = 10MHz
- Z_O = 50Ω
- Δt/ΔV ≤ 1ns/V



A. CL includes probe and jig capacitance.

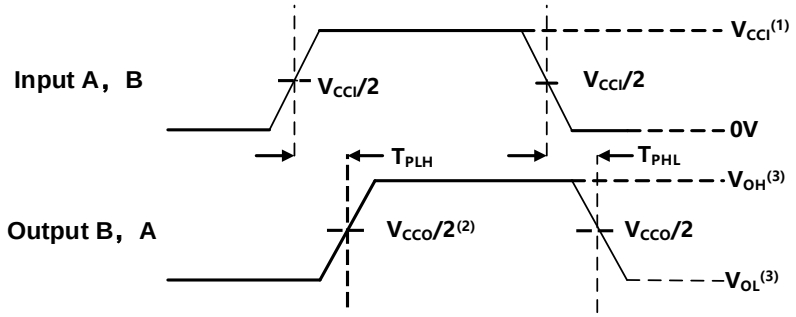
Figure 4. Load Circuit

Table 2. Load Circuit Parameters

Test Parameter		S1
t_{pd}	Propagation (delay) time	Open
t_{PZL}, t_{PLZ}	Enable time, disable time	2 × V_{CCO}
t_{PZH}, t_{PHZ}	Enable time, disable time	GND

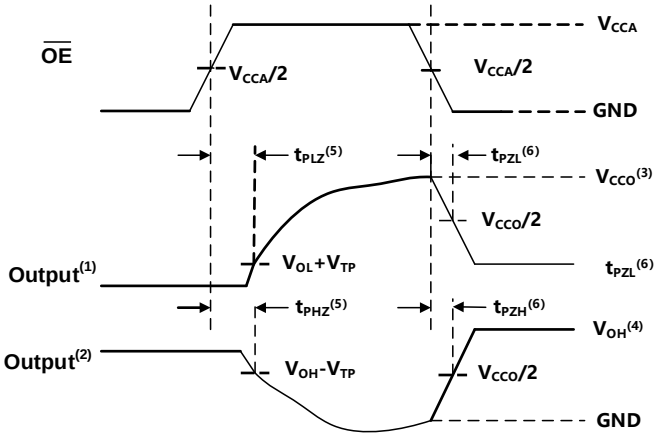
Table 3. Load Circuit Conditions

V_{CCO}	R_L	C_L	V_{TP}
1.2V±0.1V	2kΩ	15pF	0.1V
1.5V ± 0.1V	2kΩ	15pF	0.1V
1.8V ± 0.15V	2kΩ	15pF	0.15V
2.5V±0.2V	2kΩ	15pF	0.15V
3.3V±0.3V	2kΩ	15pF	0.3V
5.5V±0.3V	2kΩ	15pF	0.3V



(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.
(4) t_{PLH} and t_{PHL} are the same as t_{pd}.
(5) The outputs are measured one at a time, with one transition per measurement.

Figure 5. Propagation Delay



(1) Output waveform on the condition that input is driven to a valid Logic Low.
(2) Output waveform on the condition that input is driven to a valid Logic High.
(3) V_{CCO} is the supply pin associated with the output port.
(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.
(5) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
(6) t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6. Enable Time And Disable Time

Detailed Description

● Overview

The RS7LS4T774Q is a 4-bit, dual-supply, noninverting, bi-directional voltage level translation. Pins An and control pins (DIR1, DIR2, DIR3, DIR4 and $\overline{OE}$) are support by V_{CCA} and pins Bn are support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.1V to 1.95V, while the B port can accept I/O voltages from 1.65V to 5.5V. A high on DIR allows data transmission from An to Bn and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both An and Bn are in the high-impedance state.

● Functional Block Diagram

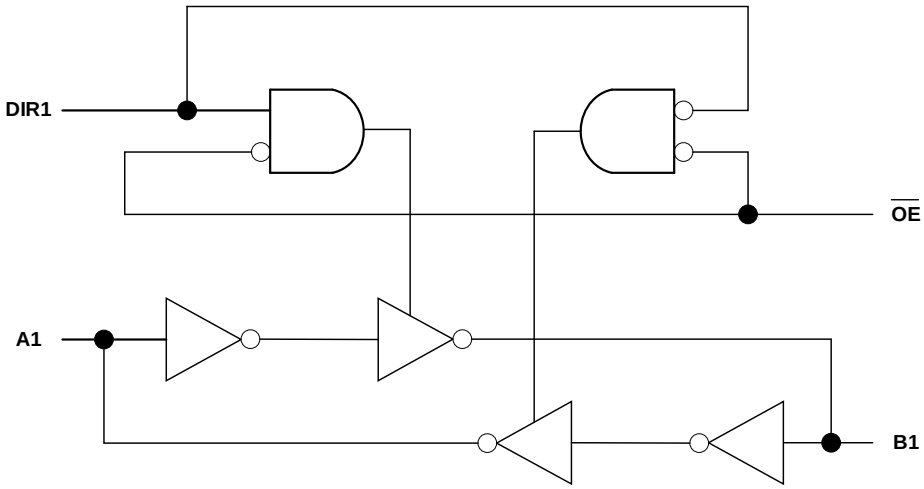


Figure 7. Logic Diagram (Positive Logic)

● Feature Description

1. Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Respective Power-Supply Range: VCCA at 1.1V to 1.95V and VCCB at 1.65V to 5.5V.

Both VCCA (1.1V to 1.95V) and VCCB (1.65V to 5.5V) can be supplied at any voltage within their respective ranges, making the device suitable for translating between various low-voltage and standard-voltage nodes (1.2V, 1.8V, 2.5V, 3.3V, and 5V).

2. Support High-Speed Translation

RS7LS4T774Q can support high data rate application. The translated signal data rate can be up to 380Mbps when signal is translated from 1.8V to 3.3V.

3. I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

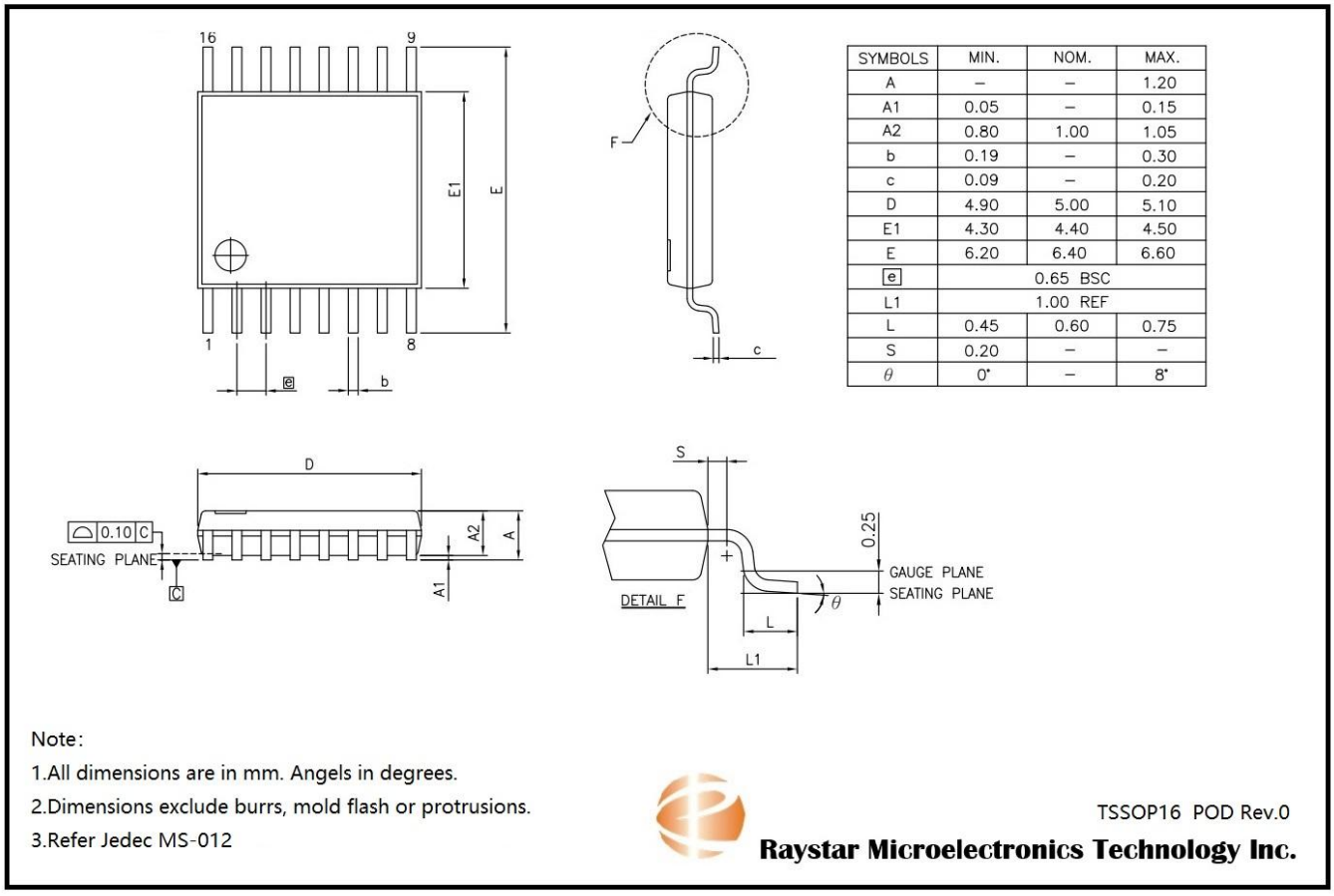
● Device Functional Modes

Table 4. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

Package Information

TSSOP16

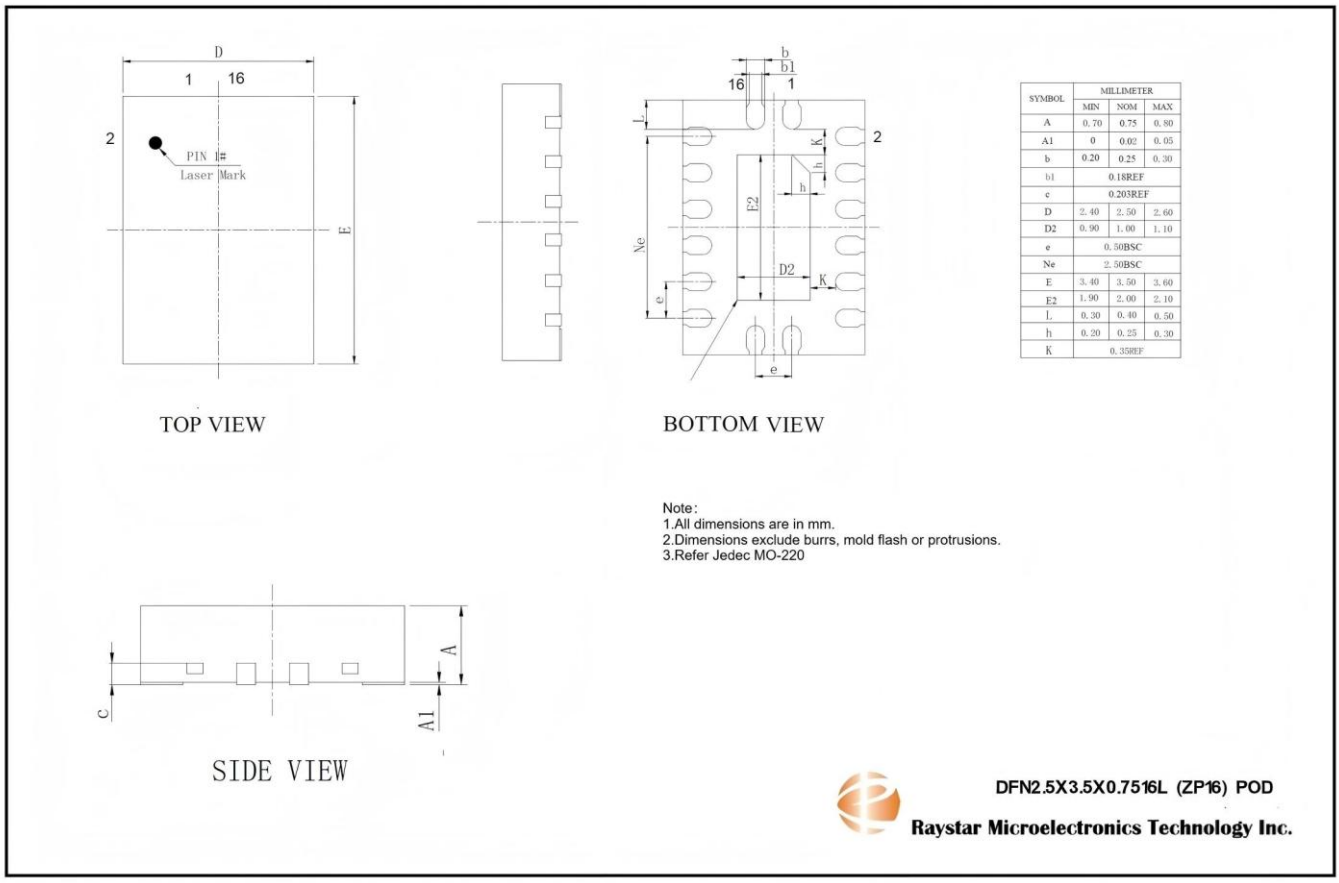


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012

TSSOP16 POD Rev.0
Raystar Microelectronics Technology Inc.

QFN16L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	2.40	2.50	2.60
D2	0.90	1.00	1.10
e	0.50BSC		
Ne	2.50BSC		
E	3.40	3.50	3.60
E2	1.90	2.00	2.10
L	0.30	0.40	0.50
h	0.20	0.25	0.30
K	0.350EF		

Revision History

Revision	Description	Date
V0.9	Preliminary release	2025/04/10
V1.0	Update the minimum voltage of VIL	2026/01/27