Features

- Built in frequency adjusted 32.768-kHz crystal unit.
- Real-time clock function， Clock/calendar function, Wakeup timer function, alarm interrupt function, etc.
- User RAM: Built in 128-bit RAM
- Frequency output function:32.768 kHz, 1024 Hz, 1Hz
- Digital offset function: Adjustment range is -195.3~+192.3 (10^{-6})
- Interface type: I2C-Bus
- Interface voltage range:1.6 V~5.5 V
- Timekeeper voltage range:1.1 V~5.5 V
- AEC-Q100 qualified. PPAP capable, and manufactured in IATF 16949 certified facilities.

Description

This is a real-time clock module of the serial interface system that incorporates a 32.768 kHz crystal oscillator.

The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, interval timer, and time update interruption, among other features.

All of these many functions are implemented in a thin, compact SOP package, which makes it suitable for various kinds of small electronic devices.

Ordering Information

Ordering Code	Package	Description
RS4C8010QWE	SOP8	Frequency stability: 5±23ppm
RS4C8010QWE-B	SOP8	Frequency stability: ±10ppm

Notes:
E = Pb-free and Green

Block Diagram

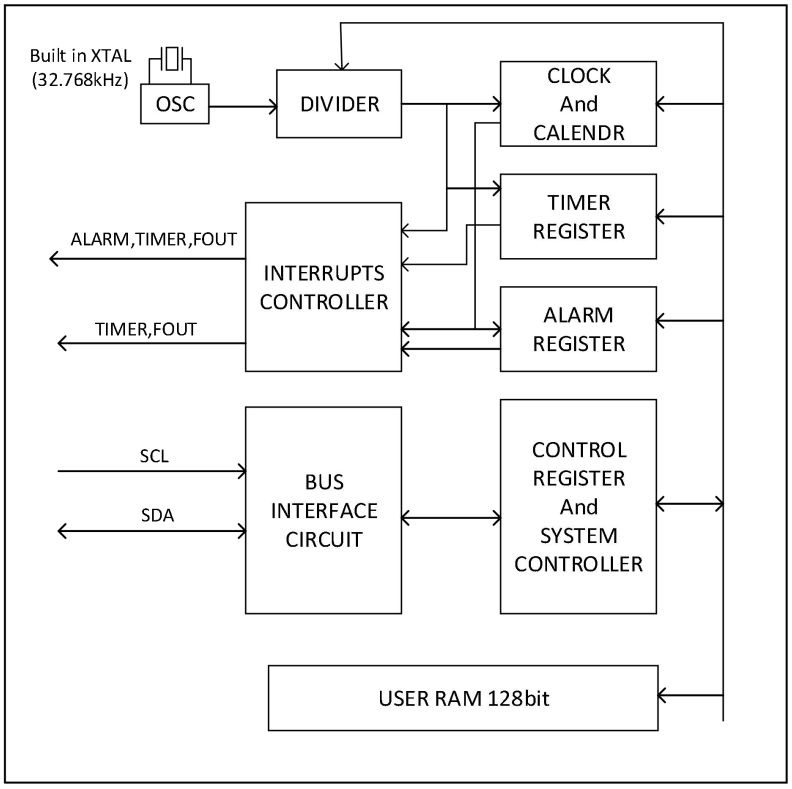


Figure 1 Block Diagram

Pin Configuration

Figure 2 Pin Configuration

Pin Name	Pin No.	Type	Description
IRQ2	3	Output	This pin outputs interrupt signals ("L" level) for timer and FOUT. This is a CMOS output.
GND	4	GND	Ground
SDA	5	I/O	Serial data address input/output
SCL	6	Input	Serial clock.
IRQ1	7	Output	This pin outputs interrupt signals ("L" level) for alarm, timer, time update, and FOUT. This is an N-ch open-drain output.
V_{DD}	8	Power	Supply voltage
N.C.	1,2	-	No connection

Notes:
1.Input pins are able to input up to 5.5V regardless of VDD applied voltage.
2.Open drain pins are able to Pull-up to 5.5V regardless of VDD applied voltage.
3.Connect a bypass capacitor rated at least 0.1μF between power supply pins and GND pin.

Typical Application Circuit

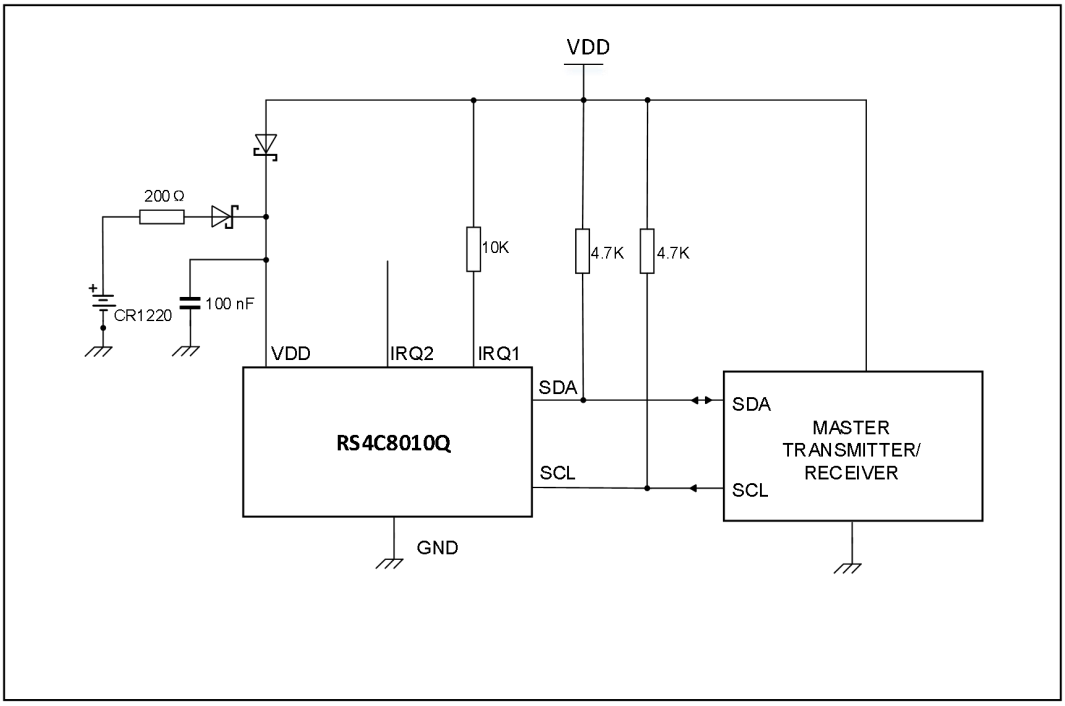


Figure 3 Typical Application Circuit

Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage	VDD	Between VDD and GND	-0.3~6.5	V
Input voltage	VIN	SCL, SDA	-0.3~6.5	V
Output voltage 1	VOUT1	IRQ2	-0.3~VDD+0.3	V
Output voltage 2	VOUT2	SDA, IRQ1	-0.3~6.5	V
Storage temperature	TSTG	When stored separately, without packaging	-55 to 125	°C

Recommended operation conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VACC	-	1.6	3	5.5	V
Clock supply voltage	VCLK	-	1.1	3	5.5	V
Low voltage detection	VLOW	-			1.1	V
Applied voltage when OFF	VPUP	SDA, IRQ1pin			5.5	V
Operating temperature	TOPR	No condensation	-40	25	125	°C

Frequency Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output frequency	fo			32.768		kHz
Frequency stability (△f / f)	RS4C8010QWE	Ta = +25 °C VDD = 3.0 V		5 ± 23		×10^{-6}
	RS4C8010QWE-B	Ta = +25 °C VDD = 3.0 V		± 10		×10^{-6}
Frequency/voltage characteristics	f / V	Ta = +25 °C VDD = 1.2 V ~ 5.5 V	-2		2	×10^{-6}/V
Frequency/temperature characteristics	Top	Ta = -20 °C ~ +70 °C VDD = 3.0 V; +25 °C reference	-120		10	×10^{-6}
Oscillation start time	tSTA	Ta = ±0 °C ~ +50 °C VDD = 1.6 V ~ 5.5 V			1	s
		Ta = -40 °C ~ +85 °C VDD = 1.6 V ~ 5.5 V			3	s
Aging	fa	Ta = +25 °C, VDD = 3.0 V; first year	-5		5	× 10^{-6} /year

DC Electrical Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	IDD1	Input pins are "L" fSCL = 0 Hz, IRQ1,2 = OFF TSEL2="1"	VDD = 5 V		450	600	nA
Current consumption (2)	IDD2		VDD = 3 V		400	550	
Current consumption (3)	IDD3	fSCL = 0 Hz, IRQ2 = OFF, IRQ1: 32.768 kHz ON	VDD = 5 V		0.6	1.1	uA
Current consumption (4)	IDD4		VDD = 3 V		0.52	0.9	
Current consumption (5)	IDD5	fSCL = 0 Hz, IRQ1 = OFF, IRQ2: 1024 Hz ON, CL = 15 pF	VDD = 5 V		0.45	1.1	uA
Current consumption (6)	IDD6		VDD = 3 V		0.4	0.9	
High-level input voltage	VIH	SCL, SDA		0.8×VDD		5.5	V
Low-level input voltage	VIL	SCL, SDA		GND-0.3		0.2×VDD	V
High-level output voltage	VOH1	IRQ2 pin	VDD=5 V, IOH=-1 mA	4.5		GND +5.0	V
	VOH2		VDD =3 V, IOH=-0.5 mA	2.7		GND +3.0	
Low-level output voltage	VOL1	SDA, IRQ2 pin	VDD =5 V, IOL=1 mA	GND		GND +0.5	V
	VOL2		VDD =3 V, IOL=0.5 mA	GND		GND +0.3	
	VOL4	IRQ1 pin	VDD =5 V, IOL=1 mA	GND		GND+0.25	
	VOL5		VDD =3 V, IOL=1 mA	GND		GND +0.4	
	VOL6	SDA pin	VDD≥ 2 V, IOL=3.0 mA	GND		GND +0.4	
Input leakage current	ILK	Input pin, VIN = VDD or GND		-0.1		0.1	uA
Output leakage current	IOZ	Output pin, VOUT = VDD or GND		-0.1		0.1	uA

AC Electrical characteristics

AC characteristics (1)

Item	Symbol	Standard-Mode fSCL=100 kHz		Fast-Mode fSCL=400 kHz		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL		100		400	kHz
Start condition setup time	tSU;STA	4.7		0.6		μs
Start condition hold time	tHD;STA	4		0.6		μs
Data setup time	tSU;DAT	250		100		ns
Data hold time	tHD;DAT	0		0		ns
Stop condition setup time	tSU;STO	4		0.6		μs
Bus idle time between start condition and stop condition	tBUF	4.7		1.3		μs
Time when SCL = "L"	tLOW	4.7		1.3		μs
Time when SCL = "H"	tHIGH	4		0.6		μs
Rise time for SCL and SDA	tr		1		0.3	μs
Fall time for SCL and SDA	tf		0.3		0.3	μs
Allowable spike time on bus	tSP		50		50	ns

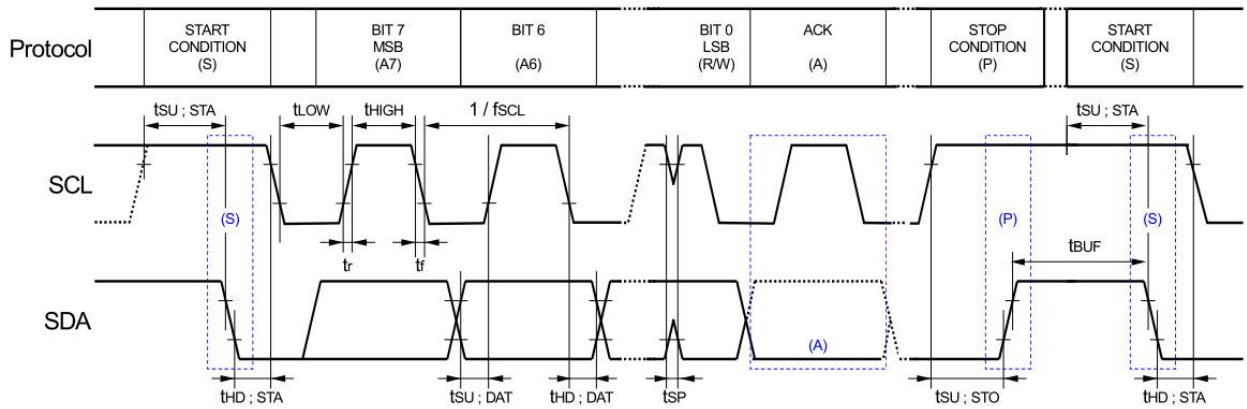


Figure 4 IIC-bus timing diagram

Caution: When communication of I2C-Bus is started, consumption electric currents increase.
When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds.
If such communication requires 1 seconds or longer, the I2C-Bus interface is reset by the internal bus timeout function.

AC characteristics (2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT symmetry (IRQ2)	SYM	50% VDD Level	40	50	60	%

Note of usage in power on / Off (3)

Characteristic for the fluctuation of the power supply

tR1 is restrictions to validate power-on reset. When cannot keep this standard, power-on reset does not work normally. It is necessary to initial setting by the software command.
Repeated ON/OFF of the power supply in short term, the power-on reset becomes unstable. After power-OFF, keep a state of VDD=GND more than 60 seconds to validate power-on reset. When it is impossible, please perform initial setting by the software command

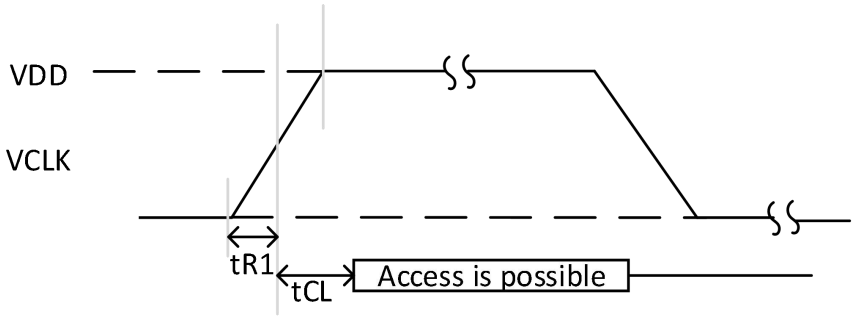


Figure 5 Power on reset

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	tR1	GND ~VDD	1	-	100	us / V
access wait time (Initial power on)	tCL		40	-	-	ms

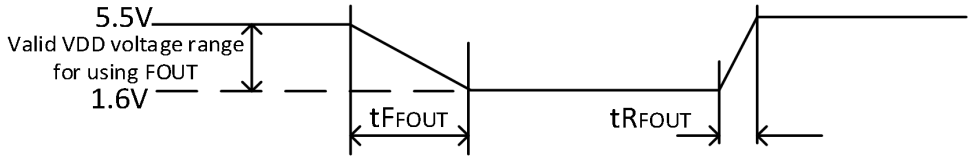
A power-on reset procedure by the software command

1) Power- on
2) Wait: At least 40ms.
3) Dummy read. ∗1
4) Check VLF bit = “1”
5) Write 00h Address: Reg-1Fh
6) Write 80h Address: Reg-1Fh
7) Write D3h Address: Reg-60h
8) Write 03h Address: Reg-66h
9) Write 02h Address: Reg-6Bh
10) Write 01h Address: Reg-6Bh

END

∗1 Dummy read
The location of the address is arbitrary.
Do not check ACK/NACK from RS4C8010Q.

A disappearance of the FOUT output when the voltage sharply went up and down.
For example, VDD voltage of the RS4C8010Q is come and go between Main power and backup battery.
The clock output from output pins disappears then during several milli-seconds when a sharp voltage change happens.
Please check that there is not a problem by this characteristic on your system.
A reference example of a power up and down timing without affect to FOUT.



tFFOUT Please make speed to descend of a power supply voltage loose than 4ms/V
tRFOUT Please make speed to rise of a power supply voltage loose than 4ms/V

Restrictions on Access Operations during Power-on Initialization and Recovery from Backup (4)

• Note the following caution points concerning access operations during power-on initialization or when restoring the power supply voltage from backup mode (here after referred to as "switching to the operating voltage").

1) Before switching to the operating voltage, read the VLF-bit (which indicates the RTC error status).
2) Initialization is required when the value read from the VLF-bit is "VLF = 1 (error status)".
Before initializing in response to this VLF = "1" result, we recommend first waiting for the internal oscillation stabilization time (see the tSTA standard) to elapse.

Initialization is required when the status after reading a VLF-bit value of "1" is either of the following. (Status 1) During power-on initialization (Status 2) When the clock setting is invalid, such as due to a voltage drop during backup

Application Notes

Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1uF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electronic noise near this module.

(2) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VIO or GND.

Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 ° C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

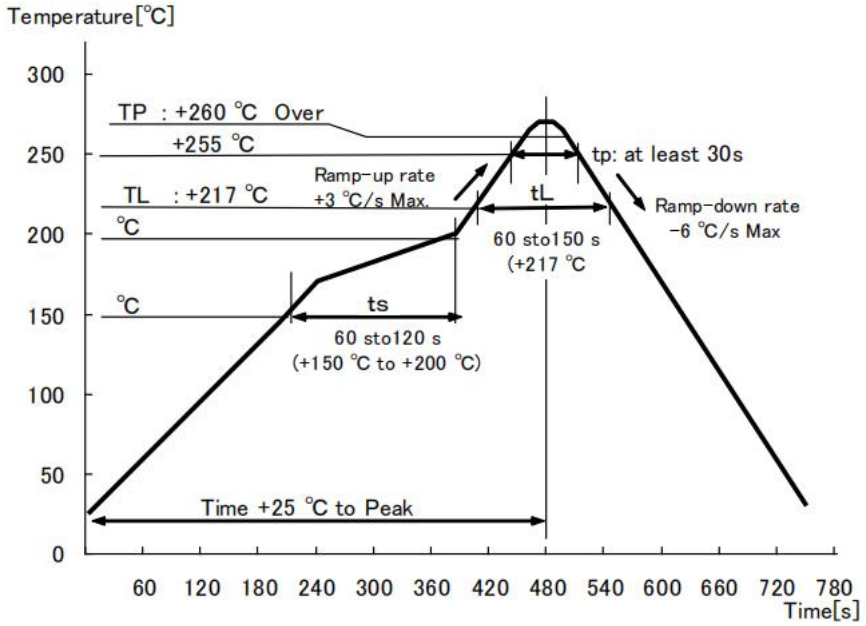


Figure 6 Soldering heat resistance

(2) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside

of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

Overview of Functions and Description of Registers

Note: The initialization of the register is necessary about the unused function and Reserved bit

Overview of Functions

(1) Clock functions

This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data. Any (two-digit) year that is a multiple of 4 is treated as a leap year immunization start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.

(2) Wakeup Timer Interrupt function

The wakeup timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14us and 65535 hours.

When an interrupt event is generated, the IRQ2 pin goes to low level ("L") and "1" is set to the TF bit to report that an event has occurred.

(3) Long-Timer function

It is able to use wakeup timer interrupt function as Long-Timer that deals with for approx 15 years.

(4) Alarm interrupt function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the IRQ1 pin goes to low level to indicate that an event has occurred.

(5) Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock. When an interrupt event is generated, the IRQ1 pin goes to low level ("L") and "1" is set to the UF bit to report that an event has occurred.

(6) Frequency stop detection function (VLF-bit)

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop.

(7) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the IRQ1, IRQ2 pin.

(8) Digital offset function

The clock precision can be set ahead or behind. The minimum resolution is 3.05×10^{-6} and it can adjust it in the range of $+192.3\times10^{-6}$ from -195.3×10^{-6}. When calculate compensation value from frequency accuracy or clock accuracy, please refer to accuracy after initialized a register by all means.

(9) User RAM

RAM register is read/write accessible for any data.

Register table

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	○	40	20	10	8	4	2	1
11	MIN	○	40	20	10	8	4	2	1
12	HOUR	○	○	20	10	8	4	2	1
13	WEEK	○	6	5	4	3	2	1	0
14	DAY	○	○	20	10	8	4	2	1
15	MONTH	○	○	○	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	Reserved	-	-	-	-	-	-	-	-
	Setting data	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**
18	MIN Alarm	AE	40	20	10	8	4	2	1
19	HOUR Alarm	AE	•	20	10	8	4	2	1
	WEEK Alarm		6	5	4	3	2	1	0
1A	DAY Alarm	AE	•	20	10	8	4	2	1
1B	Timer Counter 0	128	64	32	16	8	4	2	1
1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	AF	○	VLF	○
1F	Control Register	***TEST***	STOP	UIE	TIE	AIE	TSTP	-	-
	Setting data	**0**	STOP	UIE	TIE	AIE	TSTP	**0**	**0**

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20 | 2F	RAM	User Register 128 bit (16 word x 8 bit)							

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1
31	Reserved	○	○	○	-	-	-	-	-
	Setting data	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
32	IRQ Control	○	-	-	-	○	TMPIN	FOPIN1	FOPIN0
	Setting data	**0**	**0**	**0**	**0**	**0**	TMPIN	FOPIN1	FOPIN0

Note：During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.
When doing this, be careful to avoid setting incorrect data as the date or time, as timed operations cannot be guaranteed if incorrect date or time data has been set.

(1) During the initial power-on (from 0 V), the power-on reset function sets "1" to the VLF bit.

* Since the value of other registers is undefined at this time, be sure to reset all registers before using them.

(2) The ***TEST***, bit are Raystar test bits. Always leave this bit value as "0" except when testing.

* Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
* The four ***TEST**** bits are undefined when read. Those bits should be masked after being read.

(3) The ' ○ ' mark indicates a write-prohibited bit, which returns a "0" when read.

(4) The ' • ' mark indicates a read/write-accessible RAM bit for any data.

(5) The '-' mark is a Reserved bit. It is necessary to write in Setting data at the time of initialization.

(6) User Register is a free register.

Description of registers

(1) Clock and calendar counter

This is counter registers from a second to year.

(2) RAM registers

This RAM register is read/write accessible for any data in the range from 00 h to FF h.

(3) Alarm Function and registers

The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.

(4) wakeup Timer setting and Timer counter register

This register is used to set the default (preset) value for the counter.
To use the wakeup timer interrupt function, TE, TF, TIE, TSEL2,TSEL1, TSEL0,TMPIN bits are set and used. When the wakeup timer interrupt function is not being used, the wakeup timer control register can be used as a RAM register. In such cases, stop the wakeup timer function by writing "0" to the TE and TIE bits.

(5) Function-related register 1

1) FSEL1, FSEL0 bit
A combination of the FSEL1 and FSEL0 bits is used to select the frequency to be output.
The choice is possible by a combination of FSEL-bits select the frequency of clock output or inhibits the clock output.

2) USEL, UF, UIE bit
This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.

3) TE, TF, TIE, TSEL2, TSEL1, TSEL0, TSTP bit
These bits are used to control operation of the wakeup timer interrupt function.

4) WADA, AF, AIE bit
These bits are used to control operation of the alarm interrupt function.

5) TEST bit
TEST bit is prepared for shipping inspection. Always leave this bit value as "0" except when testing.

6) VLF bit
This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop.

7) STOP bit
This bit is to stop a timekeeping operation. In the case of “STOP bit = 1", working is as follows a function. All the update of timekeeping and the calendar operation stops. With it, an update interrupt event does not occur at an alarm interrupt and the time.

The part of the wakeup timer interrupt function stops. A count stops the source clock setting of the timer in case of "64Hz, 1Hz, 1/60Hz, 1/3600Hz".

The effect of STOP bit to FOUT functions. When STOP = "1", 32768Hz output is possible. But 1Hz and 1024Hz output is disabled.

1) unction-related register 2.

FOPIN1, FOPIN0 bit

This bit selects destination (IRQ1 or IRQ2) of FOUT.

TMPIN bit

This bit selects destination (IRQ1 or IRQ2) of wakeup timer function.

2) Reserved bit

The ' - ' mark has to write in specified fixed value in the case of initialization by all means. Writing data as follows.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
17	Reserved	-	-	-	-	-	-	-	-
	Setting data	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**
1F	Control Register	**TEST**	STOP	UIE	TIE	AIE	TSTP	-	-
	Setting data	**0**	STOP	UIE	TIE	AIE	TSTP	**0**	**0**

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
31	Reserved	○	○	○	-	-	-	-	-
	Setting data	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
32	IRQ Control	○	-	-	-	○	TMPIN	FOPIN1	FOPIN0
	Setting data	**0**	**0**	**0**	**0**	**0**	TMPIN	FOPIN1	FOPIN0

The ' ○ 'mark indicates a write-prohibited bit, which returns a "0" when read.

How to use

Clock calendar explanation

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end. Therefore it recommends that the access to a clock calendar has continuous access by the auto increment function.

Setting example: Sun, 29-Feb-88 17:39:45 (leap year)

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	1	0	0	0	1	0	1
11	MIN	0	0	1	1	1	0	0	1
12	HOUR	0	0	0	1	0	1	1	1
13	WEEK	0	0	0	0	0	0	0	1
14	DAY	0	0	1	0	1	0	0	1
15	MONTH	0	0	0	0	0	0	1	0
16	YEAR	1	0	0	0	1	0	0	0

*Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

(1) Clock counter

1) [SEC] [MIN] register

These registers are 60-base BCD counters. These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.

When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512Hz ~1 Hz) is cleared to 0.

2) [HOUR] register

This register is a 24-base BCD counter (24-hour format). These registers are incremented at the timing when carry is generated from a lower register.

(2) Week counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.

The day data values are counted as: Day 01h →Day 02h→Day 04h →Day 08h →Day 10h →Day 20h →Day 40h →Day 01h →Day 02h, etc.

It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.

The setting example of the week registers value.

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data h
Sunday	0	0	0	0	0	0	0	**1**	01 h
Monday	0	0	0	0	0	0	**1**	0	02 h
Tuesday	0	0	0	0	0	**1**	0	0	04 h
Wednesday	0	0	0	0	**1**	0	0	0	08 h
Thursday	0	0	0	**1**	0	0	0	0	10 h
Friday	0	0	**1**	0	0	0	0	0	20 h
Saturday	0	**1**	0	0	0	0	0	0	40

* Do not set "1" to more than one day at the same time.

(3) Calendar counter

1) [DAY], [MONTH] resister

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is 12-base BCD counter. when carry is generated from a lower register.

		Jan.	Feb.	Mar	Apr.	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Days	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

2) [YEAR] register

This register is a BCD counter for years 00 to 99.

The leap year is automatically determined, which reflects in the DAY register.

Wakeup Timer Interrupt Function

The wakeup timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 us and 65535 hours. This function can stop at one time and is available as an accumulative timer. After the interrupt occurs, the /IRQ status is automatically cleared.

(1) Related registers for function of wakeup timer interrupt function

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
1C	Timer Counter 1	**32768**	**16384**	**8192**	**4096**	**2048**	**1024**	**512**	**256**
1D	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	**TSEL2**	**TSEL1**	**TSEL0**
1E	Flag Register	○	○	UF	**TF**	AF	○	VLF	○
1F	Control Register	***TEST***	STOP	UIE	**TIE**	AIE	**TSTP**	**-**	**-**

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
32	IRQ Control	○	-	-	-	○	**TMPIN**	FOPIN1	FOPIN0

*Before entering operation settings, we recommend first clearing the TE bit to "0" .

*When the wakeup timer function is not being used, the wakeup Timer Counter0,1 register can be used as a RAM register. In such cases, stop the wakeup timer function by writing "0" to the TE and TIE bits.

1) Down counter for wakeup timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 (0001 h) to 65535 (FFFFh) can be set.

Be sure to write "0" to the TE bit before writing the preset value.

*When TE=0, read out data of timer counter is default (Preset) value.

And when TE=1, read out data of timer counter is just counting value.

But, when access to timer counter data, counting value is not held.

Therefore, for example, perform twice read access to obtain right data, and a way to

2) TSEL2, TSEL1, TESL0 bit

The combination of these three bits is used to set the countdown period (source clock) for this function.

TSEL2 (bit 2)	TSEL1 (bit 1)	TSEL0 (bit 1)	Source clock		Auto reset time tRTN
0	0	0	4096 Hz	/Once per 244.14 us	122 us
0	0	1	64 Hz	/Once per 15.625 ms	7.813 ms
0	1	0	1 Hz	/Once per second	7.813 ms
0	1	1	1/60 Hz	/Once per minute	7.813 ms
1	0	0	1/3600 Hz	/Once per hour	7.813 ms

The IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

The first countdown shortens than a source clock.

When selected 4,096Hz / 64HZ / 1Hz as a source clock, one period of error occurs at the maximum.
When selected1/60Hz / 1/3600Hz as a source clock, 1Hz of error occurs at the maximum.

3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write	0	Stops wakeup timer interrupt function.
		* Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	Starts wakeup timer interrupt function.
		* The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This bit is used to control output of interrupt signals from the IRQ1 or /IRQ" pin when a wakeup timer interrupt event has occurred.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection
		*Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z)
	1	This bit is invalid after a "1" has been written to it.
Read	0	-
	1	Wakeup timer interrupt events are detected.
		(Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the IRQ1 or IRQ2" pin when a wakeup timer interrupt event has occurred.

TIE	Data	Description
Write	0	1)When a wakeup timer interrupt event occurs, an interrupt signal is not generated.
		2)When a wakeup timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When a wakeup timer interrupt event occurs, an interrupt signal is generated
		(/IRQ status changes from Hi-z to low).

6) TSTP bit (Timer Stop)

This bit is used to stop wakeup timer count down.

operation	STOP	TSTP	Description
Write	0	0	Writing a "0" to this bit cancels stop status (restarts timer count down). The reopening value of the countdown is a stopping value
		1	Count stops.
	1	x	The count stops at the time of the setting of 64Hz, 1Hz,1/60Hz,1/3600Hz.

7) TMPIN bit

Select the destination of the timer interrupt output signal. (IRQ1 or IRQ2)

TMPIN	Data	Description
Write	0	IRQ2 pin
	1	IRQ1 pin

(2) Wakeup timer start timing

Counting down of the wakeup timer value starts at the rising edge of the SCL (ACK output) signal that occurs when the TE value is changed from "0" to "1"

(3) Wakeup timer interrupt interval (example)

The combination of the source clock settings and wakeup timer countdown setting sets interrupt interval, as shown in the following examples.

Timer Counter setting 1~65535	Source clock				
	4096 Hz TSEL2 = 0 TSEL1, 0 = 0, 0	64 Hz TSEL2 = 0 TSEL1, 0 = 0, 1	1 Hz TSEL2 = 0 TSEL1, 0 = 1, 0	1 / 60 Hz TSEL2 = 0 TSEL1, 0 = 1, 1	1 / 3600 Hz TSEL2 = 1 TSEL1, 0 = 0, 0
0	-	-	-	-	-
1	244.14 us	15.625 ms	1 s	1 min	1 h
.	.	.	.	.	.
.	.	.	.	.	.
410	100.10 ms	6.406 s	410 s	410 min	410 h
.	.	.	.	.	.
.	.	.	.	.	.
3840	0.9375 s	60.000 s	3840 s	3840 min	3840 h
.	.	.	.	.	.
.	.	.	.	.	.
4096	1.0000 s	64.000 s	4096 s	4096 min	4096 h
.	.	.	.	.	.
.	.	.	.	.	.
65535	15.9998 s	1023.984 s	65535 s	65535 min	65535 h

(4) Diagram of wakeup timer interrupt function

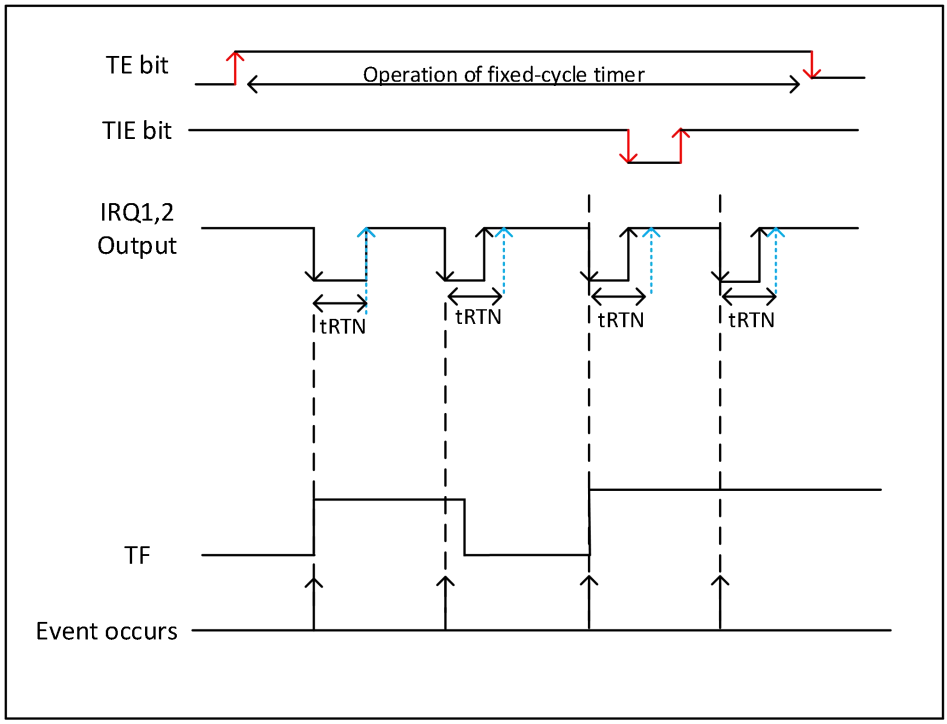


Figure 7 Diagram of wakeup timer interrupt function

After the interrupt event that occurs when the count value changes from 0001h to 0000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such date, day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to "1" and the IRQ1 pin goes to low level to indicate that an event has occurred. AF bit and IRQ output change after 1.46ms from alarm agreement at the maximum.

IRQ1=”L” output when occurs alarm interruption event is not cancelled automatically unless giving intentional cancellation and IRQ1=”L” is maintained.

(1) Related registers for Alarm interrupt functions.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
18	MIN Alarm	**AE**	40	20	10	8	4	2	1
19	HOUR Alarm	**AE**	•	20	10	8	4	2	1
1A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1D	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	**AF**	○	VLF	○
1F	Control Register	***TEST***	STOP	UIE	TIE	**AIE**	TSTP	-	-

* Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
* When the STOP bit value is "1" alarm interrupt events do not occur.
* When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
* Even if use alarm register as RAM register, inside of RTC is processed as alarm setting, therefore it is able to prevent unintentional alarm occurrence (IRQ1=” L” occurrence) due to unexpected agreement with writing data and timer condition by means of setting to AIE=”0”.

1) Alarm registers (Reg ~18h to 1Ah)

* In the WEEK alarm /Day alarm register (Reg - 1A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).
* The register that "1" was set to "AE" bit, doesn't compare alarm.
* (Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 1A): Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets. As a result, alarm occurs if only an hour and minute accords with alarm data.
* If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.
* Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	Clearing this bit to zero enables IRQ1 low output to be canceled (IRQ1 remains Hi-z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	-
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the IRQ1 pin when an Alarm interrupt event has occurred.

AIE	Data	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (IRQ1 status remains Hi-z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (IRQ1 status changes from low to Hi-z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (IRQ1 status changes from Hi-z to low).

∗The AIE bit is only output control of the IRQ1 terminal. It is necessary to clear an AF flag to cancel alarm.

(2) Examples of alarm settings

1) Example of alarm settings when "Week" has been specified (and WADA bit = "0")

Week is specified WADA bit = "0"	Week Alarm								HOUR Alarm	MIN Alarm
	bit7 AE	bit6 S	bit5 F	bit4 T	bit3 W	bit2 T	bit1 M	bit0 S		
Monday through Friday, at 7:00 AM. Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour .Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Day Alarm								HOUR Alarm	MIN Alarm
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		
	AE	·	20	10	8	4	2	1		
First of each month, at 7:00 AM Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit = 1
15th of each month, for 30 minutes each hour. Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

(3) Diagram of alarm interrupt function

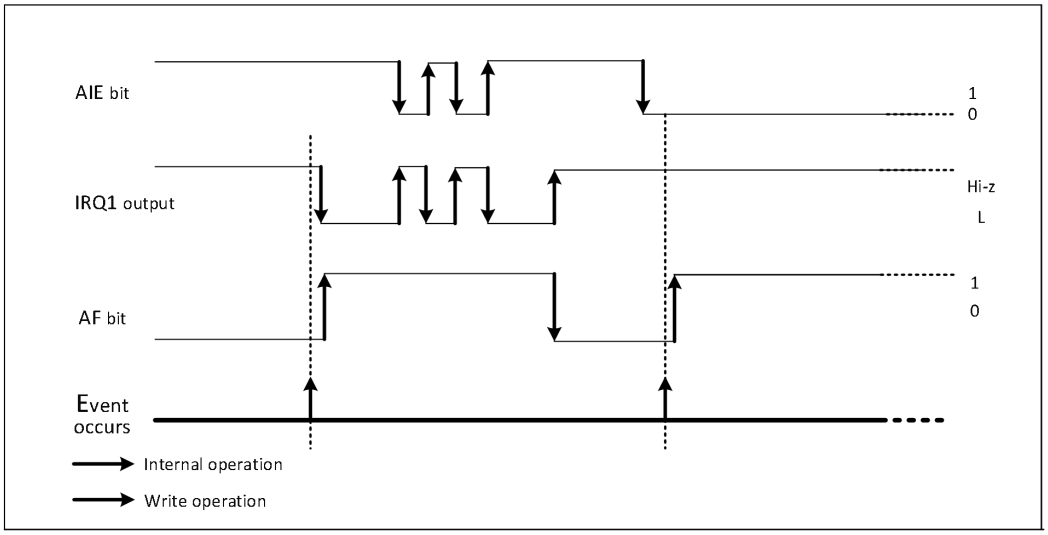


Figure 8 Diagram of alarm interrupt function

Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock. This IRQ1 status is automatically cleared

(1) Related registers for time update interrupt functions.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	**UF**	TF	AF	○	VLF	○
1F	Control Register	***TEST***	STOP	**UIE**	TIE	AIE	TSTP	-	-

* Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
* When the STOP bit value is "1" time update interrupt events do not occur.
* Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the IRQ1 pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

UF	Data	Description
Write	0	Clearing this bit to zero enables IRQ1 low output to be canceled (IRQ1 remains Hi-z) when a time update interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	-
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

UIE	Data	Description
Write / Read	0	1)Does not generate an interrupt signal. (IRQ1 remains Hi-z) 2)Cancels interrupt signal triggered by time update interrupt event (IRQ1 changes from low to Hi-z).
	1	When an Update interrupt event occurs, an interrupt signal is generated.

(2) time update interrupt function diagram

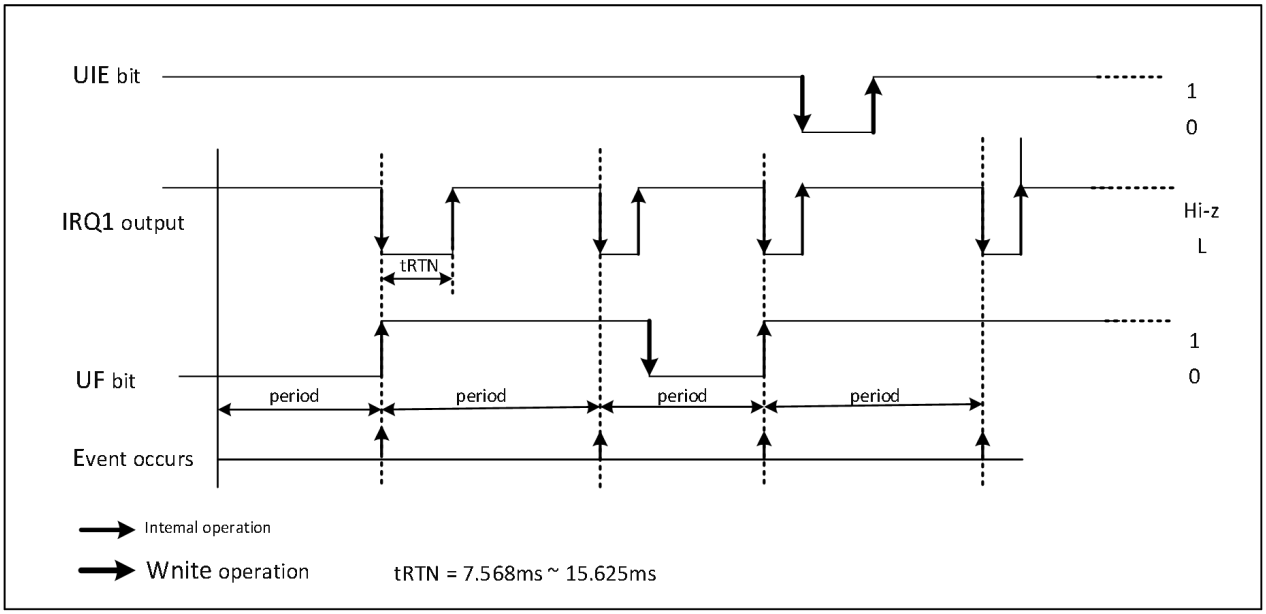


Figure 9 Time update interrupt function diagram

Frequency stops detection function

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a"0" is written to it. This function cannot detect voltage down of short time.

During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.

VLF	Data	Description
Read	0	The VLF is cleared to 0, and waiting for next low voltage detection.
	1	It is impossible to write in 1 to VLF.
Read	0	RTC register data are valid.
	1	RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

FOUT function

The clock signal can be output via the IRQ1, IRQ2 pin. When stopped the IRQ2 pin output, the pin becomes the Hi-z.

(1) FOUT control register.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	TSEL2	TSEL1	TSEL0

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
32	IRQ Control	○	-	-	-	○	TMPIN	**FOPIN1**	**FOPIN0**

By a combination of FSEL1, FSEL0, an FOUT outputs 32768Hz and 1024Hz and 1Hz and can stop the output.

(2) FOUT function table.

FOUT output pin layout and select the frequency.
At the time of the initial power-on, “0” is set to FSEL1, FSEL0.

FOPIN1	FOPIN0	Output pin	FSEL1	FSEL0	output
0	0	IRQ2 (CMOS)	0	0	OFF
			0	1	1 Hz Output
			1	0	1024 Hz Output
			1	1	Don't set it
0	1	IRQ1 (Open-Drain)	0	0	OFF
			0	1	1 Hz Output
			1	0	1024 Hz Output
			1	1	32768 Hz Output

Note: When STOP = "1", 32768Hz output is possible,but 1Hz and 1024Hz output is disabled.

Digital offset function

The clock precision can be set ahead or behind. The minimum resolution is 3.05×10^{-6} and it can adjust it in the range of $+192.3\times10^{-6}$ from -195.3×10^{-6}. When calculate compensation value from frequency accuracy or clock accuracy, please refer to accuracy after initialized a register by all means.

(1) Digital offset register

30h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1

When DTE=”1”, the digital offset function is enabled.

When digital offset is enabled, the digital offset register digitally offsets the timekeeper according to the values set for the digital offset register by changing one second of the clock count every 10 seconds.

The FOUT of 32.768kHz output does not change because the oscillation frequency of a built-in crystal does not change.

When disabled digital offset, set to DTE = ”0”. A value of setting of L7 L1 is arbitrary.

The relationship of the L7~L1 bit and the digital offset value

When the L7 bit = “0”, it is a positive offset, when the L7 bit = “1”, it is a negative offset.

Digital offset bits							Offset value
L7	L6	L5	L4	L3	L2	L1	(x 10-6)
0	1	1	1	1	1	1	192.26
0	1	1	1	1	1	0	189.21
		.					.
		.					.
		.					.
0	0	0	0	0	1	0	6.1
0	0	0	0	0	0	1	3.05
0	0	0	0	0	0	0	±0.00
1	1	1	1	1	1	1	-3.05
1	1	1	1	1	1	0	-6.1
		.					.
		.					.
		.					.
1	0	0	0	0	0	1	-192.26
1	0	0	0	0	0	0	-195.31

How to calculate the offset value

1) When the offset value is positive:

L [7 ~1] = [Offset Value]/ 3.05 However, decimals are discarded.

Example calculation: When the offset value is +192x10^{-6}

L [7 ~1] = 192.26 / 3.05 = 63 (dec)
= 0111111(bin) is set.

2) When the offset value is negative:

L [7 ~1] = 128 – [Offset Value] / 3.05 However, decimals are discarded.

Example calculation: When the offset value is -158 x10^{-6}

L [7 ~1] = 128 - (158 / 3.05) = 76(dec)
= 1001100(bin) is set.

3) When calculate from accuracy of a clock When adjust 30 seconds in 30 days:

Example calculation: 30s. / 2592000s (30days) = 11.57 x10^{-6}

Positive offset

L[7 ~1] = 11.57 / 3.05 = 4 (dec) However, decimals are discarded.

= 0000100(bin) is set.

Negative offset

L[7 ~1] = 128 – (11.57 / 3.05) = 124 (dec) However, decimals are discarded.

= 1111100(bin) is set.

(2) An effect to the other function, when used a digital offset function

Because this function adjusts an internal clock, this function affects a Wakeup timer interrupt function and a FOUT function.

1) FOUT function:

1Hz setting: Once in 10 a 1Hz period fluctuates.

1024Hz setting: Once in 10 seconds, a 1024Hz period fluctuates.

32.768kHz is not affected.

2) Wakeup timer interrupt function:

64Hz or 1Hz source clock setting:Once in 10 seconds, a period fluctuates.

4kHz source clock is not affected.

The I2C-Bus Interface

1) Overview of I2C-Bus

The I2C-Bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

2) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on a mount (bytes) of data that are transferred between the START condition and STOP condition. (However, the transfer time must be no longer than 0.95 seconds.)

3) Start and stop of I2C-Bus communications

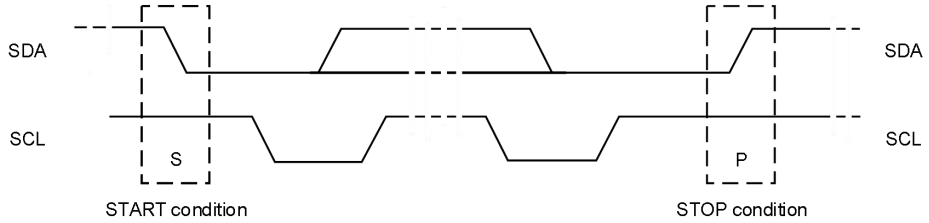


Figure 10 Start and stop mode

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition – P.

4) Slave address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	1	1	0	0	1	0	0 Write mode 1 Read mode

5) Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a

way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

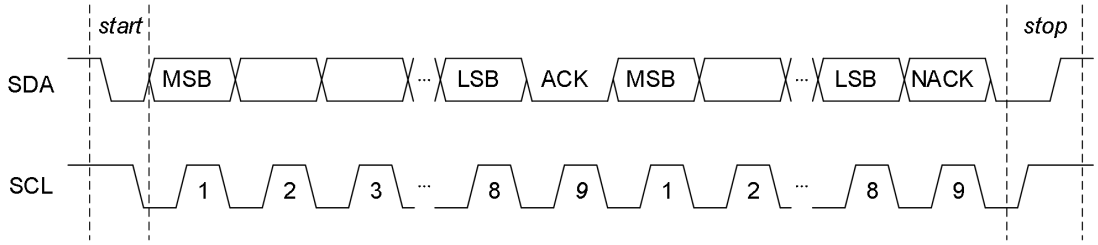


Figure11 Serial bus data transfer sequence

6) Read mode

In this mode, the master reads the RS4C8010Q slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the
master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.
The RS4C85 slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.
This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

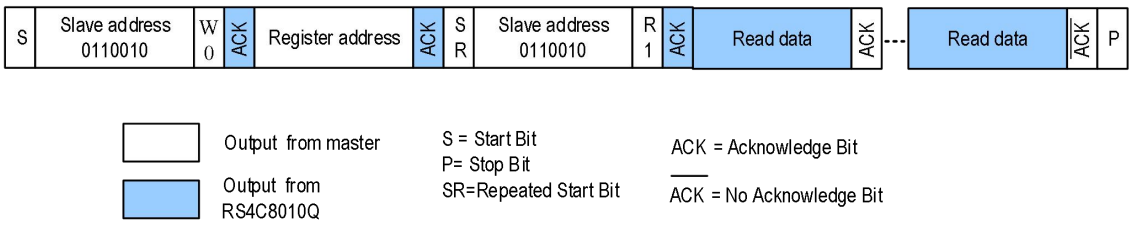


Figure 12 Read Mode Sequence

7) Write mode

In this mode the master transmitter transmits to the RS4C8010Q slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The RS4C8010Q slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

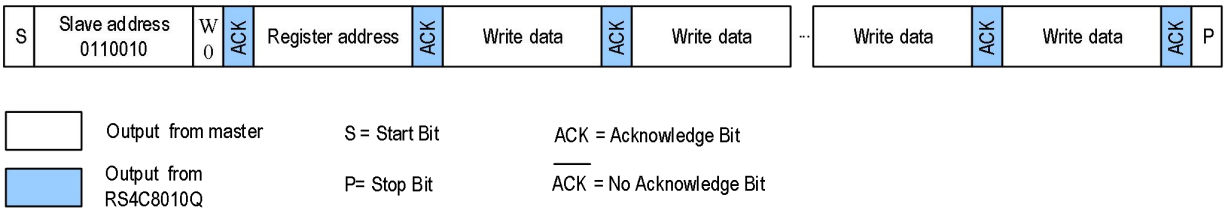
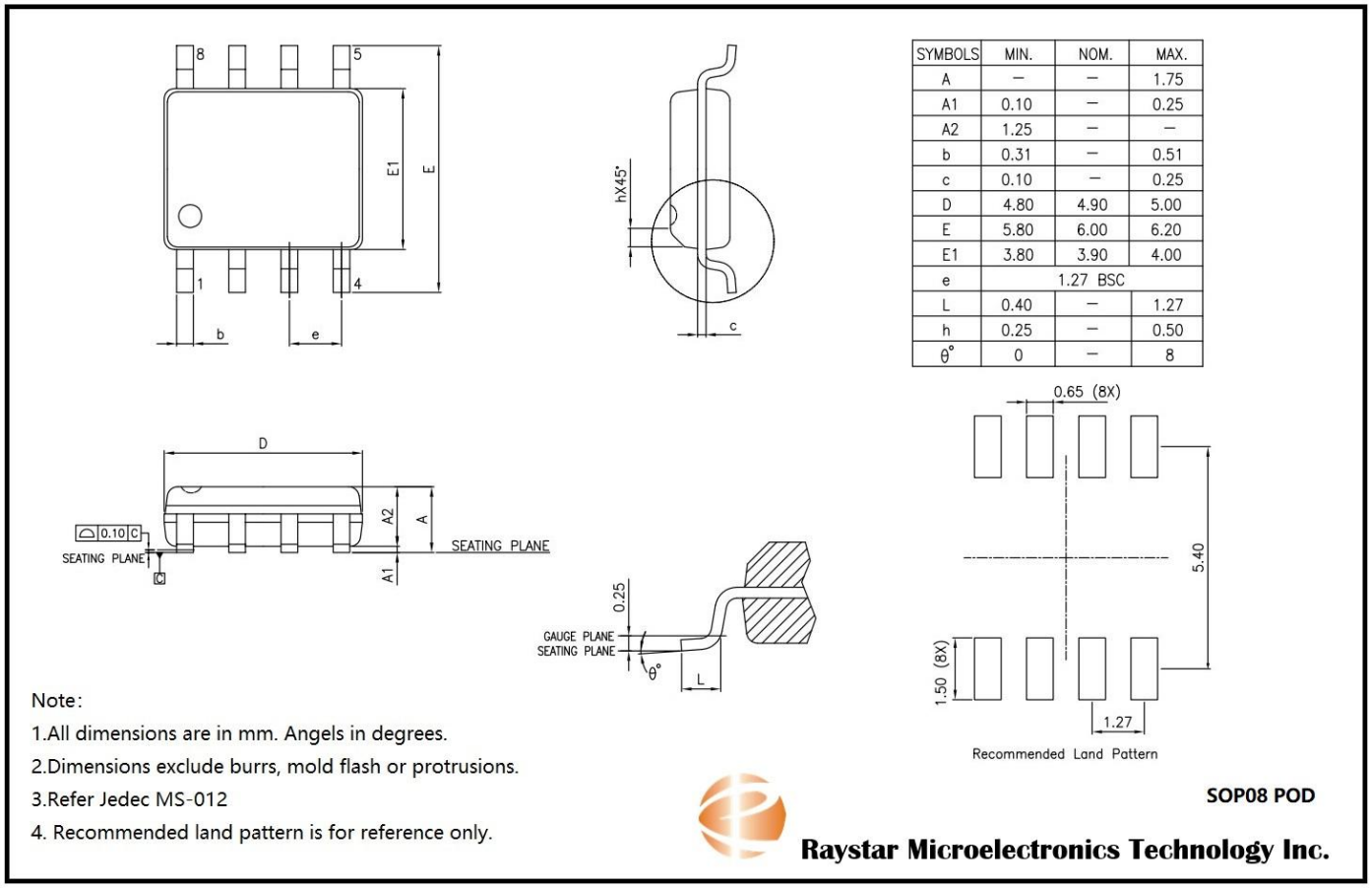


Figure 13 Write Mode Sequence

Package Information

SOP-8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	Initial Release	2026/3/19