Features

- Time keeping voltage: 1.3V to 6.0V
- Supply current: 0.5uA (Typ 3V 25° C)
- IIC bus Interface, Max 400kHz
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, and days of the week) in BCD codes
- Two systems of alarm functions
- Oscillation halt sensing to judge internal data validity
- Clock output of 32.768kHz (32.000kHz) (output controllable via a register)
- Second digit adjustment by ±30 seconds
- Automatic leap year recognition up to the year 2099
- 12-hour or 24-hour time display selectable
- High precision time trimming circuit
- Oscillator of 32.768kHz or 32.000kHz may be used
- Operating Temperature Range: -40~125 ºC
- AEC-Q 100 qualified. PPAP capable, and manufactured in IATF 16949 certified facilities.

Description

The RS4C5372Q is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption. An offset register allows fine-tuning of the clock. All addresses and data are transferred serially via the two-line bidirectional I2C-bus. Maximum data rate is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

The RS4C5372Q can generate various periodic interrupt clock pulses lasting for long period (one month), and alarm interrupt can be made by days of the week, hours, and minutes by two incorporated systems.

Ordering Information

Part Number	Package	Package Description
RS4C5372QWE	SOP8	4.9mm x 6mm
RS4C5372QLE	TSSOP8	6.4mm x 3mm

Applications

- TBOX
- Intelligent cabin

Function Block

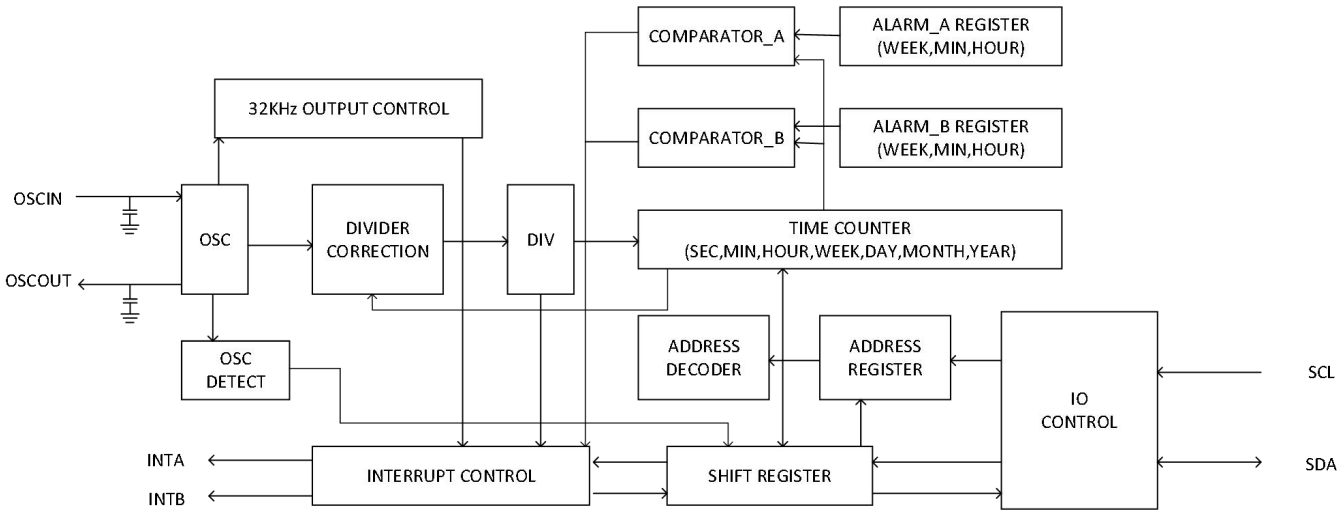


Figure1 Function Block

Pin Configuration

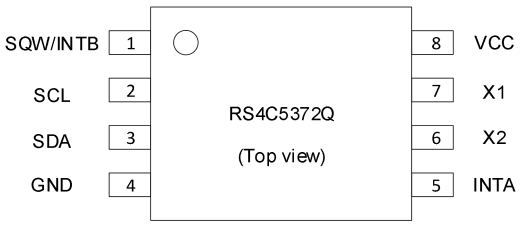


Figure2 Pin Configuration

Pin No	Pin	Type	Description
1	SQW/INTB	O	**Square-Wave/Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor.
2	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the IIC serial interface.
3	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
4	GND	P	**Ground.**
5	INTA	O	**Interrupt Output.** When enabled, INTA is asserted low when the time matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull up resistor.
6	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
7	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them. Or external clock input.
8	VCC	P	**Power.**

Typical Application Circuit

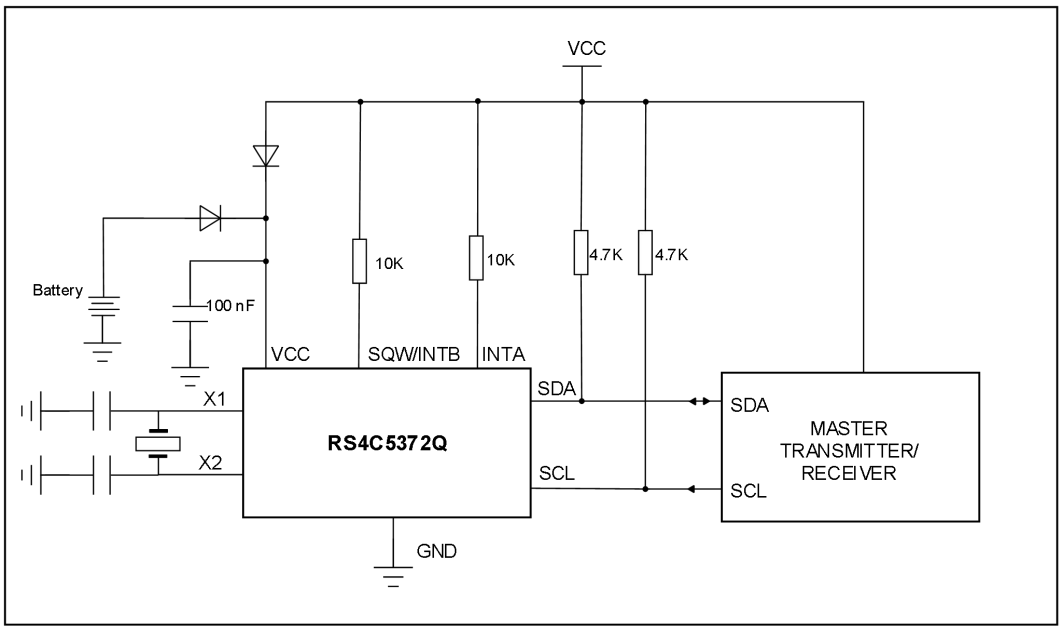
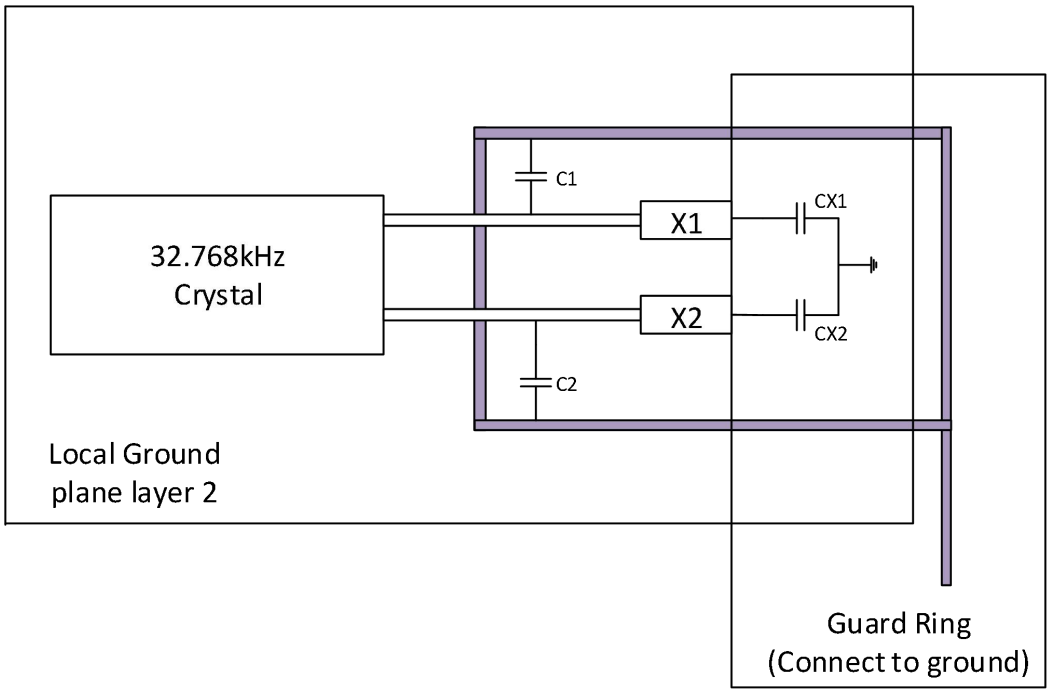


Figure3 Typical Application Circuit

Recommended Layout for Crystal



Parameter	Symbol	MIN	TYP	MAX	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_1(Optional)	0	-	15	pF
Load Capacitance	C_2(Optional)	0	-	15	pF
Build-in Cap	C_{X1}, C_{X2}	-	10	-	pF

Note:

The crystal, traces and crystal input pins should be isolated from RF generating signals.

Function Description

1. Interfacing with the CPU

The RS4C5372Q read/write data over I^2C bus interface via 2-wires: SDA (data) and SCL (clock). Since the output of the I/O pin of SDA is open drain, data interfacing with a CPU with different supply voltage is possible by applying pull-up resistor on the circuit board. The maximum clock frequency of 400kHz of SCL enables data transfer in I^2C bus fast mode.

2. Clock function

The clock function of the RS4C5372Q allows write/read data from lower two digits of the dominical year to seconds to and from the CPU. When lower two digits of the dominical year are multiples of 4, the year is recognized as a leap year automatically. Up to the year 2099 leap years will be automatically recognized.

3. Alarm function

The RS4C5372Q has an alarm function that outputs an interrupt signal from INTRA or INTRB output pins to the CPU when the day of the week, hour or minute corresponds to the setting. These two systems of alarms (Alarm_A, Alarm_B), each may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for each day of the week, thus allowing outputting alarm everyday or on a specific day of the week. The Alarm_A is output from the INTRA pin while the Alarm_B is output from either the INTRA or the INTRB pins.

4. High precision time trimming function

The RS4C5372Q have an internal oscillation circuit capacitance C_G and C_D so that an oscillation circuit may be configured simply by externally connecting a crystal. Either 32.768kHz or 32.000kHz may be selected as a crystal oscillator by setting the internal register appropriately. The RS4C5372Q incorporate a time trimming circuit that adjusts gain or loss of the clock from the CPU up to approx. ±189ppm (±194ppm when 32.000kHz crystal is used) by approximately 3ppm steps to correct discrepancy in oscillation frequency.
(Error after correction: ±1.5ppm: 25°C)

Thus by adjusting frequencies for each system,Clock display is possible at much higher precision than conventional real-time clock while using a crystal with broader fluctuation in precision.

Even seasonal frequency fluctuation may be corrected by adjusting seasonal clock error.

For those systems that have temperature detection precision of clock function may be increased by correcting clock error according to temperature fluctuations.

5. Oscillation halt sensing

The oscillation halt sensing function uses a register to store oscillation halt information. This function may be used to determine if the RS4C5372Q supply power has been booted from 0V and if it has been backed up.

This function is useful for determining if clock data is valid or invalid.

6. Periodic interrupt

The RS4C5372Q can output periodic interrupt pulses in addition to alarm function from the INTRA and INTRB pins.

This frequency may be selected from 2Hz (every 0.5 seconds), 1Hz (every second), 1/60Hz (every minute), 1/3600Hz (every hour) and monthly (1st of month).

Output wave form for periodic interrupt may be selected from regular pulse waveform (2Hz and 1Hz) and waveforms (every second, every minute, every hour and every month) that are appropriate for CPU level interrupt. Outputs may be selected either INTRA or INTRB . The RS4C5372Q has polling function that monitors pin status in the register.

7. 32-kHz clock output

The RS4C5372Q may output oscillation frequency from the INTRB pin. This clock output is set for output by default, which is set to on or off by setting the register.

Registers

Addr. (hex)*1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Seconds (00-59)	0	S40	S20	S10	S8	S4	S2	S1
1	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
2	Hours (00-23 / 01-12)	0	0	H20 or P, /A	H10	H8	H4	H2	H1
3	Days of the week (00-06)	0	0	0	0	0	W4	W2	W1
4	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
5	Months (01- 12)	0	0	0	MO10	MO8	MO4	MO2	MO1
6	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
7	Calibration Register	XSL	F6	F5	F4	F3	F2	F1	F0
8	Alarm_A: Minutes	0	AM40	AM20	AM10	AM8	AM4	AM2	AM1
9	Alarm_A: Hours	0	0	AH20 AP, /A	AH10	AH8	AH4	AH2	AH1
A	Alarm_A: Week	0	AW6	AW5	AW4	AW3	AW2	AW1	AW0
B	Alarm_B: Minutes	0	BM40	BM20	BM10	BM8	BM4	BM2	BM1
C	Alarm_B: Hours	0	0	BH20 BP, /A	BH10	BH8	BH4	BH2	BH1
D	Alarm_B: Week	0	BW6	BW5	BW4	BW3	BW2	BW1	BW0
E	Control Register 1	AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0
F	Control Register 2	0	0	12/24	ADJ XSTP	CLEN	CTFG	AAFG	BAFG

Notes:

(1) All the listed data can be read and written except forADJ/XSTP.The ADJ/XSTP bit of the control register2 is set to ADJ for write and XSTP for read operation. The XSTP bit is set to “0” by writing data into the control register2 for normal oscillation.
(2)When XSTP is set to “1”, the XSL, F6 to F0, CT2 to CT0, AALE, BALE, SL2, SL1, CLEN and TEST bits are reset to “0”.

1、Control Register 1 (at internal address Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0

1.1 AALE,BALE

Alarm_A, Alarm_B enable bits

AALE,BALE	Data	Description
Read / Write	0	Alarm_A (Alarm_B) Correspondence action invalid (Default)
	1	Alarm_A (Alarm_B) Correspondence action valid

1.2 SL2,SL1

Interrupt output select bits

SL2	SL1	Description
0	0	Outputs Alarm_A, Alarm_B, INT to the INTRA . Outputs 32k clock pulses to the INTRB . (Default)
0	1	Outputs Alarm_A, INT to the INTRA . Outputs 32k clock pulses, Alarm_B to the INTRB .
1	0	Outputs Alarm_A, Alarm_B to the INTRA . Outputs 32k clock pulses, INT to the INTRB .
1	1	Outputs Alarm_A to the INTRA . Outputs 32k clock pulses, Alarm_B, INT to the INTRB .

By setting SL1 and SL2 bits, two alarm pulses (Alarm_A and alarm_B), periodic interrupt output (INT), 32k clock pulses may be output to the INTRA or INTRB pins selectively.

1.3 TEST

Test bit

TEST	Description
0	Ordinary operation mode (Default)
1	Test mode

The test bit is used for IC test. Set the TEST bit to 0 in ordinary operation.

1.4 CT2,CT1,CT0

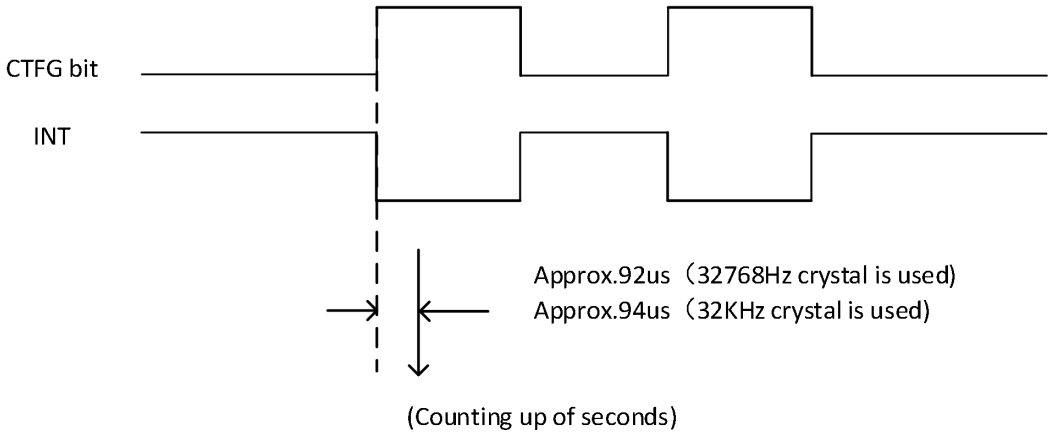
Periodic interrupt cycle select bit

CT2	CT1	CT0	Description	
			Wave Form Mode	Cycle and Falling Timing
0	0	0	—	off (“H”) (Default)
0	0	1	—	Fixed at “L”
0	1	0	Pulse Mode	2Hz (Duty50%)
0	1	1	Pulse Mode	1Hz (Duty50%)
1	0	0	Level Mode	Every second (synchronized with second count up)
1	0	1	Level Mode	Every minute (00 second of every minute)
1	1	0	Level Mode	Every hour (00 minute(s) 00 second(s) of every hour)
1	1	1	Level Mode	Every month (the 1st day 00 A.M. 00 minute(s) 00 second(s) of every month)

1) Pulse mode : Outputs 2Hz, 1Hz clock pulses. For relationships with counting up of seconds see the diagram below.
   When 32.000kHz crystal is used,
   In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulse are output alternately. Duty cycle for 1Hz clock pulses becomes 50.4% (“L” duration is 0.496s while “H” duration is 0.504s).
2) Level mode : One second, one minute or one month may be selected for an interrupt cycle. Counting up of seconds is matched with falling edge of interrupt output.
3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.
   Pulse mode : “L” duration of output pulses may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)
   For example, Duty will be 50±0.3784% (or 50±0.3875% when 32.000kHz crystal is used) at 1Hz.
   Level mode : Frequency in one second may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)

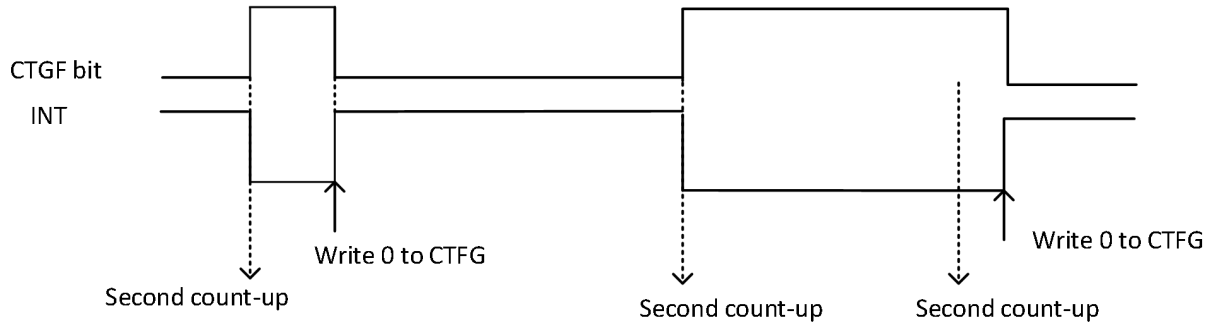
Relation Between Mode Waveforms and CTFG Bit

- **Pulse mode**



Since counting up of seconds and the falling edge has a time lag of approx. 92us (at 32.768kHz) (approx. 94us when 32.000kHz crystal is used), time with apparently approx. one second of delay from time of the real-time clock may be read when time is read in synchronization with the falling edge of output.

- **Level mode**



2、 Control Register 2 (at internal address Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	12/24	XSTP	CLEN	CTFG	AAFG	BAFG

2.1 12/24

12/24-hour Time Display System Selection bit

12 /24	Description
0	12-hour time display system (separate for mornings and afternoons)
1	24-hour time display system

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

Either the 12-hour or 24-hour time display system should be selected before writing time data.

2.2 ADJ

±30 Second Adjust Bit

ADJ	Description
0	Ordinary operation
1	Second digit adjustment

The following operations are performed by setting the second ADJ bit to 1.

1) For second digits ranging from “00” to “29” seconds:
   Time counters smaller than seconds are reset and second digits are set to “00”.
2) For second digits ranging from “30” to “59” seconds:
   Time counters smaller than seconds are reset and second digits are set to
   “00”. Minute digits are incremented by 1.

Second digits are adjusted within 122μs (within 125μs: when 32.000kHz crystal is used) from writing operation to ADJ.

The ADJ bit is for write only and allows no read operation.

2.3 XSTP

Oscillator Halt Sensing Bit

XSTP	Description
0	Ordinary oscillation
1	Oscillator halt sensing (Default)

The XSTP bit senses the oscillator halt.

When oscillation is halted after initial power on from 0V or drop in supply voltage the bit is set to “1” and which remains to be “1” after it is restarted. This bit may be used to judge validity of clock and calendar count data after power on or supply voltage drop.

When this bit is set to “1”,XSL,F6 to F0, CT2, CT1, CT0, AALE, BALE, SL2, SL1,CLEN and TEST bits are reset to “0”.INTRA will stop output and the INTRB will output 32kHz clock pulses.

The XSTP bit is set to “0” by setting the control register 2 (address Fh) during ordinary oscillation.

2.4 CLEN

32-kHz Clock Output Bit

CLEN	Description
0	32-kHz clock output enabled (Default)
1	32-kHz clock output disabled

By setting this bit to “0”, output of clock pulses of the same frequency as the crystal oscillator is enabled.

2.5 CTFG

Periodic Interrupt Flag Bit

CTFG	Description
0	Periodic interrupt output=OFF (“H”) (Default)
1	Periodic interrupt output=ON (“L”)

This bit is set to “1” when periodic interrupt pulses are output (INTRA or INTRB =“L”)

The CTFG bit may be set only to “0” in the interrupt level mode. Setting this bit to “0” sets either the INTRA or the INTRB to OFF (“H”). When this bit is set to “1” nothing happens.

2.6 AAFG,BAFG

Alarm_A (Alarm_B) Flag Bit

AAFG, BAFG	Description
0	Unmatched alarm register with clock counter (Default)
1	Matched alarm register with clock counter

The alarm interruption is enabled only when the AALE, BALE bits are set to “1”. This bit turns to “1” when matched time is sensed for each alarm.

The AAFG, BAFG bit may be set only to “0”. Setting this bit to “0” sets either the INTRA or the INTRB to the OFF “H”. When this bit is set to “1” nothing happens.

When the AALE, BALE bit is set to “0”, alarm operation is disabled and “0” is read from the AAFG, BAFG bit.

3、Clock Counter

3.1 Clock and calendar Counter (at internal address 0-6h)

Time digit display (in BCD code).

Second digits : Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
Minute digits : Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
Hour digits : See descriptions on the 12/24 bit (Section 2.2-1).
Day-of-the-week digits:

1) Incremented in septimal notation is (W4, W2,W1)=(0,0,0) –>(0,0,1).--> … →(1,1,0) →(0,0,0)
2)The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday 0,0,0).
3) The (W4, W2, W1) should not be set to (1, 1, 1).

Day digits:

1) Range from 1 to 31 (for January, March, May, July, August, October, and December).
2) Range from 1 to 30 (for April, June, September, and November). Range from 1 to 29 (for February in leap years).
3) Range from 1 to 28 (for February in ordinary years). Carried to month digits when cycled to 1.

Month digits : Range from 1 to 12 and carried to year digits when cycled to 1.
Year digits: Range from 00 to 99 and 00, 04, 08,..., 92, and 96 are counted as leap years.

Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

4、Time Trimming Register (at internal address 7h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
XSL	F6	F5	F4	F3	F2	F1	F0

4.1 XSL

The XSL bit is used to select a crystal oscillator.

XSL	Description
0	Set the XSL to 0 to use 32.768kHz (Default)
1	Set the XSL to 1 to use 32kHz

4.2 F6 to F0

The time trimming circuit adjust one second count based on this register readings when second digit is 00, 20, or 40 seconds. Normally, counting up to seconds is made once per 32,768 of clock pulse (or 32,000 when 32.000kHz crystal is used) generated by the oscillator. Setting data to this register activates the time trimming circuit.

Register counts will be incremented as ((F5,F4,F3,F2,F1,F0)–1)×2 when F6 is set to "0".
Register counts will be decremented as (($\overline{F5}$,$\overline{F4}$,$\overline{F3}$,$\overline{F2}$,$\overline{F1}$,F0)+1)×2 when F6 is set to "1".
Counts will not change when (F6,F5,F4,F3,F2,F1,F0) are set to (∗, 0, 0, 0, 0, 0,∗).

For example, when 32.768kHz crystal is used.
When (F6,F5,F4,F3,F2,F1,F0) are set to (0, 0, 0, 0, 1, 1, 1), counts will change as: 32,768+(7–1)×2=32,780 (clock will be delayed) when second digit is 00, 20, or 40.
When (F6,F5,F4,F3,F2,F1,F0) are set to (0, 0, 0, 0, 0, 0, 1), counts will remain 32,768 without changing when second digit is 00, 20, or 40.
When (F6,F5,F4,F3,F2,F1,F0) are set to (1, 1, 1, 1, 1, 1, 0), counts will change as: 32,768+(–2)×2=32,764 (clock will be advanced) when second digit is 00, 20, or 40.

Adding 2 clock pulses every 20 seconds: 2/(32,768×20)=3.051ppm (or 3.125ppm when 32.000kHz crystal is used), delays the clock by approx. 3ppm. Likewise, decrementing 2 clock pulses advances the clock by 3ppm. Thus the clock may be adjusted to the precision of ±1.5ppm. Note that the time trimming function only adjust clock timing and oscillation frequency and 32-kHz clock output is not adjusted.

5、Alarm Register (internal address Alarm A: 8h – Ah ;Alarm B: Bh to Dh)

1) Alarm_A, Alarm_B hour register D5 is set to 0 for AM and 1 for PM in the 12-hour display system at AP/A. The register D5 indicates 10 digit of hour digit in 24-hour display system at AH20.
2) To activate alarm operation, any imaginary alarm time setting should not be left to avoid unmatching.
3) In hour digit display midnight is set to 12, noon is set to 32 in 12-hour display system. (See section 2.2-1)
4) AW0 to AW6 correspond to the day-of-the-week counter (W4, W2, W1) being set at (0, 0, 0) to (1, 1, 0).
5) No alarm pulses are output when all of AW0 to AW6 are set to "0".

Example of Alarm Time Settings

Alarm Time Settings	Day-of-the-week							12-hour system				24-hour system			
	Sun. AW0	Mon. AW1	Tue. AW2	Wed. AW3	Thu. AW4	Fri. AW5	Sat. AW6	10-hour	1-hour	10-min	1-min	10-hour	1-hour	10-min	1-min
00:00 AM every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
01:30 AM every day	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59 AM every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00 PM on Monday through Friday	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
01:30 PM on Sunday	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59 PM on Monday, Wednesday, and Friday	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratinge	Unit
VDD	Supply Voltage		−0.3 to +7.0	V
VI	Input Voltag	SCL, SDA	−0.3 to +7.0	V
VO1	Output Voltage 1	SDA	−0.3 to +7.0	V
VO2	Output Voltage 2	INTRA,INTRB	−0.3 to +12	
PD	Power Dissipation	Topt=25°C	300	mW
Topt	Operating Temperature		−40 to +125	°C
Tstg	Storage Temperature		−55 to +125	°C

Note: Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limit.

RECOMMENDED OPERATING CONDITIONS

(Vss=0V,Topt=−40 to +125°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
VDD	Supply Voltage		1.7		6.0	V
VCLK	Timekeeping Voltage		1.3		6.0	V
FXT	Oscillation Frequency			32.768 or 32.000		kHz
V_{PUP1}	Pull-up Voltage 1	SCL, SDA			6.0	V
V_{PUP2}	Pull-up Voltage 2	INTRA,INTRB			10.0	V

DC Characteristics

Unless otherwise specified: Vss=0V, V_{DD}=3V, Topt=−40 to +125°C, Oscillation frequency=32.768kHz, or 32.000kHz(R1=30kΩ)

Symbol	Item	Pin name	Conditions	Min.	Typ.	Max.	Unit
VIH	"H" Input Voltage	SCL, SDA		0.8VDD		6.0	V
VIL	"L" Input Voltage	SCL, SDA		−0.3		0.2VDD	V
IOL1	Output Current	INTRA , INTRB	VOL1=0.4V	1			mA
IILK	Input Leakage Current	SCL	VI=6V or Vss VDD=6V	−1		1	μA
IOZ	Output Off State Leakage Current	SDA, INTRA , INTRB	VO=6V or Vss VDD=6V	−1		1	μA
IDD1	Standby Current	VDD	VDD=3V Topt=25°C SCL, SDA=3V Output=OPEN*1		0.5	0.9	μA
IDD2		VDD	VDD=3V Topt=−40 to +125°C SCL, SDA=3V Output=OPEN*1			1.0	μA
IDD3		VDD	VDD=6V SCL, SDA=6V Output=OPEN*1		0.8	2.0	μA
CG	Internal Oscillation Capacitance 1	OSCIN			10		pF
CD	Internal Oscillation Capacitance 2	OSCOUT			10		pF

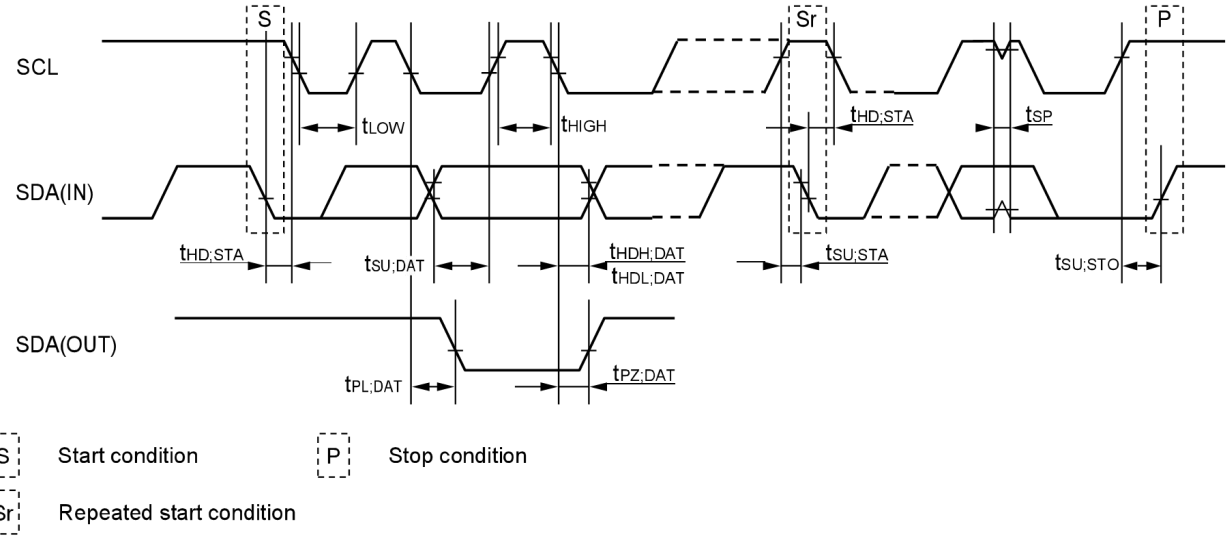
Note1: The mode outputs no clock pulses when output is open (output off state)

I2C AC Characteristics

V_{DD}≥1.7V (supports standard mode IIC bus)

Unless otherwise specified : Vss=0V, Topt=−40 to +125, Crystal=32.768kHz or 32.000kHz, Input and Output Conditions:VIH=0.8×VDD,VIL=0.2×VDD,VOL=0.2×VDD,CL=50pF

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency		0		100	kHz
t_{LOW}	SCL Clock “L” Time		4.7			μs
t_{HIGH}	SCL Clock “H” Time		4.0			μs
$t_{HD;STA}$	Start Condition Hold Time		4.0			μs
$t_{SU;STO}$	Stop Condition Setup Time		4.0			μs
$t_{SU;STA}$	Start Condition Setup Time		4.7			μs
$t_{SU;DAT}$	Data Setup Time		250			ns
$t_{HDH;DAT}$	“H”Data Hold Time		0			ns
$t_{HDL;DAT}$	“L”Data Hold Time	VDD≥2.0V	35			ns
$t_{HDL;DAT}$	“L”Data Hold Time	VDD≥1.7V	150			ns
$t_{PL;DAT}$	SDA “L”Stable Time After Falling of SCL				2.0	μs
$t_{PZ;DAT}$	SDA off Stable Time After Falling of SCL				2.0	μs
t_R	Rising Time of SCL and SDA (Input)				1000	ns
t_F	Falling Time of SCL and SDA (Input)				300	ns
t_{SP}	Spike Width that can be Removed with Input Filter				50	ns



S Start condition

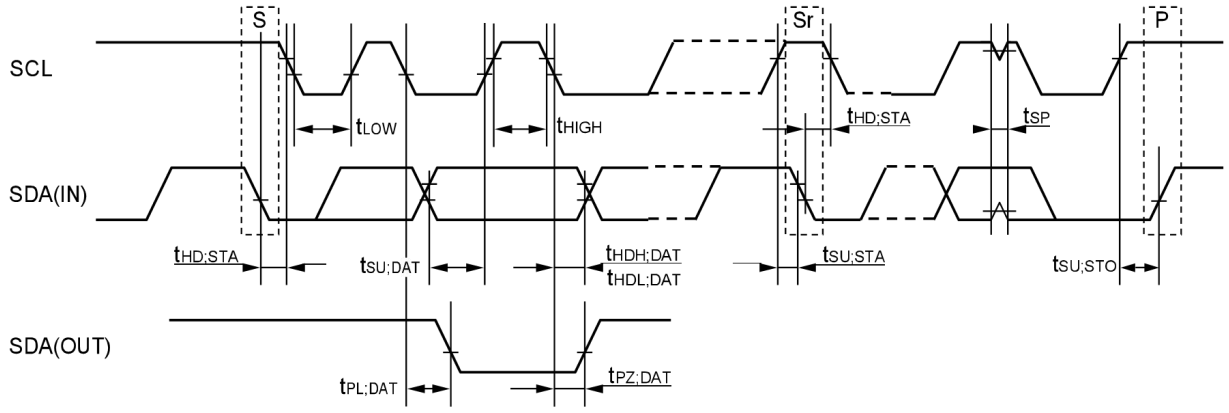
P Stop condition

Sr Repeated start condition

V_{DD}≥2.5V (supports fast mode IIC bus)

Unless otherwise specified : Vss=0V, Topt=−40 to +125° C, Crystal=32.768kHz or 32.000kHz, Input and Output Conditions:VIH=0.8×VDD,VIL=0.2×VDD,VOL=0.2×VDD,CL=50pF

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency		0		400	kHz
t_{LOW}	SCL Clock "L" Time		1.3			μs
t_{HIGH}	SCL Clock "H" Time		0.6			μs
$t_{HD\ ;\ STA}$	Start Condition Hold Time		0.6			μs
$t_{SU\ ;\ STO}$	Stop Condition Setup Time		0.6			μs
$t_{SU\ ;\ STA}$	Start Condition Setup Time		0.6			μs
$t_{SU\ ;\ DAT}$	Data Setup Time		100			ns
$t_{HDH\ ;\ DAT}$	"H"Data Hold Time		0			ns
$t_{HDL\ ;\ DAT}$	"L"Data Hold Time		35			ns
$t_{PL\ ;\ DAT}$	SDA "L" Stable Time After Falling of SCL				0.9	μs
$t_{PZ\ ;\ DAT}$	SDA off Stable Time After Falling of SCL				0.9	μs
t_R	Rising Time of SCL and SDA (Input)				300	ns
t_F	Falling Time of SCL and SDA (Input)				300	ns
t_{SP}	Spike Width that can be Removed with Input Filter				50	ns



S Start condition

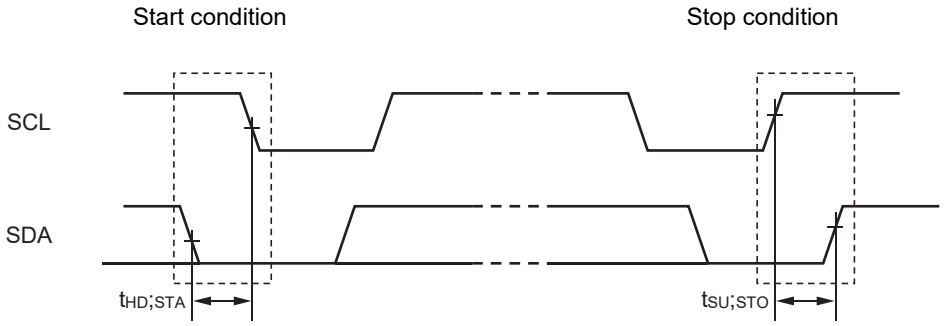
P Stop condition

Sr Repeated start condition

Transmission System of I2C bus

1、Start and stop conditions

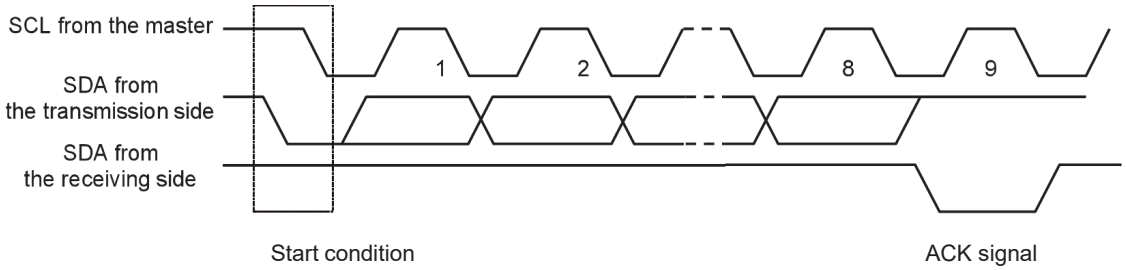
The SCL and SDA pins are at the “H” level when no data transmission is made. Changing the SDA from “H” to “L” when the SCL and the SDA are “H” activates the start condition and access is started. Changing the SDA from “L” to “H” when the SCL is “H” activates stop condition and accessing stopped. Generation of start and stop conditions are always made by the master (see the figure below).



2、Data transmission and its acknowledge

After start condition is entered, data is transmitted by 1byte (8bits). Any bytes of data may be serially transmitted.

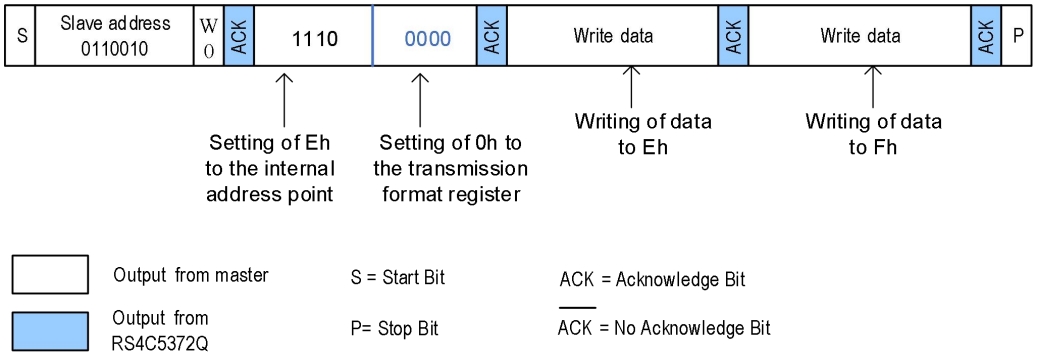
The receiving side will send an acknowledge signal to the transmission side each time 8bit data is transmitted. The acknowledge signal is sent immediately after falling to “L” of SCL8bit clock pulses of data transmission, by releasing the SDA by the transmission side that has asserted the bus at that time and by turning the SDA to “L” by the receiving side. When transmission of 1byte data next to preceding 1byte of data is received, the receiving side releases the SDA pin at falling edge of the SCL9bit of clock pulses or when the receiving side switches to the transmission side it starts data transmission. When the master is the receiving side, it generates no acknowledge signal after the last 1byte of data from the slave to tell the transmitter that data transmission has completed when the slave side (transmission side) continues to release the SDA pin so that the master will be able to generate stop condition.



3、 Data transmission write format in the RS4C5372Q

Although the IIC bus standard defines a transmission format for the slave address allocated for each IC, transmission method of address information in IC is not defined. The RS4C5372Q transmit data the internal address pointer (4bit) and the transmission format register (4bit) at the 1byte next to one which transmitted a slave address and a write command. For write operation only one transmission format is available and (0000) is set to the transmission format register. The 3byte transmits data to the address specified by the internal address pointer written to the 2byte. Internal address pointer settings are automatically incremented for 4byte and after. Note that when the internal address pointer is Fh, it will change to 0h on transmitting the next byte.

Example of data writing (When writing to internal address Eh to Fh)

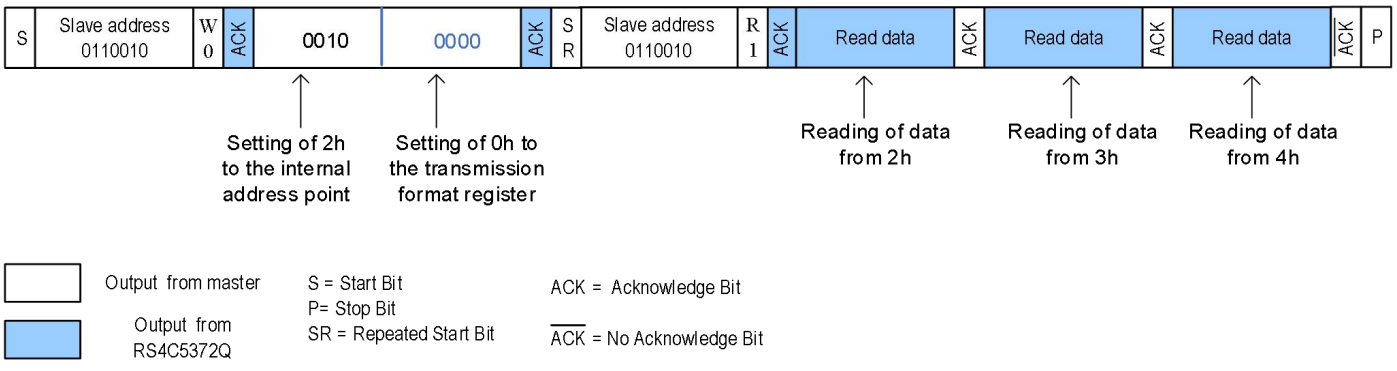


4、 Data transmission read format of the RS4C5372Q

The RS4C5372Q allow the following three readout methods of data from an internal register.

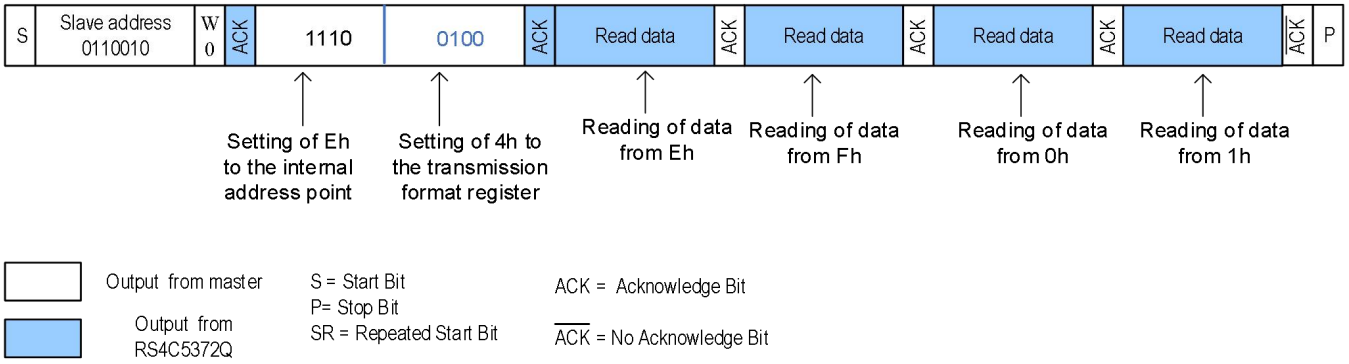
1) The first method to reading data from the internal register is to specify an internal address by setting the internal address pointer and the transmission format register, generate the repeated start condition to change the data transmission direction to perform reading. The internal address pointer is set to Fh when the stop condition is met. Therefore, this method of reading allows no insertion of the stop condition before the repeated start condition. Set 0h to the transmission format register.

Example 1 of data read (when data is read from 2h to 4h)



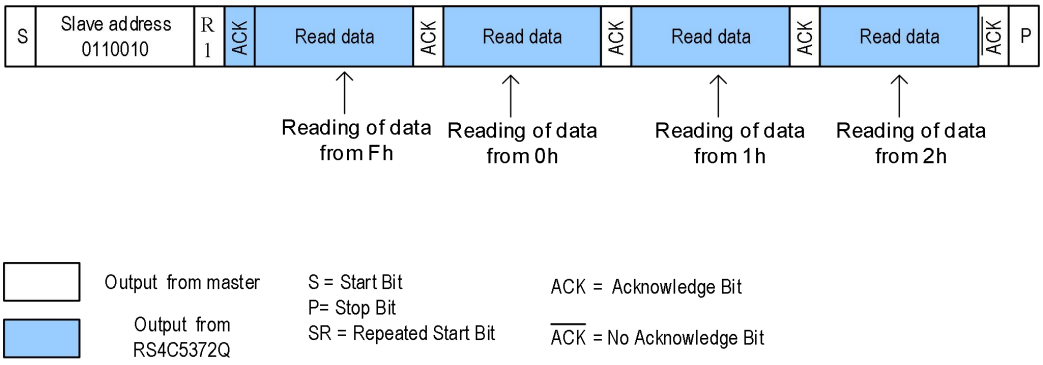
2) The second method to reading data from the internal register is to start reading immediately after writing to the internal address pointer and the transmission format register. Although this method is not based on the IIC bus standard in a strict sense it still effective to shorten read time to ease load to the master. Set 4h to the transmission format register when this method is used.

Example 2 of data read (when data is read from internal addresses Eh to 1h).



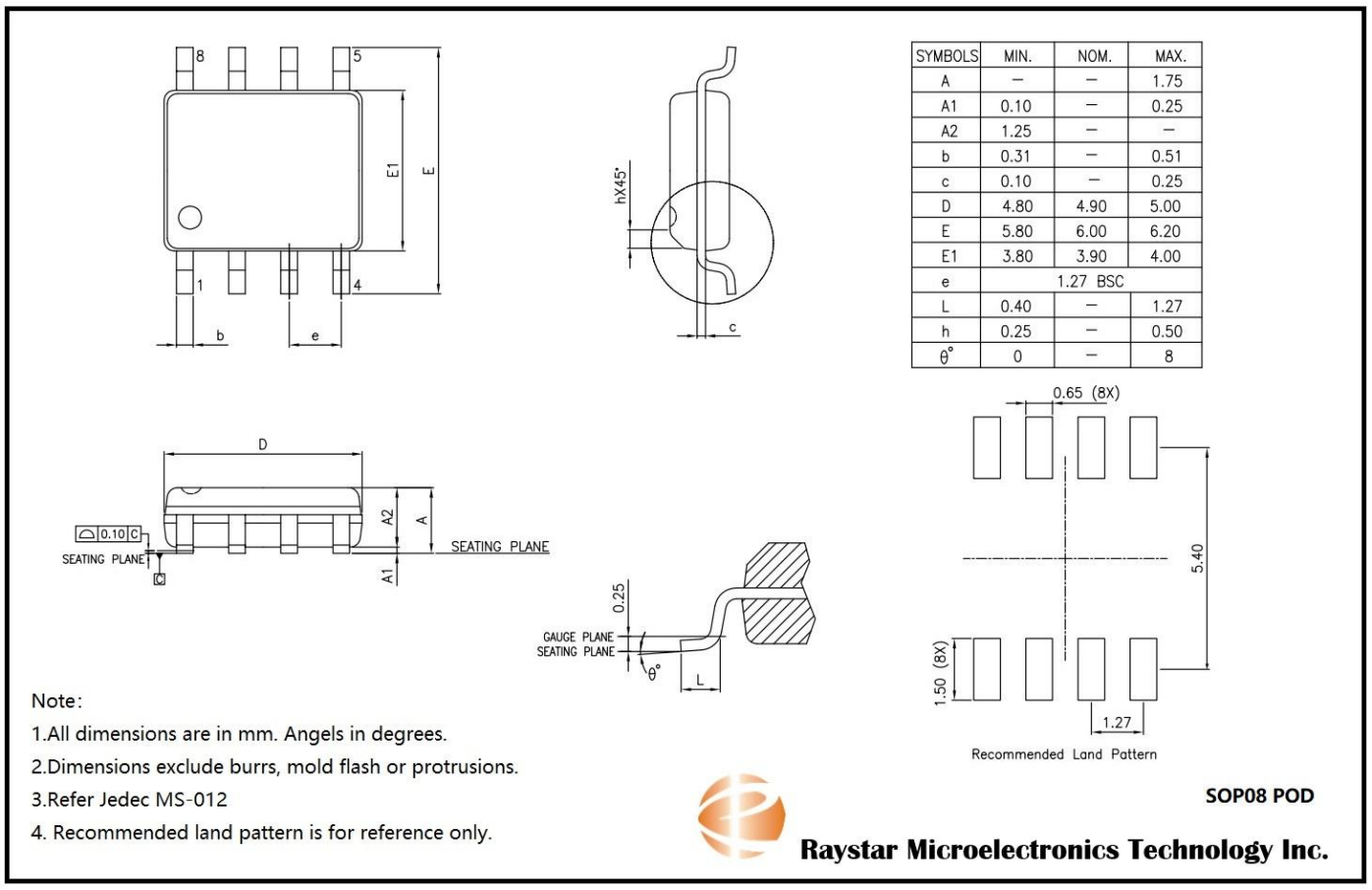
3) The third method to reading data from the internal register is to start reading immediately after writing to the slave address and the R/ W bit. Since the internal address pointer is set to Fh by default as described in 1), this method is only effective when reading is started from the internal address Fh.

Example 3 of data read (when data is read from internal addresses Fh to 2h).



Package Information

SOP8



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	—	1.27
h	0.25	—	0.50
θ°	0	—	8

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD

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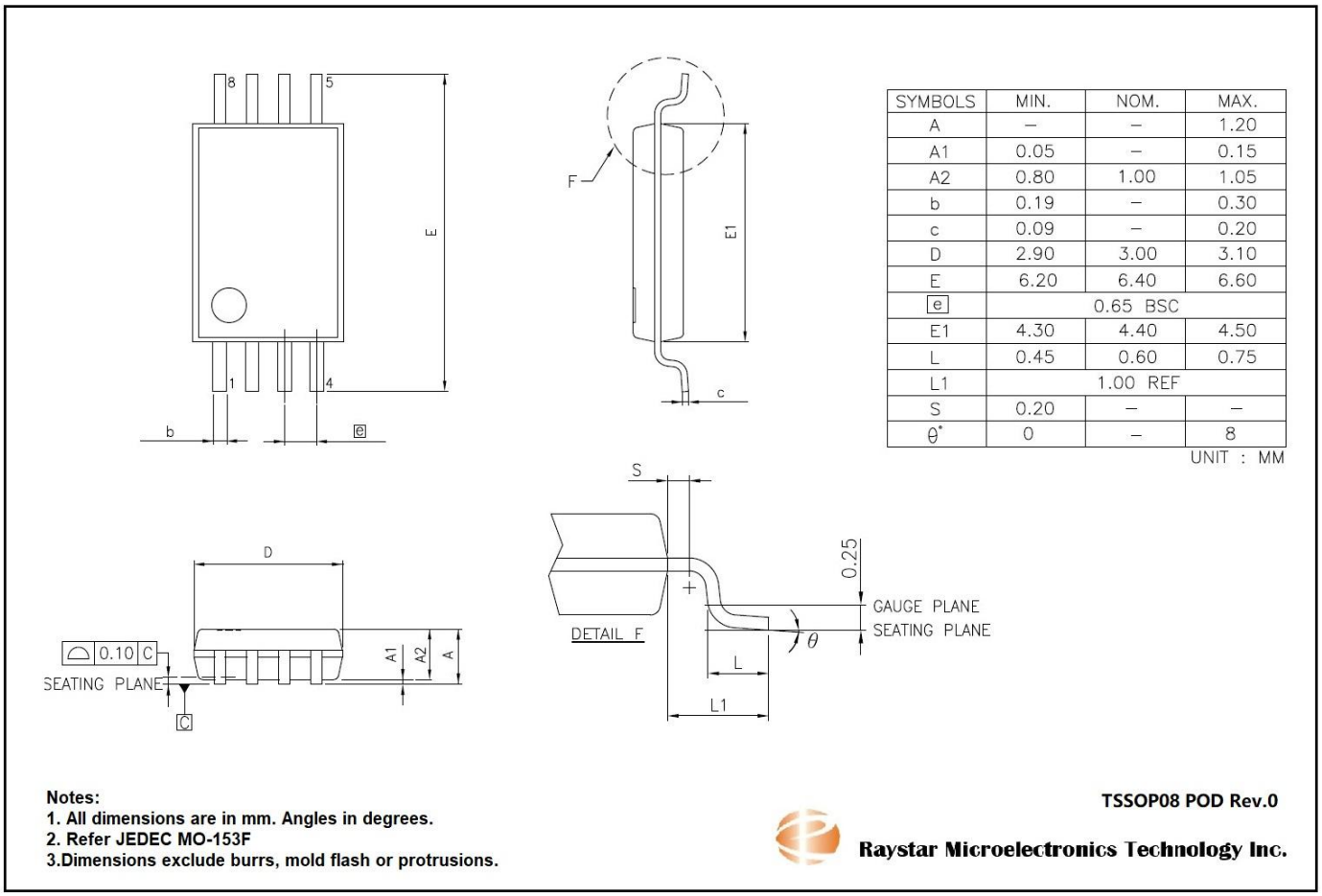
TSSOP8



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E	6.20	6.40	6.60
e	0.65 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	–	–
θ°	0	–	8

UNIT : MM

Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-153F
3.Dimensions exclude burrs, mold flash or protrusions.

TSSOP08 POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
1.0	Initial Release	2025/12/30