Features

- Four LVCMOS / LVTTL outputs
- LVCMOS / LVTTL clock input
- CLK can accept the input levels: LVCMOS, LVTTL
- Maximum output frequency: 200MHz
- Additive phase jitter, RMS: 60fs (typical) @ 3.3V
- Output skew: 45ps (maximum) @ 3.3V
- Part-to-part skew: 500ps (maximum)
- 3.3V input, outputs may be 3.3V, 2.5V or 1.8V Supply

Applications

- PCIX controllers
- Ethernet, Switch
- IPC, NVR
- General Clock Distribution

Block Diagram

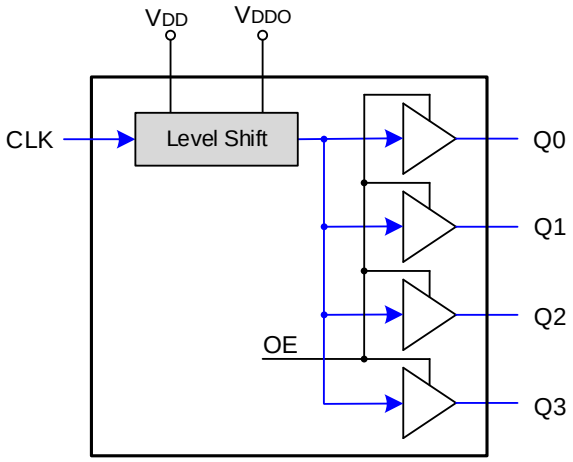


Figure 1 Block Diagram

Description

Raystar's RS8304 are low-skew, low- noise, high speed clock buffers and are ideal for computing, networking, and communication applications. The RS8304 is a low skew, 1-to-4 Fanout Buffer from RSM. The RS8304 is characterized at full 3.3V for input (V_{DD}), and mixed 3.3V, 2.5V and 1.8V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the RS8304 ideal for those clock distribution applications demanding well defined performance and repeatability.

Order Information

Part Number	Package	Description
RS8304WE	8-Pin SOIC	4.9mmx6mm
RS8304UE	8-Pin MSOP	3.2mmx5.15mm
RS8304TE	8-Pin TSSOP	3mmx6.4mm
RS8304ZAE	8-Pin DFN8	2mmx2mm
RS8304ZFE	8-Pin DFN8	1.5mmx1.5mm

Notes
[1] E = Pb-free and Green

Pin Configuration

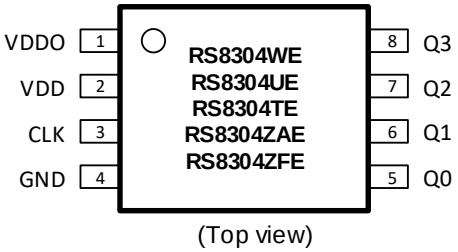


Figure 2 Pin configuration

Pin Description

Pin No.	Name	Type		Description
1	VDDO	Power		Output supply pin.
2	VDD	Power		Positive supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTL interface levels.

Absolute Maximum Ratings

Parameter	Range
Supply Voltage (V_{DD})	–0.0V to +6.5V
Input Voltage	–0.5V to VDD+0.5V
Industrial Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Input ESD MIL- 883, method 3015, HBM	2KV

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_{DD}	Core Supply	1.71	3.63	V
V_{DDO}	I/O Supply	1.8	3.3	V
T_A	Industrial Ambient Temperature	–40	+85	° C

DC Electrical Characteristics

- **Power Supply DC Characteristics**

(T_A=-40~85℃, V_{DD}=V_{DDO}=3.3V, C_L=10pF)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	
I_{DD}	Power Supply Current				1	mA
I_{DDO}	Output Supply Current	C_L = 10pF/100MHz			45	

(T_A=-40~85℃, V_{DD}=3.3V, V_{DDO}=2.5V, C_L=10pF)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		2.375	2.5	2.625	
I_{DD}	Power Supply Current				1	mA
I_{DDO}	Output Supply Current	C_L = 10pF/100MHz			35	

(T_A=-40~85℃, V_{DD}=3.3V, V_{DDO}=1.8V, C_L=10pF)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		1.71	1.8	1.89	
I_{DD}	Power Supply Current				1	mA
I_{DDO}	Output Supply Current	C_L = 10pF/100MHz			25	

● LVCMOS / LVTTL DC Characteristics

(T_A=-40~85℃, V_{DD}=V_{DDO}=3.3V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage	V_{DDO}=3.3V			0.8	V
V_{IH}	Input High Voltage	V_{DDO}=3.3V	0.6*VDD		VDD+0.3	
I_{IL}	Input Low Current	V_{IN}=0	–5			μA
I_{IH}	Input High Current	V_{DD}=V_{IN}=3.3V			100	
V_{OL}	Output Low Voltage	V_{DDO}=3.3V, I_{OL} = 8mA			0.5	V
V_{OH}	Output High Voltage	V_{DDO}=3.3V, I_{OH} = -8mA	0.7*VDD			
Zo	Nominal Output Impedance			17		Ω

(T_A=-40~85℃, V_{DD}= 3.3V, V_{DDO}=2.5V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage	V_{DDO}=2.5V			0.8	V
V_{IH}	Input High Voltage	V_{DDO}=2.5V	0.6*VDD		VDD+0.3	
I_{IL}	Input Low Current	V_{IN}=0	–5			μA
I_{IH}	Input High Current	V_{DD}=V_{IN}=2.5V			100	
V_{OL}	Output Low Voltage	V_{DDO}=3.3V, I_{OL} = 8mA			0.5	V
V_{OH}	Output High Voltage	V_{DDO}=3.3V, I_{OH} = -8mA	0.7*VDD			
Zo	Nominal Output Impedance			20		Ω

(T_A=-40~85℃, V_{DD}= 3.3V, V_{DDO}=1.8V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage	V_{DDO}=1.8V			0.8	V
V_{IH}	Input High Voltage	V_{DDO}=1.8V	0.6*VDD			
I_{IL}	Input Low Current	V_{IN}=0	–5			μA
I_{IH}	Input High Current	V_{DD}=V_{IN}=1.8V			100	
V_{OL}	Output Low Voltage	V_{DDO}=1.8V, I_{OL} = 8mA			0.5	V
V_{OH}	Output High Voltage	V_{DDO}=1.8V, I_{OH} = -8mA	0.7*VDD			
Zo	Nominal Output Impedance			25		Ω

AC Characteristics

(T_A=-40~85℃, V_{DD}=V_{DDO}=3.3V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
F_{IN}	Input frequency		0		200	MHz
T_{PLH}, T_{PHL}	Propagation delay	CLK to Qn rising edges	2.5	3	3.5	ns
T_{jitter}	Additive Phase Jitter, RMS	100MHz, Integration Range: 12kHz – 20MHz		60		fs
$T_{SK(O)}$	Output skew	@ VDD/2			100	ps
$T_{SK(P)}$	Pulse skew	@ VDD/2			300	
$T_{SK(T)}$	Package skew	@ VDD/2			500	
T_R, T_F	Rise, Fall time	20%~80%		1.3	2	ns
T_{DC}	Output Duty Cycle	$t_{DC} = t_H/t_{CYCLE}$	45		55	%

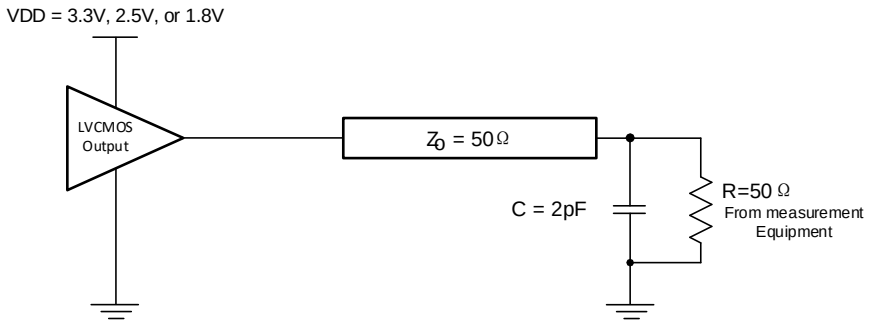
(T_A=-40~85℃, V_{DD}= 3.3V, V_{DDO}=2.5V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
F_{IN}	Input frequency		0		200	MHz
T_{PLH}, T_{PHL}	Propagation delay	CLK to Qn rising edges	3	3.5	4.1	ns
T_{jitter}	Additive Phase Jitter, RMS	100MHz, Integration Range: 12kHz – 20MHz		67		fs
$T_{SK(O)}$	Output skew	@ VDD/2			100	ps
$T_{SK(P)}$	Pulse skew	@ VDD/2			300	
$T_{SK(T)}$	Package skew	@ VDD/2			500	
T_R, T_F	Rise, Fall time	20%~80%		1.3	2	ns
T_{DC}	Output Duty Cycle	$t_{DC} = t_H/t_{CYCLE}$	45		55	%

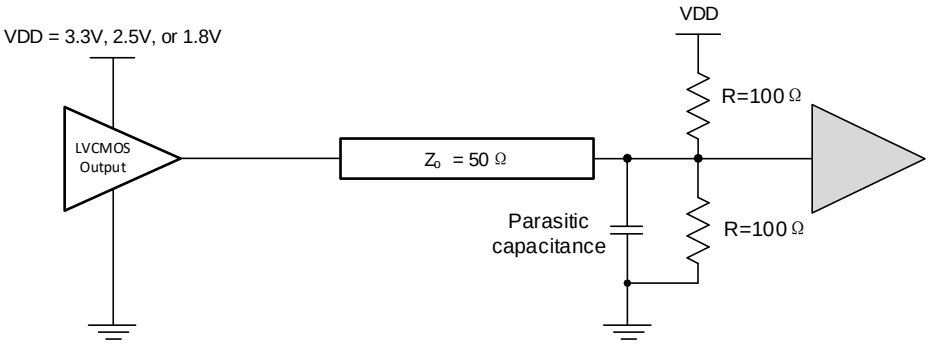
(T_A=-40~85℃, V_{DD}= 3.3V, V_{DDO}=1.8V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
F_{IN}	Input frequency		0		200	MHz
T_{PLH}, T_{PHL}	Propagation delay	CLK to Qn rising edges	2.5	4	6.5	ns
T_{jitter}	Additive Phase Jitter, RMS	100MHz, Integration Range: 12kHz – 20MHz		120		fs
$T_{SK(O)}$	Output skew	@ VDD/2			100	ps
$T_{SK(P)}$	Pulse skew	@ VDD/2			300	
$T_{SK(T)}$	Package skew	@ VDD/2			500	
T_R, T_F	Rise, Fall time	20%~80%		1.3	2	ns
T_{DC}	Output Duty Cycle	$t_{DC} = t_H/t_{CYCLE}$	45		55	%

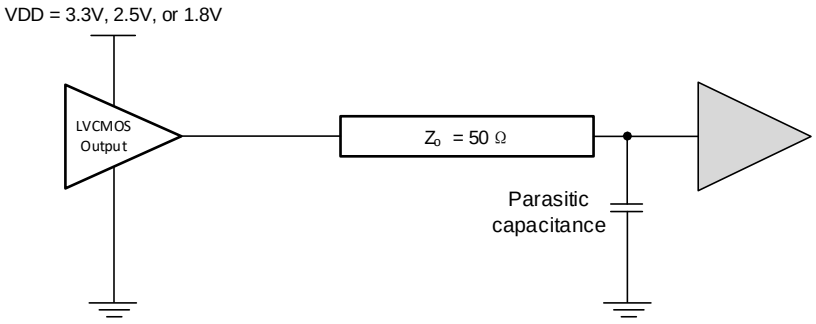
Parameter Measurement Information



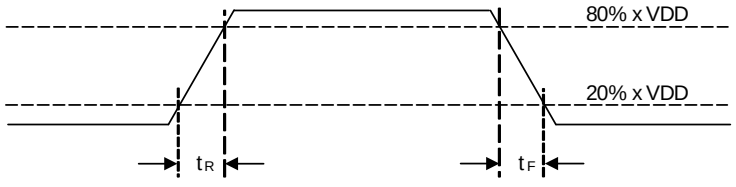
Test Load Circuit



Application Load With 50-Ω Termination



Application Load With Termination

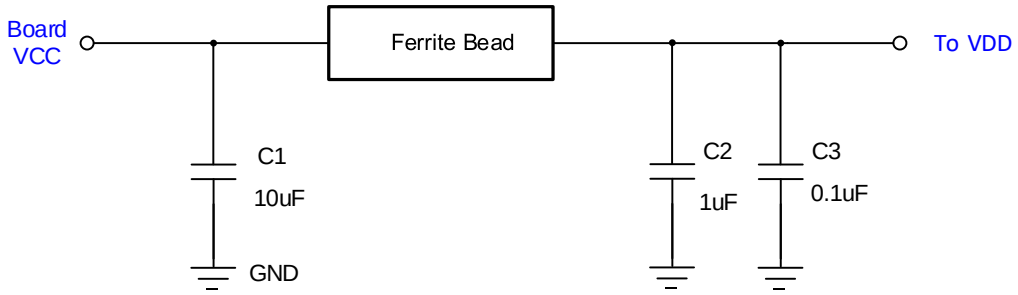


Rise and Fall Time

Power Supply Recommendations

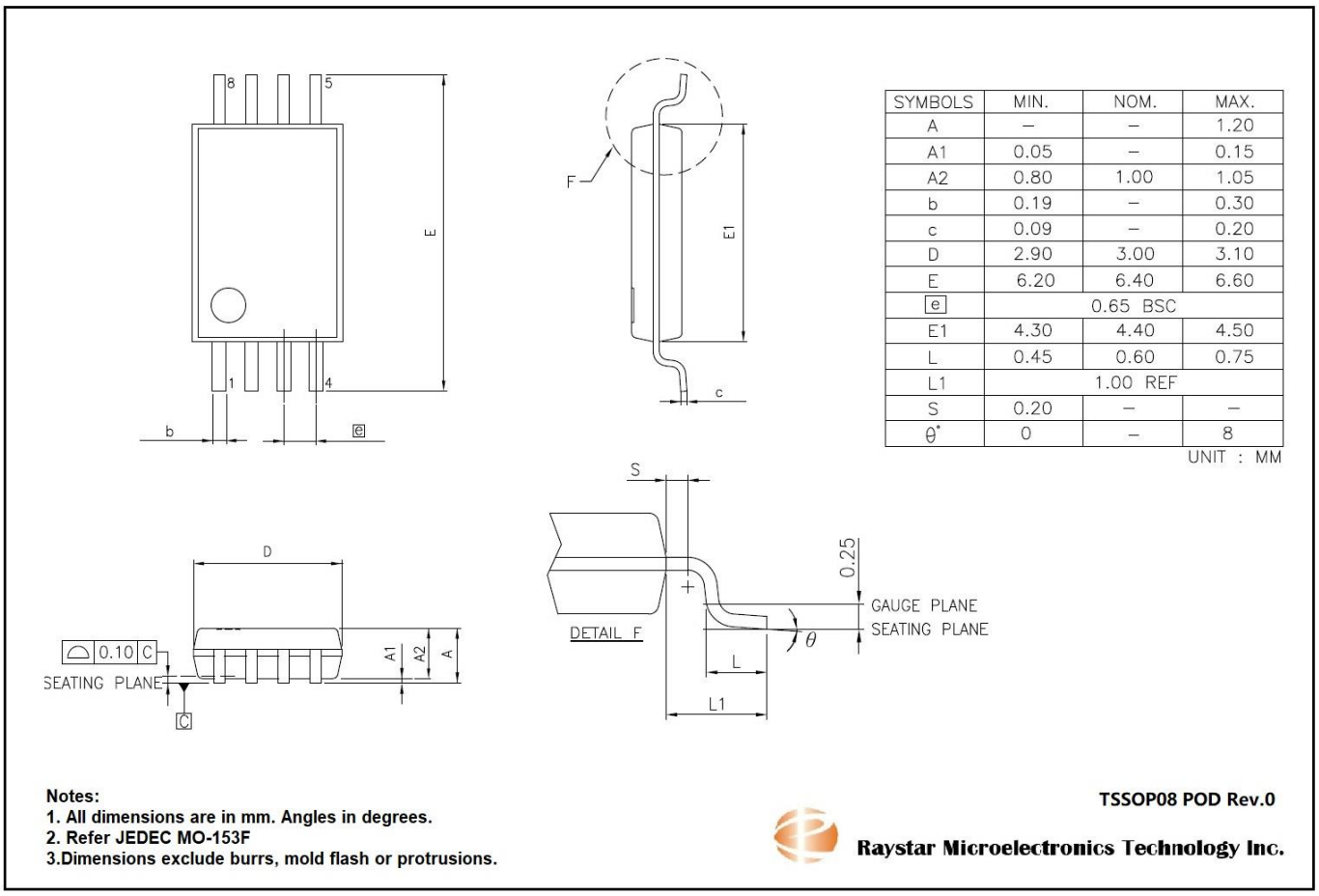
High-performance clock buffers can be sensitive to noise on the power supply, which may dramatically increase the additive jitter of the buffer. Thus, it is essential to manage any excessive noise from the system power supply, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. It's recommended adding as many high- frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. We recommend, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.



Package Information

8-Pin TSSOP (T)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E	6.20	6.40	6.60
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

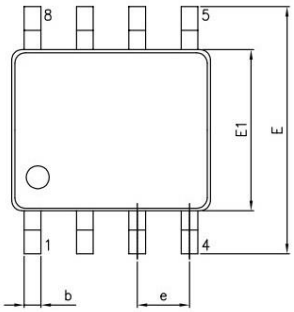
UNIT : MM

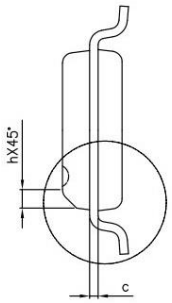
Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-153F
3.Dimensions exclude burrs, mold flash or protrusions.

TSSOP08 POD Rev.0

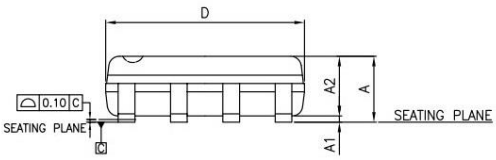
Raystar Microelectronics Technology Inc.

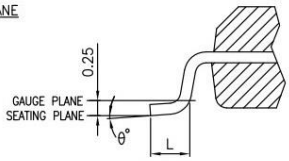
8-Pin SOIC (W)

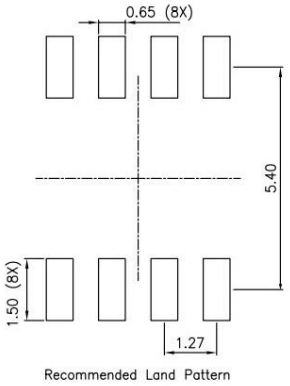




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8







Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

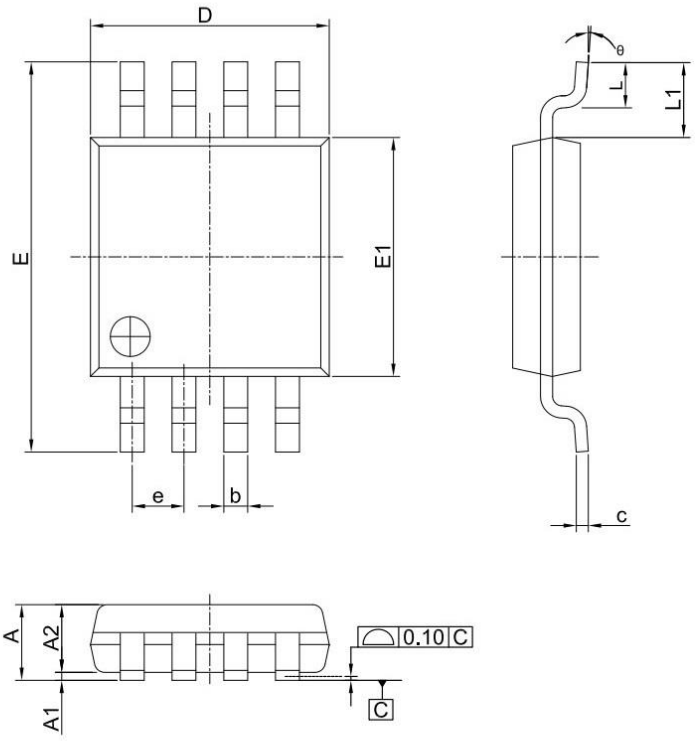
3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

Raystar Microelectronics Technology Inc.

8-Pin MSOP (U)



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Note:

1.All dimensions are in mm. Angels in degrees.

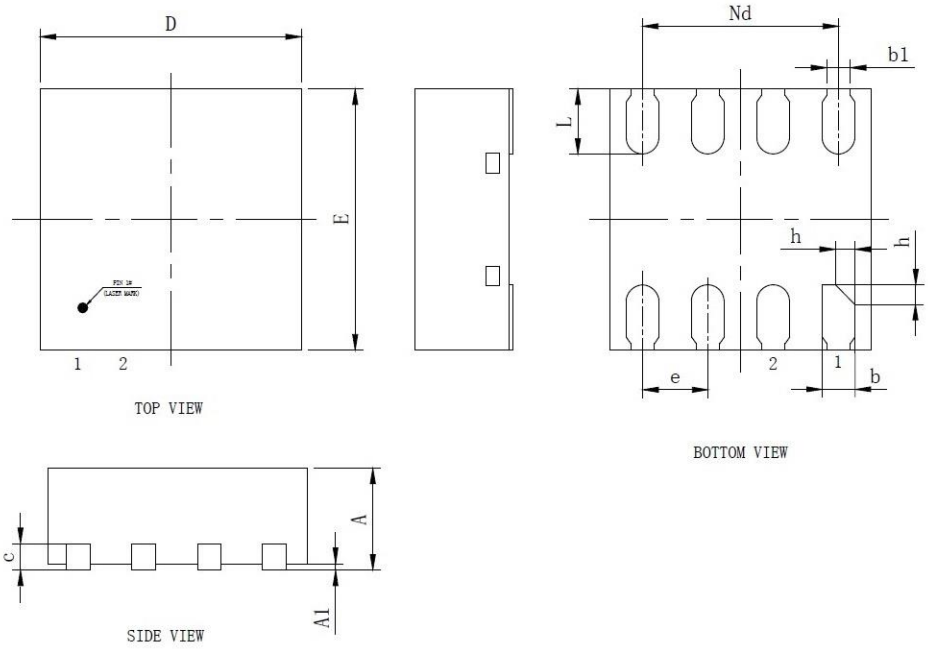
2.Refer Jedec MO-187

3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08 POD Rev.0

Raystar Microelectronics Technology Inc.

8-Pin DFN8 (ZA)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 18	0.25	0. 30
b1	0.18REF		
c	0.203REF		
D	1. 90	2. 00	2. 10
e	0. 50BSC		
Nd	1. 50BSC		
E	1. 90	2. 00	2. 10
L	0. 45	0.50	0. 55
h	0. 10	0. 15	0. 20

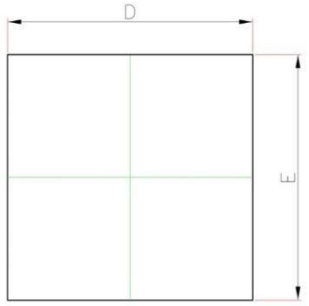
Notes:

1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-229
3.Dimensions exclude burrs, mold flash or protrusions.

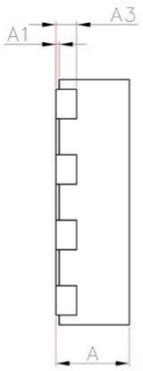
DFN 2X2X0.75-8L(ZA08) POD Rev.0

Raystar Microelectronics Technology Inc.

8-Pin DFN8 (ZF)

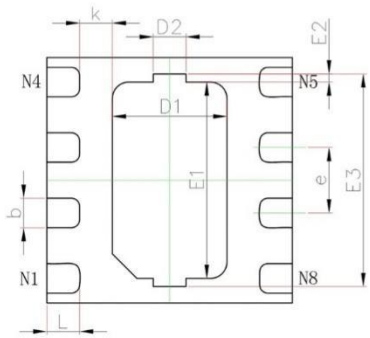


TOP VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.400	0.500	0.016	0.020
A1	0.000	0.050	0.000	0.002
A3	0.127REF.		0.005REF.	
D	1.450	1.550	0.057	0.061
E	1.450	1.550	0.057	0.061
D1	0.600	0.800	0.024	0.031
D2	0.200REF.		0.008REF.	
E1	1.100	1.300	0.043	0.051
E2	0.050REF.		0.002REF.	
E3	1.200	1.400	0.047	0.055
k	0.200REF.		0.008REF.	
b	0.150	0.250	0.006	0.010
e	0.400BSC.		0.016BSC.	
L	0.150	0.250	0.006	0.010



BOTTOM VIEW

Note:
1. All dimensions are in mm. angle in degrees.
2. Refer JEDEC MO-229.
3. demensions exclude burrs, mold flash or protrusions.

DFN 1.5X1.5X0.45 8L(ZF08) POD Rev.A

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	Initial release	2022/6/16
V1.1	Updated part name and POD	2023/01/29
V1.2	Add 1.8V and 2.5V Characteristic Parameters	2025/12/31