Features

- RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- 56-Byte Battery-Backed NV RAM for Data Storage
- I^2C Serial Interface
- Programmable Square-Wave Output Signal
- Automatic Power-Fail Detect and Switch Circuitry
- Operating Temperature: -40 ~ 85°C

Applications

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)
- Other (Utility Meter, Vending Machine, Thermostat, Modem)

Description

The RS4C1307 serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The RS4C1307 has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply.

Ordering Information:

Ordering Code	Package	Package Description
RS4C1307WE	SOP8	Pitch 1.27mm
RS4C1307UE	MSOP8	Pitch 0.65mm

Note:
1. E = Pb-free and Green

Pin Configurations

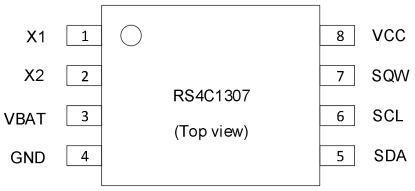


Figure 1 SOP-8/MSOP-8 pin configuration (Top view)

Pin Name	Pin No. SOP-8/MSOP-8	Description
X1	1	Oscillator input
X2	2	Oscillator output
VBAT	3	Battery supply voltage
GND	4	Ground.
SDA	5	Serial Data. Input/output pin for the I2C serial interface. It is open drain and requires an external pullup resistor.
SCL	6	Serial Clock. Used to synchronize data movement on the serial interface
SQW	7	Square-Wave/Output Driver(open drain).
VCC	8	Primary Power Supply.

Typical Application Circuit

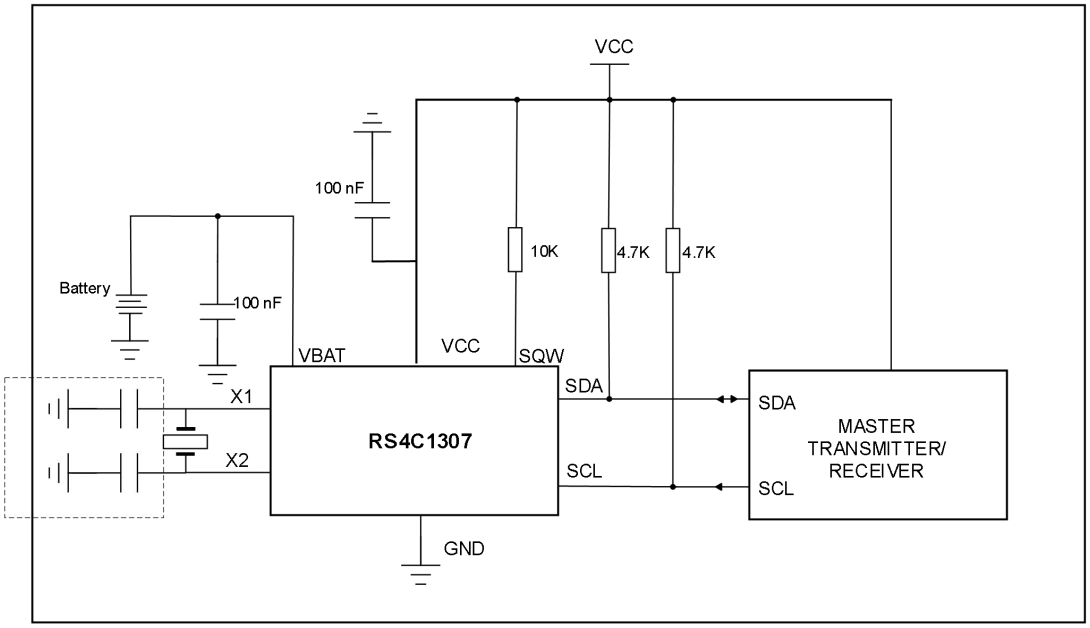


Figure 2 Typical Application Diagram

Notes:

1. It is recommended to add 0.1uf capacitor to VBAT pin.
2. If the time accuracy requirement is high, please reserve the crystal matching capacitor.

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	−55	-	+150	°C
T_{op}	Operating Temperature Range	-40	-	+85	°C
V_{IN}	Voltage Range on Any Pin Relative to Ground	-0.3	-	6	V

Note:
Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VCC	VCC Voltage	2.97	3.3	5.5	V
VIH	SCL/SDA input	0.7 x VCC	-	VCC + 0.3	V
VIL	SCL/SDA input	-0.3	-	+0.3 x VCC	V
VPF	Power-Fail Voltage	2.7	2.82	2.97	
VBAT	Battery Voltage	1.4	3.0	3.7	V

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 85°C, ($V_{CC(MIN)}$ ≤V_{CC}≤ $V_{CC(MAX)}$)

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
V_{BAT}	Battery Voltage*1		1.4		3.7	V
I_{LI}	Input Leakage	SCL only	-	-	1	µA
I_{LO}	I/O Leakage	SDA and SQW		-	1	µA
I_{OLSDA}	SDA Logic 0 Output	V_{CC} > 2V; V_{OL} = 0.4V	-	-	3	mA
		V_{CC} < 2V; V_{OL} = 0.2 V_{CC}	-	-	3	mA
I_{OLSQW}	SQW/OUT Logic 0 Output	V_{CC} > 2V; V_{OL} = 0.4V	-	-	3	mA
		1.71V < V_{CC} < 2V; V_{OL} = 0.2 V_{CC}	-	-	3	
		1.3V < V_{CC} < 1.71V; V_{OL} = 0.2 V_{CC}	-	-	250	mA
I_{CCA}	Active Supply Current Supply Current	SCL clocking at max frequency = 400kHz	-	120	200	µA
I_{CCS}	Standby Current	Specified with the I2C bus inactive	-	85	125	µA
I_{BATLKG}	V_{BAT} Leakage Current (V_{CC} Active)			25	100	nA
$I_{BATOSC1}$	V_{BAT} Current (O_{SC} ON)	V_{BAT} = 3.7V, SQW/OUT OFF		400	1200	nA
$I_{BATOSC2}$	V_{BAT} Current (O_{SC} ON)	V_{BAT} = 3.7V, SQW/OUT ON (32kHz)		570	1400	nA
I_{BATDAT}	V_{BAT} Data-Retention Current (O_{SC} Off)	V_{BAT} = 3.7V		10	100	nA

Crystal Specifications

Symbol	Parameter	MIN	TYP	MAX	Units
f_O	Nominal Frequency		32.768		kHZ
ESR	Series Resistance			70	kΩ
C_L	Load Capacitance		12.5		pF

Note:
1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

AC Electrical characteristics

(TA = -40°C to +85°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			µs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			µs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			µs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			µs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			µs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time*3/4	Fast mode	0		0.9	µs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			µs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7				10	pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay*8			100		ms

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. After this period, the first clock pulse is generated
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL
4. The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,MAX} + t_{SU:DAT} = 1000 + 250 = 1250$ns before the SCL line is released.
6. C_B—total capacitance of one bus line in pF
7. Guaranteed by design. Not production tested
8. The parameter t_{OSF} is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC\,MAX}$ and $1.4V \leq V_{BAT} \leq 3.7V$

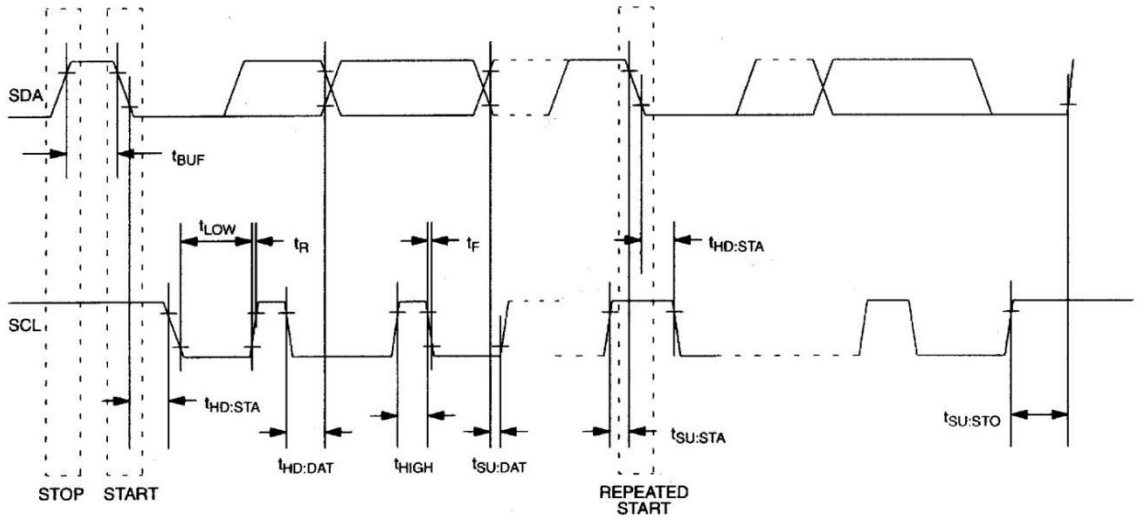


Figure 3 Timing Diagram

Power-Up/Power-Down Characteristics

(TA = -40°C to +85°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
t_{REC}	Recovery at Power-Up*2				2	ms
t_{VCCF}	V_{CC} Fall Time	V_{PF}(MAX) to V_{PF}(MIN)	300			µs
t_{VCCR}	V_{CC} Rise Time	V_{PF}(MIN) to V_{PF}(MAX)	0			µs

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

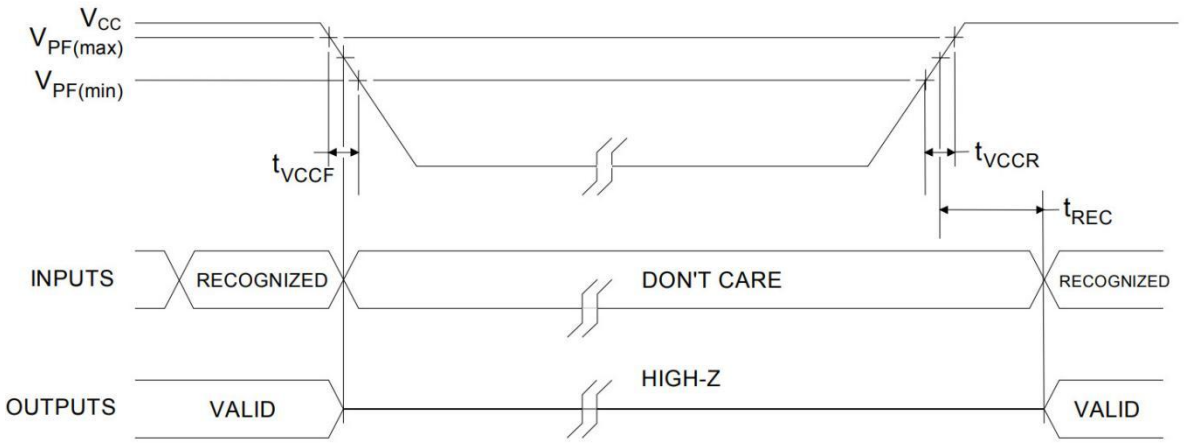


Figure 4 Power-Up/Power-Down Timing

Functional Description

The RS4C1307 serial RTC is a low-power, full BCD clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The RS4C1307 has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply.

The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 12.5pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1.

RS4C1307 has a Backup supply input for any standard 3V lithium cell or other energy source. V_{BAT} voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not required, V_{BAT} must be grounded. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and V_{CC} is below V_{PF}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is open drain and requires an external pullup resistor.

Application Information

The RS4C1307 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BAT}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT}. The registers are maintained from the V_{BAT} source until V_{CC} is returned to nominal levels. The block diagram shows the main elements of the RS4C1307.

An enable bit in the seconds register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long start-up times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within 1 second.

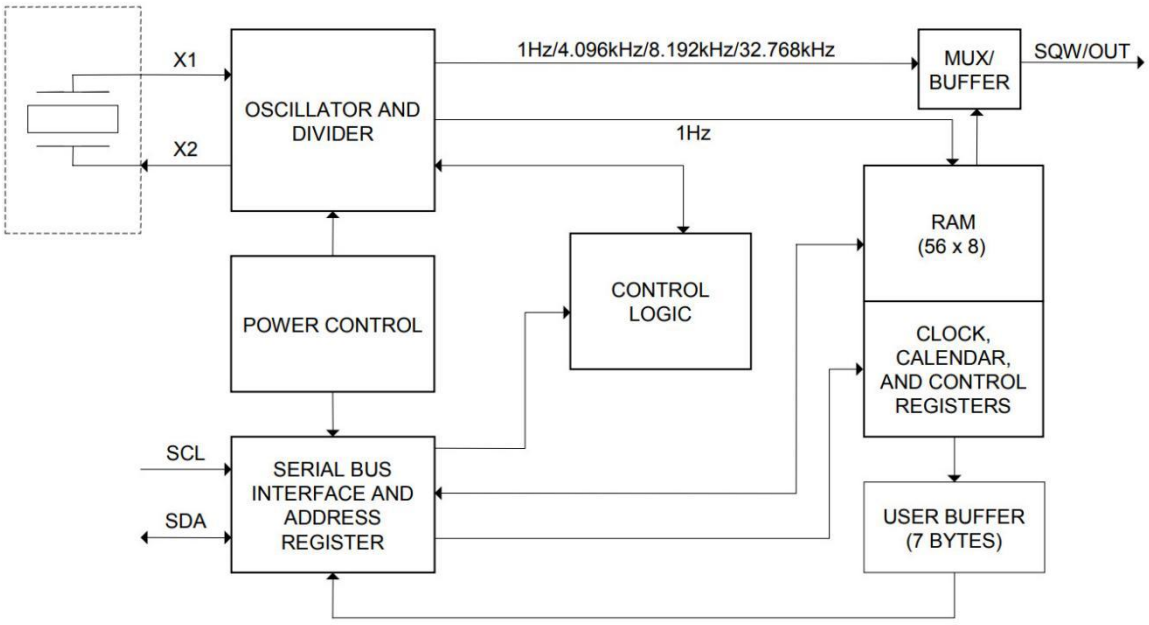


Figure 5 Block Diagram

Oscillator Circuit

RS4C1307 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Figure: Oscillator Circuit Showing Internal Bias Network shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

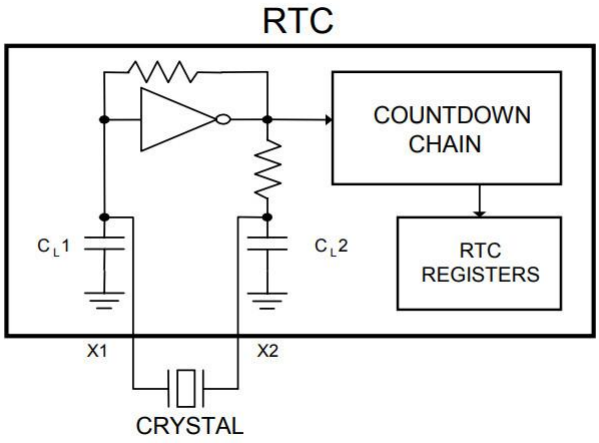


Figure 6 Oscillator Circuit Showing Internal Bias Network

Clock Accuracy

The accuracy of the clock is dependent on the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast.

RTC And RAM Address Map

The RTC registers and control register are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multibyte access, when the register pointer reaches 3Fh (the end of RAM space) it wraps around to location 00h (the beginning of the clock space). On an I2C START, STOP, or register pointer incrementing to location 00h, the current time and date is transferred to a second set of registers. The time and date in the secondary registers are read in a multibyte data transfer, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Clock And Calendar

The time and calendar information is obtained by reading the appropriate register bytes. See Figure RTC and RAM Address Map for the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The clock can be halted whenever the timekeeping functions are not required, which decreases V_{BAT} current.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the RS4C1307. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

RTC and RAM Address Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12/24	AM/PM 10 Hour	10 Hour	Hour				Hour	1-12 +AM/PM 00-23
03H	0	0	0	0	0	Day			Day	1-7
04H	0	0	10 Date		Date				Date	01-31
05H	0	0	0	10 Month	Month				Month	01-12
06H	10 Year				Year				Year	00-99
07H	OUT	0	OSF	SQWE	0	0	RS1	RS0	Control	
08H-3FH									RAM 56 x 8	00H-FFH

Note: Bits listed as "0" always read as a 0

Seconds register(0x00)

D7(CH)	D6	D5	D4	D3	D2	D1	D0
CH=1:oscillator stop CH=0:oscillator enable	10 seconds			Seconds			

Minutes register(0x01)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			Minutes			

Hours register(0x02)

D7	D6(12/24)	D5	D4	D3	D2	D1	D0
0	D6=1:12H mode D6=0:24H mode	When D6=1: D5=1:PM time D5=0:AM time When D6=0: D5 is the second 10-hour bit (20 – 23 hours)	10 Hour	Hours			

Day register(0x03)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	Day		

Date register(0x04)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	10 dates		Date			

Month register(0x05)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	10M	Month			

Year register(0x06)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Control register(0x07)

D7(OUT)	D6	D5(OSF*1)	D4(SQWE)	D3	D2	D1(RS1)	D0(RS0)
Output driver pin When D4(SQWE)=0 OUT=0,IC pin7 outputs low OUT=1,IC pin7 outputs high	0	OSF=1:The oscillator has stopped or was stopped for some time period	SQWE=1:Square-Wave Enable SQWE=0:Square-Wave disable	0	0	When SQWE=1. 00:1Hz 01:4.096kHz 10:8.192kHz 11:32.768kHz	

Note: The following are examples of conditions that may cause the OSF bit to be set:
The first time power is applied.
The voltage present on VCC and VBAT are insufficient to support oscillation.
The CH bit is set to 1, disabling the oscillator.
External influences on the crystal (i.e., noise, leakage, etc.).
This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged

RAM register(0x08-0x3F)

D7	D6	D5	D4	D3	D2	D1	D0
RAM 56 x 8							

Note that the initial power-on state of all registers, unless otherwise specified, is not defined. Therefore all registers are required to be initialized during initial configuration,include enable the oscillator (CH = 0) .

I2C Bus Interface

The RS4C1307 supports the I2C protocol. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The RS4C1307 operates as a slave on the I2C bus. Within the bus specifications, a standard mode (100kHz cycle rate) and a fast mode (400kHz cycle rate) are defined. The RS4C1307 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.
Slave addresses have a fixed length of 7 bits. The slave address is [**1101000**].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

Slave address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	R/W
1	1	0	1	0	0	0	1 = Read
							0 = Write

Read mode

In this mode, the master reads the slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the

master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

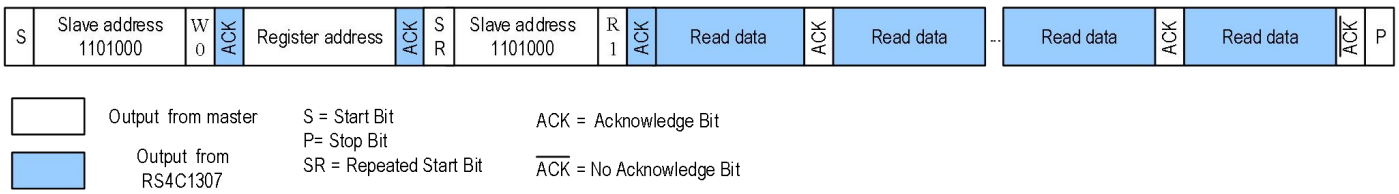


Figure 7 Read Mode Sequence

Write mode

In this mode the master transmitter transmits to the slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

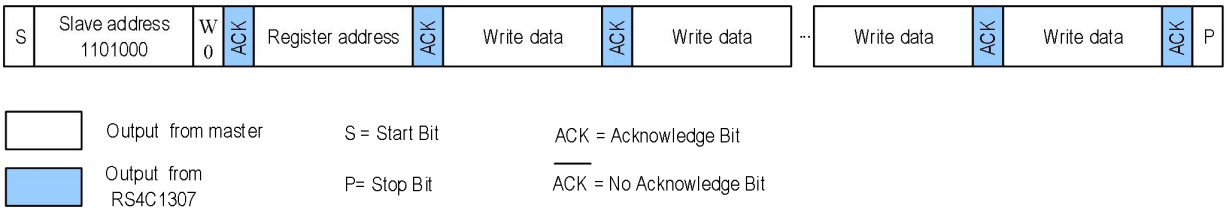
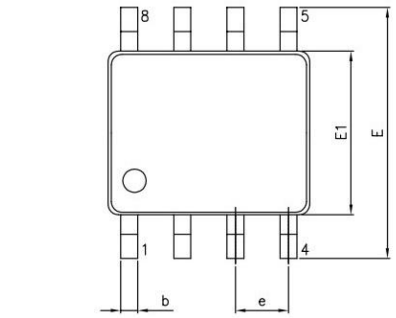
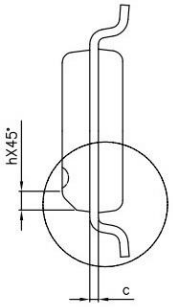


Figure 8 Write Mode Sequence

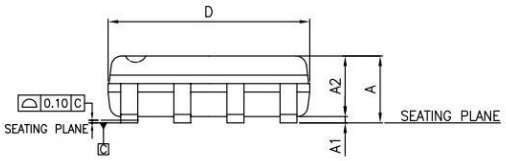
Package Information

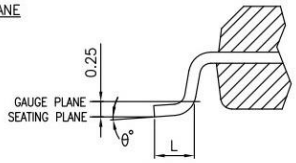
SOP-8 Package

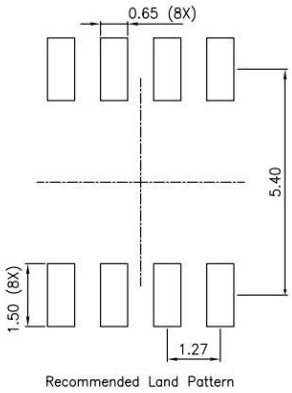




SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	—	1.27
h	0.25	—	0.50
θ°	0	—	8





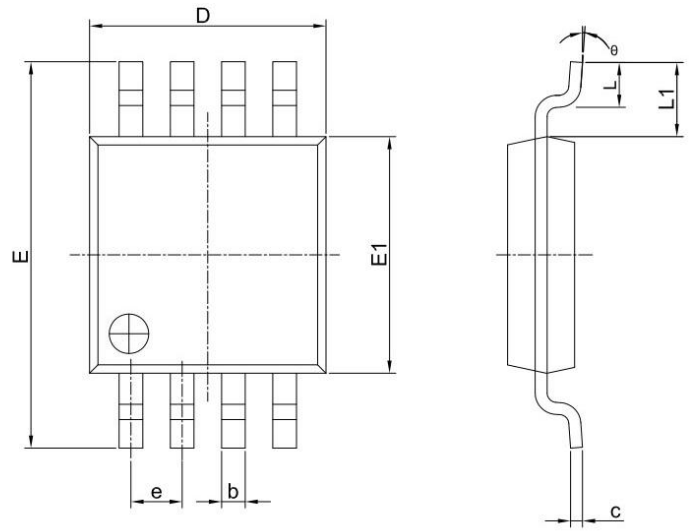


Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

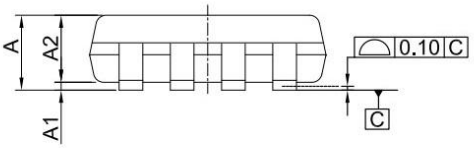
SOP08 POD

Raystar Microelectronics Technology Inc.

MSOP-8 Package



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°



Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-187
3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	Initial Release	2025/12/15