Features

- Built-in 32.768 kHz DTCXO
- Interface Type: I2C-Bus (Up to 400 kHz)
- Low current consumption at backup: 700nA / 3.0 V Typ.
- Wide time-keeping voltage range:1.5V to 5.5V
- Wide interface voltage range: 1.6V to 5.5V programmed H / L level also.
- Alarm interrupt function: Combination of Day, Date, Hour, Minute, and AE bit
- Wakeup timer interrupt function: Auto repeated 244.14 μs to 32 years
- Time update interrupt function: Every second or every minute
- Temperature compensated 32.768 kHz or other output: Available output enable control
- Auto correction of leap years: Writing of "60 seconds" is available for Leap Second adjustment

Applications

- High Performance Server
- 5G base station
- Communication equipment

Description

This module is an I2C-Bus interface-compliant real-time clock which includes a 32.768 kHz DTCXO.

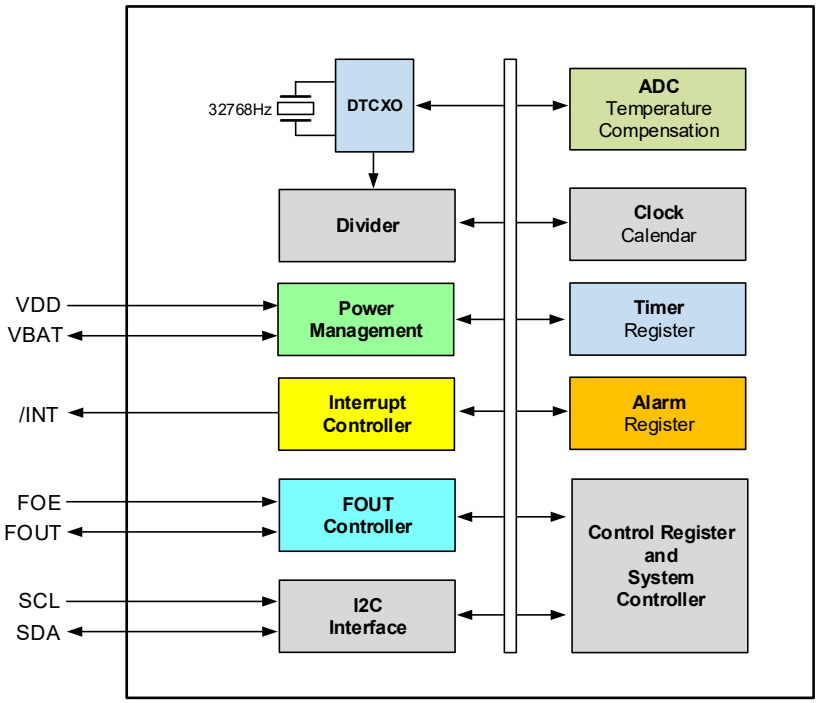
In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, wakeup timer function, time update interrupt function, 32.768 kHz output function.

The devices in this module are fabricated via a CMOS process for low current consumption, which enables long- term battery back-up.

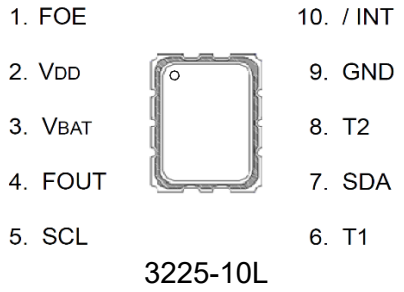
Ordering Information

Part Number	Package	Description
RS4TC8900AC	3225-10L	3.2mmX2.5mm
RS4TC8900AS	SOP14	10.1mmX7.4mm

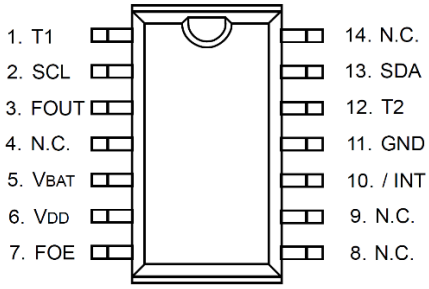
Block Diagram



Pin Configuration



3225-10L



SOP-14

Pin Name	3225-10	SOP-14	Type	Description
FOE	1	7	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
VDD	2	6	Power	This pin is connected to a positive power supply.
V_{BAT}	3	5	Power	This is the power supply pin for backup battery. Connect this pin to a large-capacity capacitor, a secondary battery or similar. When the battery switchover function is not needed, VBAT must be connected to VDD.
FOUT	4	3	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
SCL	5	2	Input	This is the serial clock input pin for I2C Bus communications.
T1	6	1	Input	Used by the manufacturer for testing. (Do not connect externally.)
SDA	7	13	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I2C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull- up resistance relative to the signal line capacity.
T2	8	12	Input	Used by the manufacturer for testing. (Do not connect externally.)
GND	9	11	Power	This pin is connected to ground.
/INT	10	10	Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
N.C.		4,8,9,14	-	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.

Note: Be sure to connect a bypass capacitor rated at least 0.1 μF between VDD and GND.

Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage	Vdd	Between VDD and GND	−0.3 to +6.5	V
Input voltage (1)	Vin1	SCL, SDA, pins	GND −0.3 to +6.5	V
Output voltage (1)	Vout1	FOUT pins	GND −0.3 to VDD +0.3	V
Output voltage (2)	Vout2	SDA and /INT pins	GND −0.3 to +6.5	V
Storage temperature	Tstg	When stored separately, without packaging	−55 to +125	°C

Recommended Operating Conditions

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Operating supply voltage Normal mode (2)	V_{ACCSW}	Between VDD and GND	2.5	3.0	5.5	V
Operating supply voltage In case of single supply (VDD = VBAT) (1)	V_{ACC}	Between VDD and GND (VDD = VBAT)	1.6	3.0	5.5	V
Backup power supply voltage	VBAT	Between VBAT and GND	1.6	3.0	5.5	V
Temp. compensation voltage	V_{TEM}	Temperature compensation voltage	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	—	1.5	3.0	5.5	V
Operating temperature	Ta	No condensation	−40	+25	+85	°C

- To apply Min. value of VACC and VCLK, the VDD and VBAT needs to be supplied with more than 1.6 V at least for the oscillation to stabilize (oscillation start time tSTA).
- VACCSW is the normal mode operation voltage, at which the Battery backup switchover function is enabled.
- The Min. value of VCLK is the Min. voltage required to retain the time counting function. It is however necessary to maintain VTEM till the oscillation of the oscillator has stabilized (oscillation start time tSTA).
- The temperature compensation stops working below Min. value of VTEM.

Frequency Characteristics

Item	Symbol	Condition	Rating	Unit
Frequency stability	Δf/f	Ta= -40~85°C, V_{DD} = 3.0 V	±5 (1)	× 10^{-6}
Frequency/voltage characteristics	f/V	Ta= +25 °C, V_{DD}=1.6 V to 5.5 V	±1.0 Max.	× 10^{-6} / V
Duty-cycle	t_{DC}	50% V_{DD} level, +25 °C, V_{DD} = 1.6 V to 5.5 V	50 ± 10	%
VOscillation start time	tSTA	Ta = +25 °C, V_{DD} = 1.6 V ~ 5.5 V Ta = -40 to + 85°C, V_{DD} = 1.6 V to 5.5 V	1.0 Max. 3.0 Max.	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V, first year	±3 Max.	× 10^{-6} / year
Reflow	fref	260 °C Max. 2 times	±3 Max. (2)	× 10^{-6}

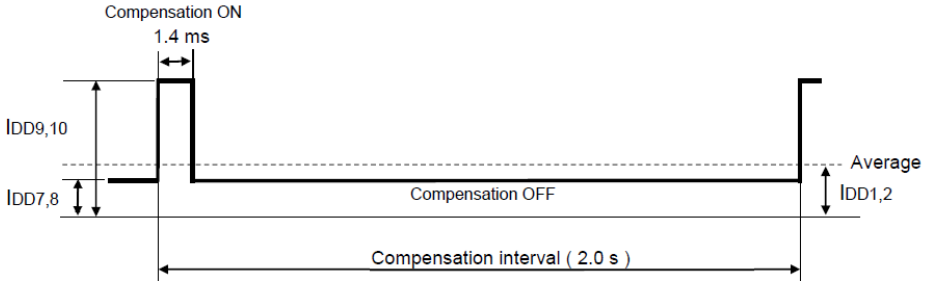
- 9.8 s error per a month.
- The result that it was measured at 25 °C, 24 hours after processing of reflow soldering.

Electrical Characteristics

Unless otherwise specified, GND = 0 V, V_{DD} = 1.6 V to 5.5 V, Ta = −40 °C to +85 °C

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Average Current consumption (1)	IDD1	f_{SCL} = 0 Hz, /INT = Hi-Z, FOUT is stopped Temp compensation interval 2.0 s	VDD = 5 V		0.75	2.6	µA
Average Current consumption (2)	IDD2		VDD = 3 V		0.69	2.4	
Average Current consumption (3)	IDD3	f_{SCL} = 0 Hz, /INT = Hi-Z, FOUT outputs 32 kHz, CL = 0 pF Temp compensation interval 2.0 s	VDD = 5 V		2.19	3.6	
Average Current consumption (4)	IDD4		VDD = 3 V		1.59	3.0	
High-level input voltage	VIH1	SCL, SDA		0.8 × VDD		5.5	V
Low-level input voltage	VIL	SCL, SDA		GND − 0.3		0.2 × VDD	
High-level output voltage	VOH1	FOUT	VDD = 5 V, IOH = −1 mA	4.5		5.0	
	VOH2		VDD = 3 V, IOH = −1 mA	2.2		3.0	
	VOH3		VDD = 3 V, IOH = −100 µA	2.9		3.0	
Low-level output voltage	VOL1	FOUT	VDD = 5 V, IOL = 1 mA	GND		GND + 0.5	
	VOL2		VDD = 3 V, IOL = 1 mA	GND		GND + 0.8	
	VOL3		VDD = 3 V, IOL = 100 µA	GND		GND + 0.1	
	VOL4	/INT	VDD = 5 V, IOL = 1 mA	GND		GND + 0.25	
	VOL5		VDD = 3 V, IOL = 1 mA	GND		GND + 0.4	
	VOL6	SDA	VDD ≥ 2 V, IOL = 3 mA	GND		GND + 0.4	
Input leakage current	ILK	INPUT pins, VIN = VDD or GND		−0.5		0.5	µA
Output leakage current	IOZ	Output pins, output voltage = VDD or GND		−0.5		0.5	
Detection voltage of VDET	VDET	(VDD = VBAT)		1.45	1.5	1.55	V
Detection voltage of VLF	VLOW	VDD		1.1	1.2	1.3	

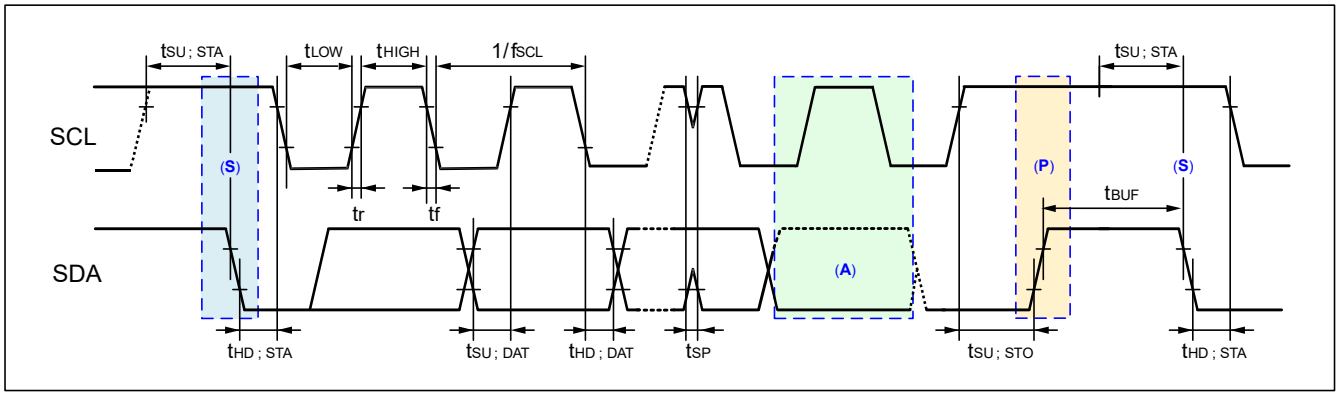
The current consumption of RS4TC8900A increases at a timing of a temperature compensation. As for this peak current consumption, it occurs in about 1.4ms.IDD1, IDD2 is the average current consumption at temperature compensation in 2 second's cycle.



AC Characteristics for I2C

Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = −40 °C to +85 °C

Item	Symbol	Condition	Standard Mode		Fast Mode		Unit
			MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	–	–	100	–	400	kHz
Start condition setup time	$t_{SU;STA}$	–	4.7	–	0.6	–	μs
Start condition hold time	$t_{HD;STA}$	–	4.0	–	0.6	–	μs
Data setup time	$t_{SU;DAT}$	–	250	–	100	–	ns
Data hold time	$t_{HD;DAT}$	–	0	–	0	–	ns
Stop condition setup time	$t_{SU;STO}$	–	4.0	–	0.6	–	μs
Bus idle time between start condition and stop condition	t_{BUF}	–	4.7	–	1.3	–	μs
Time when SCL = "L"	t_{LOW}	–	4.7	–	1.3	–	μs
Time when SCL = "H"	t_{HIGH}	–	4.0	–	0.6	–	μs
Rise time for SCL and SDA	t_r	–	–	1.0	–	0.3	μs
Fall time for SCL and SDA	t_f	–	–	0.3	–	0.3	μs
Allowable spike time on bus	t_{SP}	–	–	50	–	50	ns



- As for the communication time of I2C-Bus, completion of less than 1 second is recommended.
- If such communication requires 1 second (Max.) or longer, the I2C-Bus interface is reset by the internal bus timeout function. When bus-time-out occur, SDA is released to Hi-Z input mode.
- During access to the time registers, the time counting is on hold! This means that up to 1 second can be "lost" in case of unsuccessful communication as mentioned above!
- Please make sure to send I2C start condition before actual transmission of the RTCs slave address as otherwise the slave address appears to be shifted by 1 bit!

Functional descriptions

1. Description of Registers

Address 00h to 0Fh: Basic time and calendar register. It is compatible with RS4TC8900
Address 10h to 2Fh: Extension register
Address is incremented automatically in lower 4 bits address.
Upper 4bits address are fixed. (00, ..., 0E, 0F, 00, 01), (10, ..., 1E, 1F, 10, 11)，(20, ..., 2E, 2F, 20, 21)

	Basic register	Time stamp register	Extension register	Access is prohibited
Address (8bit)	0Fh from 00h	1Fh from 10h	2Fh from 20h	FFh from 30h

- **Register Table (Basic time and calendar register) (00h ~ 0Fh)**

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
0	SEC	○	40	20	10	8	4	2	1		√
1	MIN	○	40	20	10	8	4	2	1		√
2	HOUR	○	○	20	10	8	4	2	1		√
3	WEEK	○	6	5	4	3	2	1	0		√
4	DAY	○	○	20	10	8	4	2	1		√
5	MONTH	○	○	○	10	8	4	2	1		√
6	YEAR	80	40	20	10	8	4	2	1		√
7	RAM	●	●	●	●	●	●	●	●		√
8	MIN Alarm	AE	40	20	10	8	4	2	1		√
9	HOUR Alarm	AE	●	20	10	8	4	2	1		√
0A	WEEK Alarm	AE	6	5	4	3	2	1	0		√
	DAY Alarm		●	20	10	8	4	2	1		
0B	Timer Counter 0	128	64	32	16	8	4	2	1		√
0C	Timer Counter 1	32768	16384	8132	4096	2048	1024	512	256		√
0D	Control1	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	02h	√
0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	00h	√ *
0F	Control2	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	40h	√

○ Writing is avoided. Read value is 0, always. ● It can read and write. √ is available. - avoid.
"Init" shows value of after power-on Reset. Unit is Hex.
*Note Refer to Flag Registers

Notes	After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC. Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.
	Only a 0 can be written to the UF, TF, AF, VLF, VDET and EF bit. The EVMON bit is read only bit.
	Any bit marked with "○" should be used with a value of "0" after initialization.
	Any bit marked with "●" is a RAM bit that can be used to read or write any data.
	The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.
	If an alarm function is not used, registers 08h-0Ah can be used as RAM. (AIE: "0")
	Reading register value of address 0Bh-0Ch and 1Fh is pre-set data. If a timer function is not used, register of 0Bh-0Ch and 1Fh can be used as RAM. (TE, TIE: "0")

- **Register Table (Timer) (10h ~ 1Fh)**

0x10~17、0x19、0x1A test registers are reserved，do not to write.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
17	TEMP	128	64	32	16	8	4	2	1		R
18	Backup Function 1	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	00h	R/W
1B	Timer set	TSTP	TRES	○	○	○	○	○	○	00h	√
1C	Timer0	128	64	32	16	8	4	2	1	00h	–
1D	Timer1	32768	16384	8192	4096	2048	1024	512	256	00h	–
1E	Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	00h	–
1F	Timer counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	00h	√

- **Extension register(20h ~ 2Fh)**

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	R/W
20	Device ID	Do not to write									R
21	Backup Function 2	○	○	○	○	○	VBATSW	○	○	00h	R/W
22	RSV	Test， Do not to write								00h	R/W
23	Reg selection	Test， Do not to write								00h	R/W
24	RSV	Reserved								00h	R/W
25	Frequency offset Ctrol 1	○	○	○	○	○	○	offset step 1	offset step 0	00h	R/W
26	Frequency offset Ctrol 2	enable offset 1	enable offset 0	F5	F4	F3	F2	F1	F0	00h	R/W
27	Sub SEC 0	Sub SEC[7:0]									R
28	Sub SEC 1	Reserved						Sub SEC[9:8]			R
29~2F	RSV	Reserved								00h	R/W

○ Writing is avoided. Read value is 0, always. ● It can read and write. √ is available. - avoid.
"Init" shows value of after power-on Reset. Unit is Hex.

0x24、0x29~2F register can be use as RAM.

- **Initial Value of Registers**

	Registers' Initial value after power on reset
Initial Value	Register
1	TSEL1, VLF, VDET, CSEL0
0	TEST, WADA, USEL, TE, FSEL1, FSEL0, TSEL0, UF, TF, AF, EF, CSEL1, UIE, TIE, AIE, RESET, TRES, TSTP, All bits of address1Ch,1Dh,1Eh and 1Fh

All other register values are undefined, so be sure to perform a reset before using the module.

- **Quick Reference**

Update interrupt timing		Default
USEL = 0	Once per seconds	√
USEL = 1	Once per minutes	
Output Frequency selection		
FSEL1, FSEL0 = 00	32.768 kHz	√
FSEL1, FSEL0 = 01	1024 Hz	
FSEL1, FSEL0 = 10	1 Hz	
FSEL1, FSEL0 = 11	32.768 kHz	
Timer source clock selection		
TSEL1, TSEL0 = 00	4096 Hz	
TSEL1, TSEL0 = 01	64 Hz	
TSEL1, TSEL0 = 10	Every second update	√
TSEL1, TSEL0 = 11	Every minute update	
Temperature compensation selection		
CSEL1, CSEL0 = 00	0.5 s	
CSEL1, CSEL0 = 01	2.0 s	√
CSEL1, CSEL0 = 10	10 s	
CSEL1, CSEL0 = 11	30 s	

2. Details of Registers

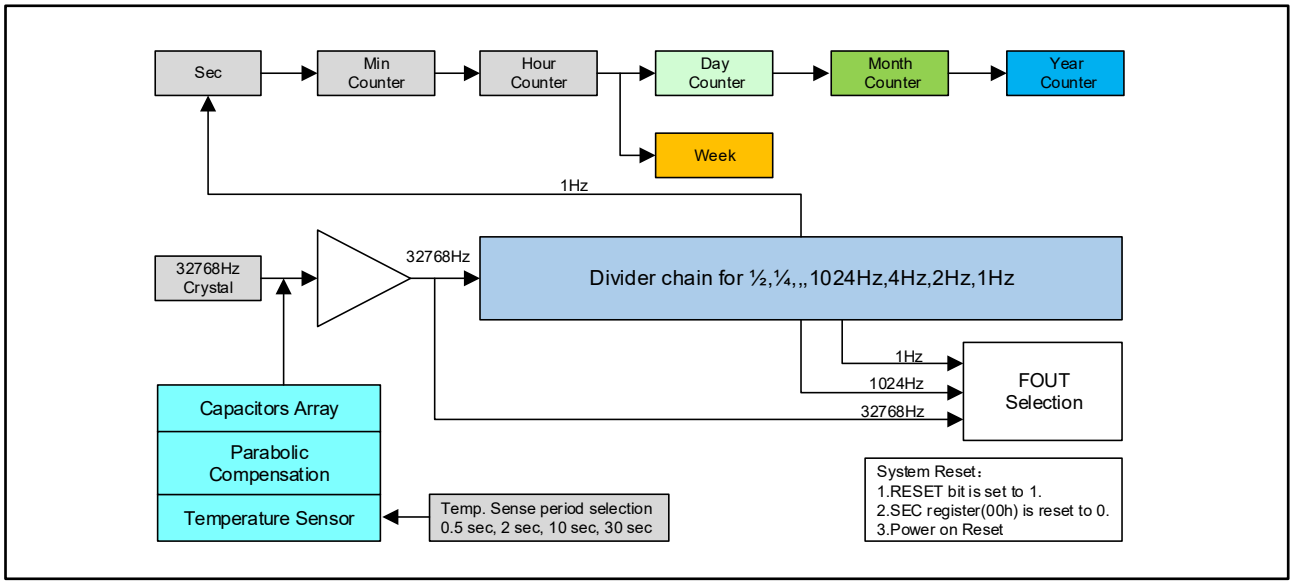
- **Clock Counter (SEC - YEAR)**

The data format is BCD format. For example, when the “seconds” register value is “0101 1001” it indicates 59 seconds. 24hours system is available.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	SEC	○	40	20	10	8	4	2	1
01	MIN	○	40	20	10	8	4	2	1
02	HOUR	○	○	20	10	8	4	2	1
03	WEEK	○	6	5	4	3	2	1	0
04	DAY	○	○	20	10	8	4	2	1
05	MONTH	○	○	○	10	8	4	2	1
06	YEAR	80	40	20	10	8	4	2	1

(1) SEC register

This second register counts from “00” to “01”, “02”, and up to 59 seconds, after 59 it starts again from 00 second. When written any data to SEC register, less than a SEC counter (512 Hz from 2 Hz) is cleared to zero.Thus, the time accuracy becomes 0 s to 30.5 μs. * (refer to the flowing Figure)



If highly precise time synchronization is needed, RESET bit setting to 1 is most suitable operation.
When 60 seconds were written to SEC register, it returns to 00 second in next update. This special update is the same as plus-adjustment of Leap second. This behavior is useful in the adjustments of Leap second.
*Note Several data writing into SEC register might cumulative time delay.

(2) MIN register

This minute register counts from “00” to “01”, “02”, and up to 59 minutes, after 59 it starts again from 00 minute.

(3) HOUR register

This 24 hours register counts from “00” hour to “01”, “02”, “23”, ”00”, ”01”. “o” indicates write-protected bits. Zero is always read from these bits.

(4) WEEK register

This WEEK register consists of 7bit shift registers.
The data values are counted as follows: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h
The correspondence between days and count values is shown below.

WEEK	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of week	Data
Write / Read	0	0	0	0	0	0	0	1	Sunday	01h
	0	0	0	0	0	0	1	0	Monday	02h
	0	0	0	0	0	1	0	0	Tuesday	04h
	0	0	0	0	1	0	0	0	Wednesday	08h
	0	0	0	1	0	0	0	0	Thursday	10h
	0	0	1	0	0	0	0	0	Friday	20h
	0	1	0	0	0	0	0	0	Saturday	40h
Write prohibit	* Do NOT set "1" more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								—	—

(5) DAY Register

The updating of DAY register varies according to the month setting.
A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01", "02", "03", to "28", "29", "01".

DAY	Month	Date update pattern
Write / Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in common year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

(6) MONTH register

This MONTH register counts from 01 (January), 02 (February), and up to 12 (December), then starts again since 01 (January).

(7) YEAR register

This YEAR register counts from 00, 01, 02 and up to 99, then starts again since 00. Any year multiple of four (04, 08, 12, 88, 92, 96, etc.) works as a leap year.

● Alarm Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN Alarm	**AE**	40	20	10	8	4	2	1
9	HOUR Alarm	**AE**	●	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
0D	Control1	TEST	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
0F	Control2	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and "1" is set to the AF bit to report that an alarm interruption has occurred.
Please refer to Alarm Interrupt Function.

● Wakeup Timer Control Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0B	Timer Counter 0	128	64	32	16	8	4	2	1	√	√
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	√	√
1B	Timer set	TSTP	TRES	○	○	○	○	○	○	√	√
1C	Timer0	128	64	32	16	8	4	2	1	√	
1D	Timer1	32768	16384	8192	4096	2048	1024	512	256	√	

1E	Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	√

These registers are used to set the preset countdown value for the wakeup timer interrupt function. The **TE, TF, TIE, and TSEL0 / 1 bits** are also used to set the wakeup timer interrupt function.
When the value in the above wakeup timer control register just changes from 01h to 00h, the /INT pin goes to low level and “1” is set to the TF bit to report that a wakeup timer interrupt event has occurred.
Please refer to Wakeup timer Control function.

- **Control Registers, Flag Registers**

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Control1	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
	(Default)	0	0	0	0	0	0	1	0
0E	Flag register	○	○	UF	TF	AF	○	VLF	VDET
	(Default)	0	0	0	0	0	0	1	1
0F	Control2	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET
	(Default)	0	1	0	0	0	0	0	0

The default value is loaded after powering up from 0 V, automatically.
TEST must be always cleared by a zero.
This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as wakeup timer operations.

(1) TEST bit

This is the manufacturer's test bit. Its value should always be “0”. Be careful to avoid writing “1” to this bit when writing to other bits.

TEST	Data	Description
Write	0	TEST bit is cleared to 0
	1	Setting prohibited (manufacturer's test bit)
Read	0	TEST bit has been cleared to 0
	1	TEST bit has been set to 1. Please reset to 0

(2) VLF (Voltage Low Flag) bit

This flag bit indicates the history of clock operations due to low voltage.
Its value change from “0” to “1” indicates a possibility of data loss or time data error, and all the data of registers should be initialized.
Once this flag bit's value is “1”, its value is retained until a “0” is written to it. After powering up from 0 V, make sure to set this bit's value to “1”.

VLF	Data	Description
Write	0	The VLF bit is cleared to 0 to prepare for the next status detection
	1	VLF data remains even it was 0 or 1. To retain the data, please write 1
Read	0	No supply voltage drops occurred
	1	Low voltage has been detected, so data loss might have occurred, and time information might be wrong. All registers should be initialized

(3) VDET (Voltage Detection Flag) bit

This flag bit indicates the history of the voltage for temperature compensation circuit.
Its value changes from “0” to “1” indicates that the temperature compensation function has stopped operation due to a supply voltage drop. Once this flag bit's value is 1, its value is retained until a 0 is written to it.
After powering up from 0 V, make sure to set this bit's value to “1”. Please confirm table in Backup and Recovery.

VDET	Data	Description
Write	0	The VDET bit is cleared to 0 to prepare for the next low voltage detection
	1	VDET data remains even it was 0 or 1. To retain the data, please write 1
Read	0	Temperature compensation is normal
	1	Temperature compensation has been stopped

(4) RESET bit

When highly precise synchronization of both time, timer is necessary, use RESET.

RESET	Data	Description
Write	0	Writing 0 is invalid
	1	Writing 1 resets 16384 Hz ~2 Hz of 32.768 kHz counter
Read	0	The read value of RESET is 0, always writes 0, it is invalid
	1	writes 1, it executes reset of count-down-chain from 32.768kHz

For example.
S is start condition. P is stop condition. [Write access to RESET-bit.]
S---Slave address(w)---ACK1---0Fh---ACK2---01h---ACK3---P.
RESET executes and it keeps between P from ACK3. After P, RESET bit clears automatically.
Reset area of circuit are the count-down-chain of 2 Hz from 16 kHz, are cleared. As for next update timing of a Seconds counter from RESET.The range is 1000 ms--30.5 μs from just 1000 ms.
RESET affects time update interruption, alarm, FOUT and timer. But it doesn't affect 32 kHz output.

Note:
RESET is released by the reception of a START or RE-START condition before receiving a STOP condition. The Single write access is recommended for precise RESET.Unnecessary use of RESET will be the cause of delay error of time.

(5) USEL (Update Interrupt Select) bit

This bit is used to define if the RTC should output a “second update” or “minute update” interrupt, allowing to synchronize external clocks with the time registers of the RTC.

(6) TSEL0, 1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the wakeup timer interrupt function (four settings can be made).

(7) FSEL0, 1 (FOUT frequency Select 0, 1) bits

The combination of these two bits is used to set the FOUT frequency. Note: All frequencies are temperature compensated.

FSEL0,1	FSEL1 (bit 3)	FSEL0 (bit 2)	FOUT frequency
Write / Read	0	0	32.768 kHz (Default)
	0	1	1024 Hz
	1	0	1 Hz
	1	1	32.768kHz

(8) CSEL0, 1 (Compensation interval Select 0, 1) bits

The combination of these two bits is used to set the temperature compensation interval.

(9) AF (Alarm Flag) bit

If set to “0” beforehand, this flag bit's value changes from “0” to “1” when an alarm interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.

(10) TF (Timer Flag) bit

If set to “0” beforehand, this flag bit's value changes from “0” to “1” when a wakeup timer interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.

(11) UF (Update Flag) bit

If set to “0” beforehand, this flag bit's value changes from “0” to “1” when a time update interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.

(12) AIE, TIE, UIE (Alarm, Wakeup Timer, Update Interrupt Enable) bit

In case of Alarm or Wakeup Timer or Update occurs AIE, TIE, UIE bit controls /INT output.
When a “1” is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) . When a “0” is written to this bit, no interrupt signal is generated.

Function	condition	Flag	/INT interrupt control
Alarm	Alarm time hit	AF	AIE
Wakeup Timer	Timer Count down to 0	TF	TIE
Update	Minute or Second update	UF	UIE

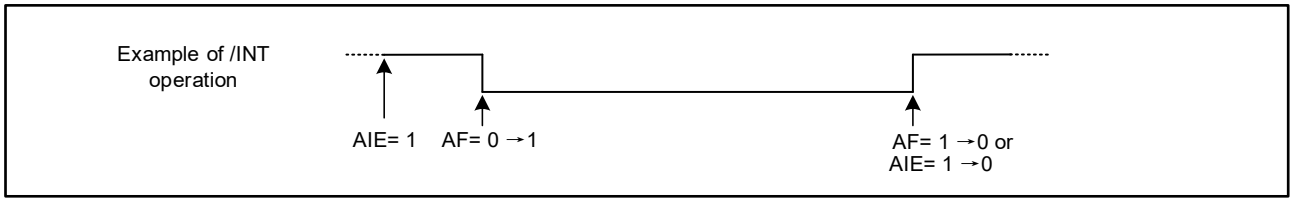
/INT pin Operation when an Interrupt Occurs.

- ***How to identify events when the interrupt output occurs***
  /INT output pin is common output terminal of interrupt events of four types Wakeup timer, alarm, time update .
  When an interrupt occurs, please read the TF, AF, UF flag to confirm which types of events occurred.
- ***Processing method in case of no using /INT output.***
  Please keep /INT pin open.
  Please set “0” to TIE, AIE, UIE bits and do poling TF, AF, UF.

3. Alarm Interrupt Function

● Alarm Interrupt Generation

The alarm interrupt function generates interrupt events at the matching time of alarm day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to “1” and the /INT pin goes to low level to indicate that an event has occurred.



Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN Alarm	**AE**	40	20	10	8	4	2	1
9	HOUR Alarm	**AE**	●	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
0D	Control1	TEST	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
0F	Control 2	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

* ”○” indicates write-protected bits. A zero is always read from these bits.
* Bits marked with” ●”are RAM bits that can contain any value and are read/write-accessible.
* Before entering settings for operations, it is recommended that writing “0” to the AIE bit to prevent unexpected hardware interrupts.
* When the RESET bit value is “1” alarm interrupt events do not occur.
* When the alarm interrupt function is not used, the Alarm registers (Reg – 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write “0” to the AIE bit.
* When the AIE bit value is “1” and the Alarm registers (Reg – 08h to 0Ah) is being used as a RAM register, /INT may be changed to low level unintentionally.

● Alarm registers

The minute, hour, day and date when an alarm interrupt event is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (0Ah), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

Unwanted alarm term is decided by setting respective AE bit =”1”. If AE is set to “1”, this alarm term becomes inactive.

Ex. WEEK Alarm / DAY Alarm (0Ah) = 80h (AE=”1”) hour, minute, second alarm active week, day alarm inactive Setting all AE bit “1” makes every one second alarm exceptionally. The result is reflected in AF bit.

Alarm event does not occur even user set alarm time to current time. Coming next time matching (alarm time = current time) can occur the event.

(1) WADA (Week Alarm /Day Alarm) bit

The alarm interrupt function uses either” Day” or “Week” as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write / Read	0	Sets WEEK as target of alarm function Register 0Ah is compared with register 03h (DAY setting is ignored)
	1	Sets DAY as target of alarm function Register 0Ah is compared with register 04h (WEEK setting is ignored)

(2) **AF (Alarm Flag) bit**

When this flag bit value is already set to “0”, occurrence of an alarm interrupt event changes it to “1”. When this flag bit value is “1”, its value is retained until a “0” is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred
	1	AF bit is retained even AF is 0 or 1. To retain AF bit, user can write 1.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to 0)

(3) **AIE (Alarm Interrupt Enable) bit**

When an alarm interrupt event occurs (when the AF bit value changes from “0” to “1”), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

AIE	Data	Description
Write / Read	0	When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). Even when the AIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = ”L”)
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is “1”. This value is retained (not automatically cleared) until the AF bit is cleared to zero

- **Examples of Alarm Setting**

(1) **Example of alarm settings when Day has been specified (and WADA bit= 0)**

Day is specified WADA bit = 0	Reg – A								Reg-9	Reg-8
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	HOUR	MIN
	AE	S	F	T	W	T	M	S	Alarm	Alarm
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07h	AE = 1
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	AE = 1	30h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18h	59h
	1	X	X	X	X	X	X	X		

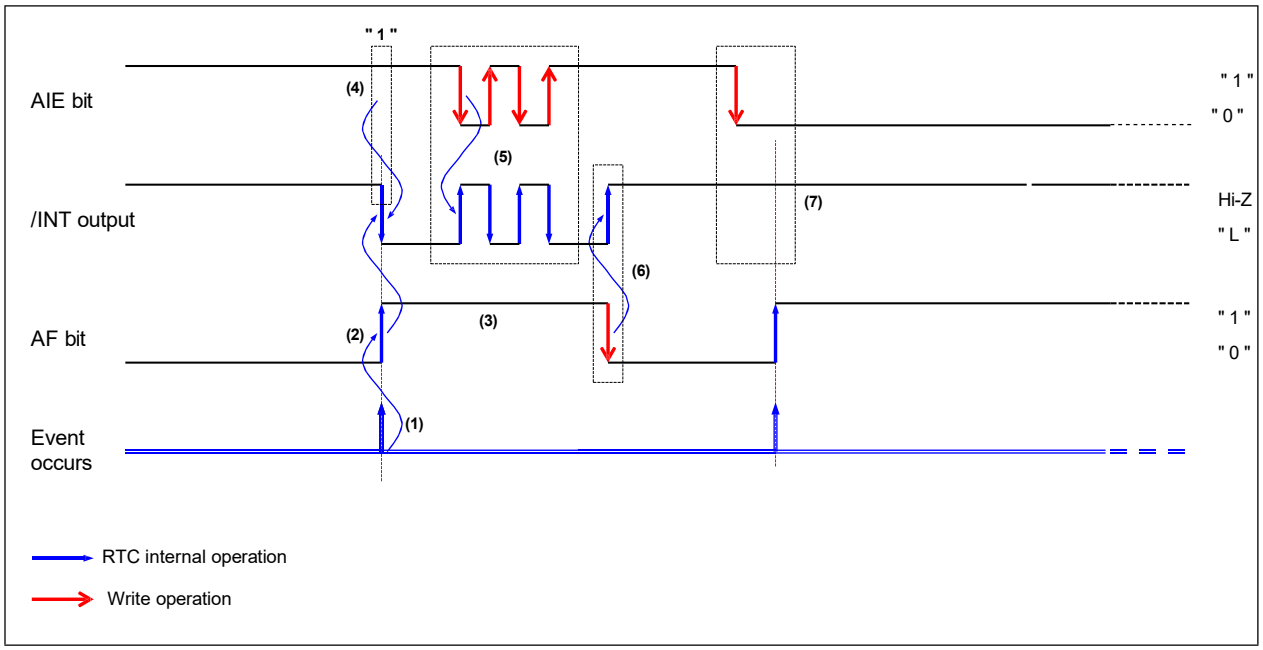
X: Don't care

(2) **Example of Alarm Settings when Day has been Specified (and WADA bit = ”1”)**

Day is specified WADA bit = 1	Reg - A								Reg-9	Reg-8
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	HOUR	MIN
	AE	•	20	10	8	4	2	1	Alarm	Alarm
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	0 h	AE = 1
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	AE = 1	30h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18h	59h

X: Don't care

- **Alarm Interrupt Timing Chart**



(1) The minute, hour, day and date, when an alarm interrupt event is supposed to occur has to be set in advance, along with the WADA bit (Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes “1”.

(3) When the AF bit = 1, its value is retained until it is cleared to zero.

(4) If AIE = 1 when an alarm interrupt occurs, the /INT pin output goes low.
∗ When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.

(6) If the AF bit value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) When the AIE bit value is “0”, and an alarm interrupt occurs, the /INT pin stay Hi-Z.

- **/INT pin Operation when an Interrupt Occurs**

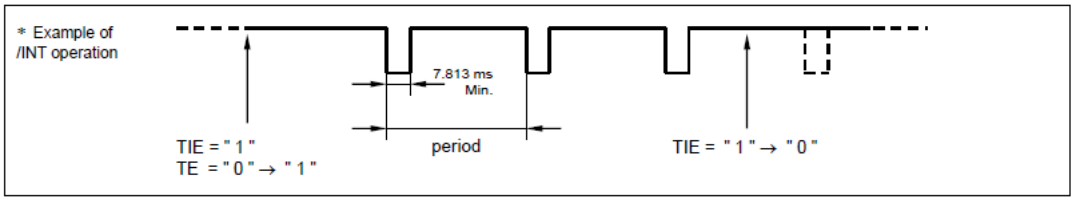
  (1) How to identify events when the interrupt output occurs
  /INT output pin is common output terminal of interrupt events of four types Wakeup timer, alarm, time update interrupt.
  When an interrupt occurs, please read the TF, AF, UF and EF flag to confirm which types of events occurred.

  (2) Processing method in case of no using /INT output. Please keep /INT pin open.
  Please set “0” to TIE, AIE, UIE bits and do poling TF, AF, UF.

4. Wakeup Timer Interrupt Function

- **Interrupt Generation**

The wakeup timer interrupt generation function generates an interrupt event periodically at any wakeup set between 244.14 μs and 32 years.
When an interrupt event is generated, the /INT pin goes to low level and “1” is set to the TF bit to report that an event has occurred. However, when a wakeup timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is “1”. Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared. /INT status changes from low-level to Hi-Z.



- **Wakeup Timer Interruption Registers**

The wakeup timer interrupt generation function generates an interrupt event periodically at any wakeup set between 244.14 s and 16777215 minutes.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0B	Timer Counter 0	128	64	32	16	8	4	2	1	√	√
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	√	√
0D	Control1	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	√	√
0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	√	Clear only
0F	Control2	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	√	√
1B	Timer set	TSTP	TRES	○	○	○	○	○	○	√	√
1C	Timer 0	128	64	32	16	8	4	2	1	√	-
1D	Timer 1	32768	16384	8192	4096	2048	1024	512	256	√	-
1E	Timer 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	-
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	√

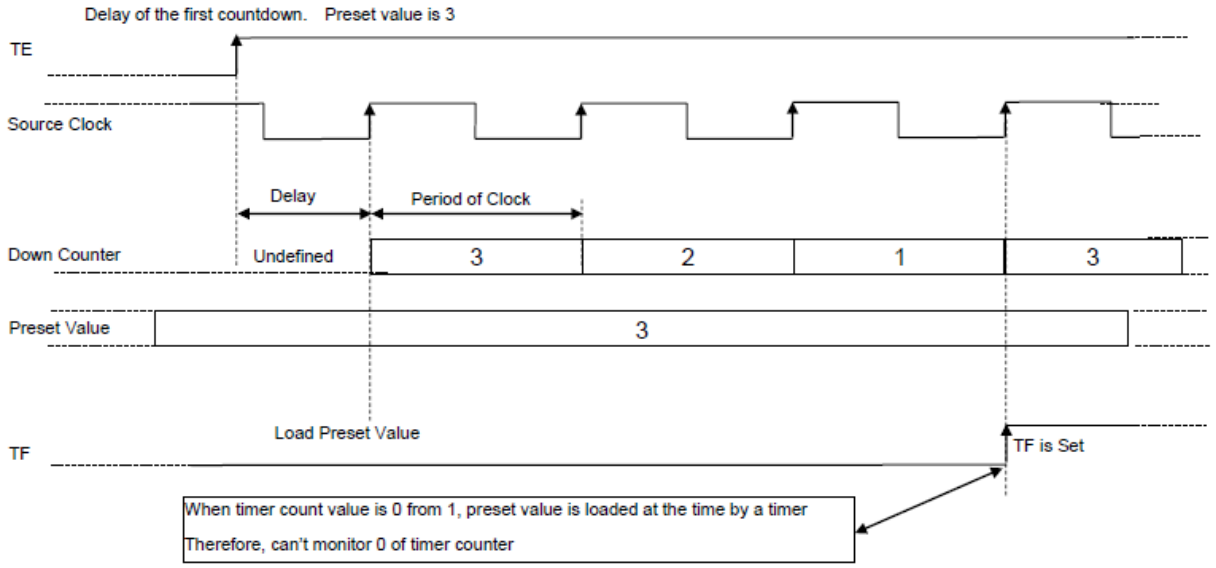
(1) Timer Counter 0, 1, 2 are preset value of timer.
(2) Timer 0, 1, 2 are current count value of timer.
(3) Before entering settings for operations, it is recommended writing a “0” to the TE and TIE bits to prevent unexpected hardware interrupts.
(4) When the RESET bit value is “1” the time update interrupt function does not operate.
(5) When the wakeup timer interrupt function is not using, the wakeup timer counter0, 1, 2 (0Bh, 0Ch, 1Fh), these can be used as a RAM register. In such cases, stop the wakeup timer function by writing “0” to the TE and TIE bits.
(6) When writes 00h to all timer counter, Timer countdown are stop, and new Timer interruption are inhibited.

(1) TSEL0, 1bits (Timer Select 0, 1)

The combination of these two bits is used to set the countdown period source clock for the wakeup timer interrupt function (four settings can be made).

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock / cycle time	Auto reset time tRTN Min.
Write / Read	0	0	4096 Hz / Once per 244.14 μs	122 μs
	0	1	64 Hz / Once per 15.625 ms	7.813 ms
	1	0	*Default Second" update / Once per second	7.813 ms
	1	1	"Minute" update / Once per minute	15.1 ms

(1) tRTN is different with a source clock in automatic release time. TF is not cleared automatically.
(2) Source clock of 1 Hz does not synchronize to update of a second. (It is a 1 Hz clock for timers)
(3) Source clock 1/60 Hz synchronize in update of a minute.
(4) A preset value, it is loaded with the first source clock of a timer counter after having set TE.
(5) Therefore, two periods of source clocks are needed at the maximum till the first countdown starts after TE="1".



(2) TSTP (Timer STOP) bit

This bit controls the temporarily stopped of Timer Counter.

TSTP	Data	Description
Write / Read	0	Count down of the Timer Counter are continued Timer
	1	Counter are stopped. (don't reset)

(3) TRES (Timer Reset) bit

This bit can be employed like Watch Dog Timer function.

TRES	Data	Description
Write / Read	0	The Timer Counter is not affected
	1	Preset value is loaded to all Timer Counters

(4) TE (Timer Enable) bit

This bit controls the start/stop setting for the wakeup timer interrupt function.

TE	Data	Description
	0	Preset value loaded to all Timer counter, and count-down stops

Write / Read	1	Starts wakeup timer countdown ∗ The countdown that starts when the TE bit value changes from 0 to 1 always begins from the preset value

(5) **TF (Timer Flag) bit**

If set to 0 beforehand, this flag bit's value changes from “0” to “1” when a wakeup timer interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	Wakeup timer interrupt events are not detected.
	1	Wakeup timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

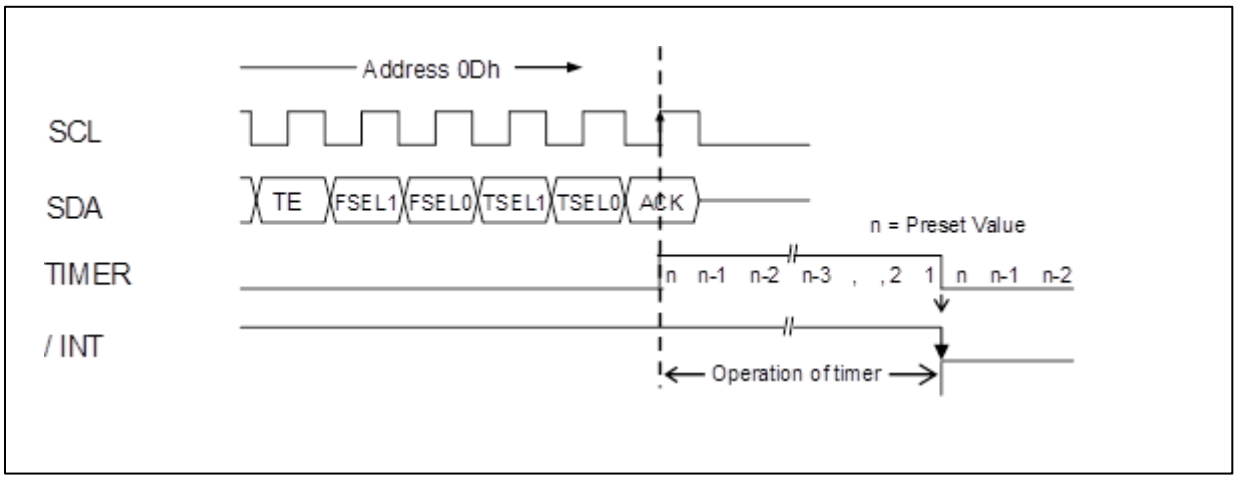
(6) **TIE (Timer Interrupt Enable) bit**

When a wakeup timer interrupt event occurs (when the TF bit value changes from “0” to “1”), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

TIE	Data	Description
Write / Read	0	1) When a wakeup timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z) 2) When a wakeup timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z) ∗ Even when the TIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = L)
	1	When a wakeup timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low) ∗ When a wakeup timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is 1. Earliest 7.813 ms the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

- **Wakeup Timer Start Timing**

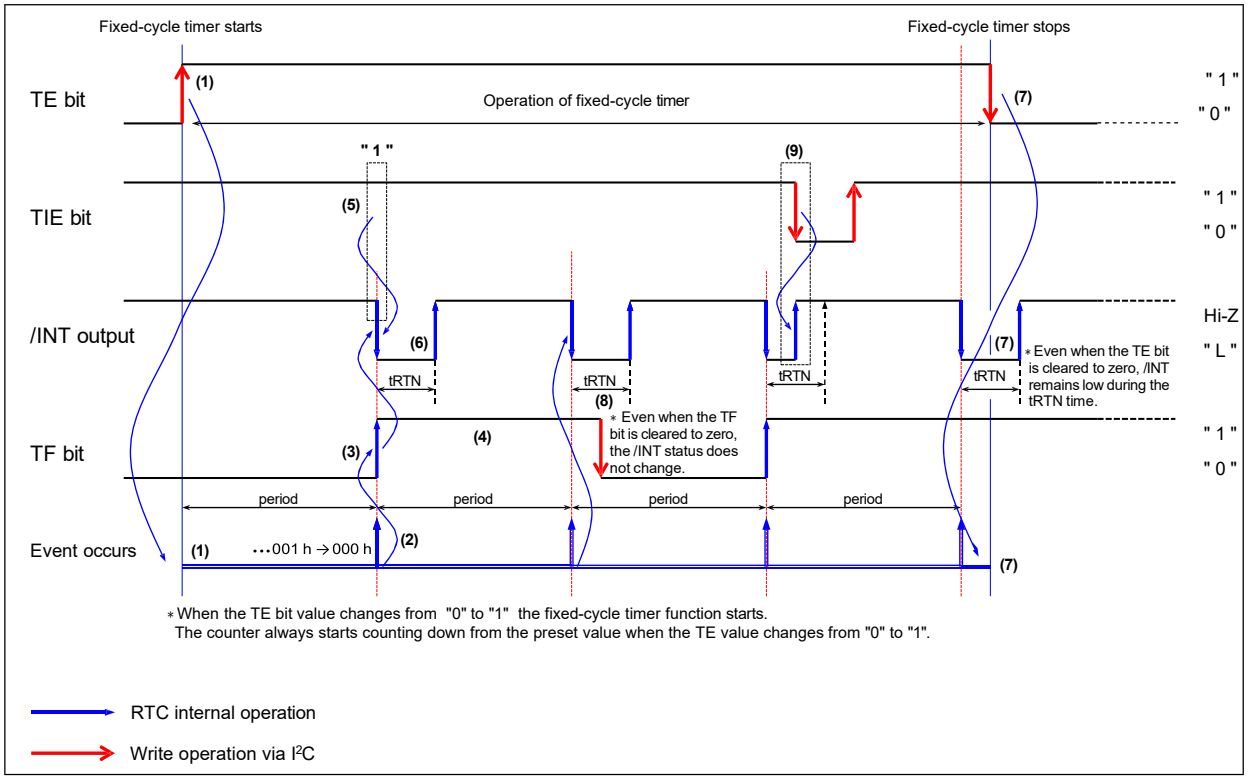
Counting down of the wakeup timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from 0 to “1” (after bit “0” is transferred).



- **Wakeup Timer Interrupt Interval**

Preset Value	Source clock			
	4096 Hz	64 Hz	"Second" update	"Minute" update
	TSEL1,0 = 0,0	TSEL1,0 = 0,1	TSEL1,0 = 1,0	TSEL1,0 = 1,1
0	–	–	–	–
1	244.14 µs	15.625 ms	1 s	1 min
2	488.28 µs	31.25 ms	2 s	2 min
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
4095	0.9998 s	63.984 s	4095 s	4095 min
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
16777215	4096 s	3 days,49 min.4 s	194 days	32 years

- **Wakeup Timer Interrupt Timing Chart**



When a “1” is written to the TE bit, the wakeup timer countdown starts from the preset value.

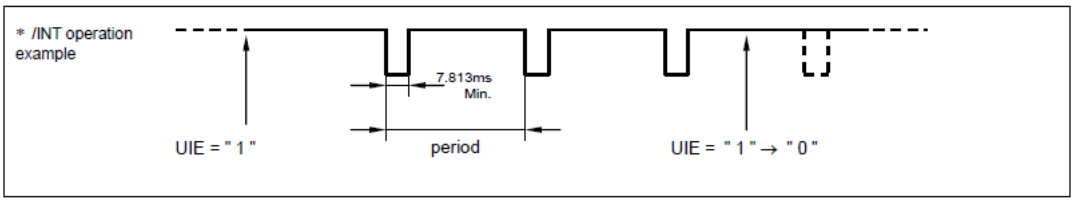
A wakeup timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 01h to 00h, an interrupt event occurs.
After the interrupt event occurs, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)
(1) When a wakeup timer interrupt event occurs, “1” is written to the TF bit.
(2) When the TF bit = “1” its value is retained until it is cleared to zero.
(3) If the TIE bit = 1 when a wakeup timer interrupt occurs, /INT pin output goes low.
If the TIE bit = “0” when a wakeup timer interrupt occurs, /INT pin output remains Hi-Z.
(4) Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
/INT is again set low when the next interrupt event occurs.
(5) When a 0 is written to the TE bit, the wakeup timer function is stopped and the /INT pin is set to Hi-Z status.
When /INT = low, the wakeup timer function is stopped. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.
(6) As long as /INT = low, the /INT pin status does not change when the TF bit value changes from “1” to “0”.
(7) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from “1” to ”0”.

5. Time Update Interrupt Function

● Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.

When an interrupt event occurs, the UF bit value becomes “1” and the /INT pin goes to low level to indicate that an event has occurred. (However, when a wakeup timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is “1”. This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) earliest 7.813 ms (fixed value) after the interrupt occurs.



● Related Registers for Time Update Interrupt

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Control 1	TEST	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
0F	Control 2	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

“ ○ ” indicates write-protected bits. A zero is always read from these bits.

Before entering settings for operations, we recommend writing a “0” to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

When the RESET bit value is 1 time update interrupt events do not occur.

Although the time update interrupt function cannot be fully stopped, if “0” is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

(1) USEL (Update Interrupt Select) bit

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Update interrupts	Auto reset time tRTN
Write / Read	0	second update ＊Default	500 ms
	1	minute update	7.813 ms Min.

(2) UF (Update Flag) bit

Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next detection. In time update interruption, even if UF is cleared, INT is not released.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Time update interrupt events are not detected
	1	Time update interrupt events are detected (The result is retained until this bit is cleared to zero)

(3) UIE (Update Interrupt Enable) bit

When a time update interrupt event occurs (UF bit value changes from “0” to ”1”), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low) or to not generate it (/INT status remains Hi-Z).

UIE	Data	Description
Write / Read	0	● Does not generate an interrupt signal when a time update interrupt event occurs (/INT remains Hi-Z). ● Cancels interrupt signal triggered by time update interrupt event (/INT changes from low to Hi-Z). ● Even when the UIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = L).
	1	● When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). ● When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the UIE bit value is “1”. Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

- **Time Update Interrupt Function Timing Chart**

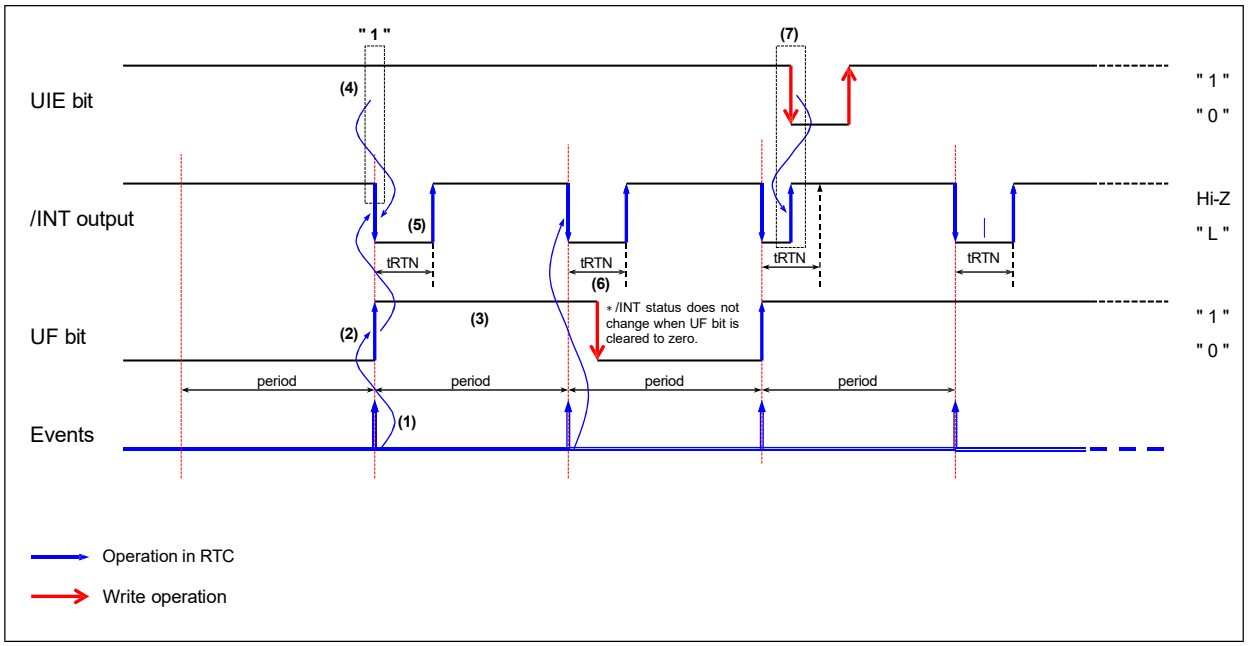


Figure 19 Update Interrupt Timing Chart

(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.
(2) When a time update interrupt event occurs, the UF bit value becomes “1”.
(3) When the UF bit value is “1” its value is retained until it is cleared to zero.
(4) When a time update interrupt occurs, /INT pin output is low if UIE = ”1”. If UIE = ”0” when a timer update interrupt occurs, the /INT pin status remains Hi-Z.
(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.813 ms for time update interrupts) after which it is automatically cleared to Hi-Z. /INT pin output goes low again when the next interrupt event occurs.
(6) As long as /INT = low, the /INT pin status does not change, even if the UF bit value changes from “1” to “0”.
(7) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from “1” to ”0”.

6. Temperature Compensation Function

● Temperature Compensation Function

During the production process of the RTC, we are programming the individual characteristics of the built-in crystal into the non-volatile memory of the RTC. The build-in temperature sensor measures the actual temperature of the module and compensates the oscillation frequency of the crystal oscillator using the stored compensation data. This way not only the time information is temperature compensated, but as well the FOUT signal, even when outputting 32.768 kHz. This function works in the supply voltage range VTEM.

● Related Registers for Temperature Compensation Function

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F	Control 2	**CSEL1**	**CSEL0**	UIE	TIE	AIE	○	○	RESET

(1) CSEL1, CSEL0 (Compensation Interval Select 1, 0) bit

This bit sets an interval of a temperature compensation operation.
Current consumption decreases when increasing the Compensation Interval by means CSEL1, 0. CSEL1, 0 is set at the time of initial power-up to (“0”, “1”).

CSEL0,1	CSEL1	CSEL0	Compensation interval
Write / Read	0	0	0.5 s
	0	1	2.0 s (Default)
	1	0	10 s
	1	1	30 s

Even if the power supply voltage falls below V_{TEM} and a VDET bit is set to “1”, the temperature compensation operation is performed again if the supply voltage raises above V_{TEM}.

7. Device ID

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
20	Device ID	Do not to write								00h	R

8. Backup Function 1

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
18	Backup Function 1	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	00h	R/W

After power on reset, VDETOFF=0, SWOFF= 0, BKSMP0=0, BKSMP1=0 are set as default value. So 1sec after power on reset, VDD voltage is detected and goes to Normal Mode (VDET3 < VDD) or Backup Mode (VDD ≦ VDET3).
The duration of VDD voltage detection is controlled by means of BKSMP0-bit, BKSMP1-bit and can be set to be 2msec, 16msec, 128sec or 256msec. VDD voltage is detected at the end of this time, so at the falling edge of the comparator ON signal.
SWOFF (SwitchOFF): The software control bit for the switch K1 between Voo and the kernel power Vcore. The default value is 0, 1 - switch off, O - switch on.

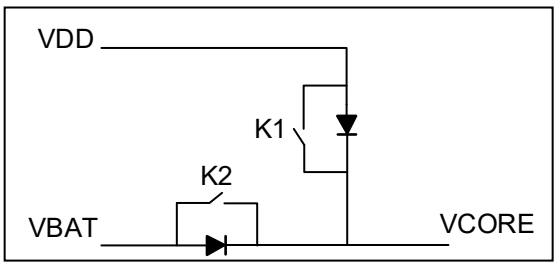
VDD detector	VDET OFF	SW OFF	BKSMP1	BKSMP0	VDET3 Samplingperiod	Pch-Switch ON/OFF	Remarks
ON	0	X	0	0	2ms	2ms OFF	VDETOFF:0,BKSMP1:0, BKSMP0:0 default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256ms OFF	
OFF	1	0	X	X	OFF	ON	VDD and Vcore short circuit via Pch- switch
		1	X	X	OFF	OFF	VDD connected via diode to Vcore

X = Don't care.

9. Backup Function 2

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	int	R/W
21	Backup Function 2	○	○	○	○	○	VBATSW	○	○	00h	R/W

(1) A built-in P-ch switch located between the internal power supply of the chip VCORE and the backup power supply pin "VBAT".
(2) VBATSW: Battery power switch K2 software control bit： 0 - switch on, 1 - switch off. The default state is 0.
(3) VBATSW=0：VCORE and VBAT short circuit via Pch- switch.
(4) VBATSW=1：VCORE connected via diode to VBAT



10. Frequency offset

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	int	R/W
25	Frequency offset Ctrol1	○	○	○	○	○	○	offset step 1	offset step 0	00h	R/W
26	Frequency offset Ctrol2	enable offset 1	enable offset 0	F5	F4	F3	F2	F1	F0	00h	R/W

- **Adjustment range**

Frequency offset		Default
enable/disable Frequency offset		
enable offset 1, enable offset 0=00/01/10	disable Freq offset	√
enable offset 1, enable offset 0=11	enable Freq offset	
Frequency offset step		
offset step 1, offset step 0=00/01/10	default step=0.2x10^{-6}	√
offset step 1, offset step 0=11	double accuracy, step=0.1x10^{-6}	

- **Adjustment amount and adjustment value**

0x26 F5~F0 data bits，offset step 1, offset step 0=00/01/10

ofst<5:0>	Freq	ofst<5:0>	Freq
00 0000	0ppm	11 1111	+0.2ppm
00 0001	-0.2ppm	11 1110	+0.4ppm
00 0010	-0.4ppm	11 1101	+0.6ppm
...	...	...	...
01 1111	-6.4ppm	10 0000	+6.4ppm

0x26 F5~F0 data bits，offset step 1, offset step 0=11

ofst<5:0>	Freq	ofst<5:0>	Freq
00 0000	0ppm	11 1111	+0.1ppm
00 0001	-0.1ppm	11 1110	+0.2ppm
00 0010	-0.2ppm	11 1101	+0.3ppm
...	...	...	...
01 1111	-3.2ppm	10 0000	+3.2ppm

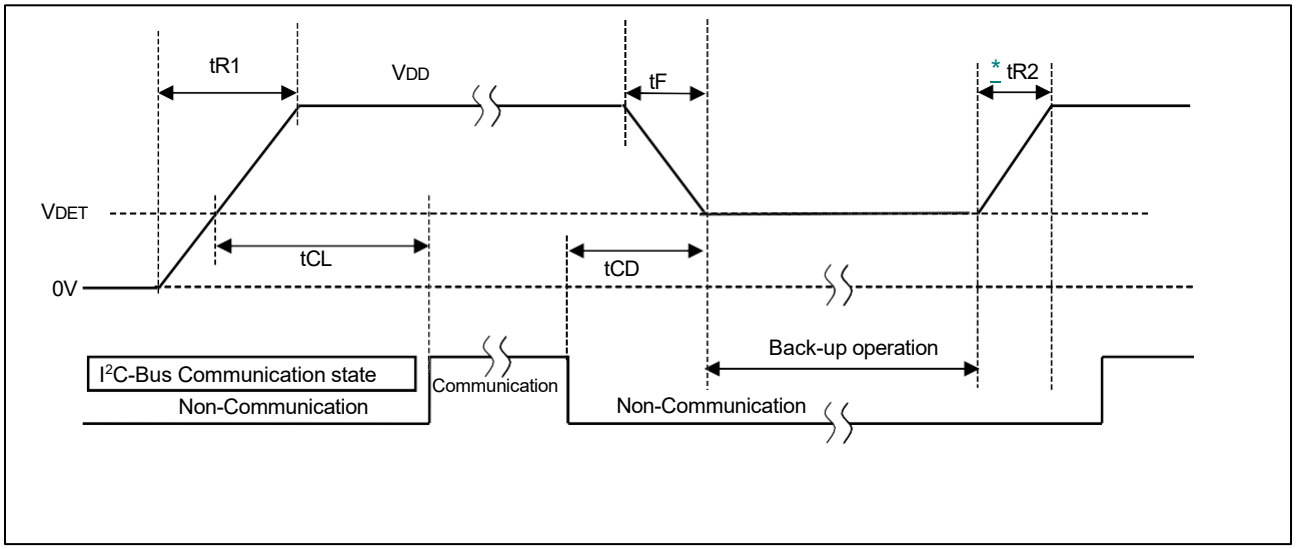
Note:
The Frequency offset register affects the frequency stability. Please be careful if you adjust it.
The offset function is effective for frequency adjustment at the normal temperature.
The single adjustment amount of 0.2ppm is approximate value.

11. Sub SEC

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	int	R/W
27	Sub SEC 0	Sub SEC[7:0]									R
28	Sub SEC 1	Reserved						Sub SEC[9:8]			R

Sub SEC[9:0] step=1/1024s

Backup and Recovery



(1) This circuit is sensitive to power supply noise and supply voltage should be stabilized to avoid negative impact on the accuracy.
(2) tR1 is needed for a proper power-on reset. If this power-on condition cannot be kept, it is necessary to send an initialization routine to the RTC by software.
(3) In case of repeated ON / OFF of the power supply within short term, it is possible that the power-on reset becomes unstable.
(4) After power-OFF, keep V_{DD} = GND for more than 10 seconds for a proper power-on reset. When it is impossible, please initialize the RTC by the software.
(5) As for the communication of I2C-Bus, completion of less than 1 second is recommended.
(6) If such communication requires 2 seconds (Max.) or longer, the I2C-Bus interface is reset by the internal bus timeout function.
(7) tR2 is specifications for an oscillation not to stop. Some clocks are not output by an FOUT terminal.
(8) When bus-time-out occur, SDA turns to Hi-Z input mode. readout data of a clock is stable anytime, and there isn't contradiction.
(9) And it does not occur that data of a clock delay even if access time is prolonged.

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Power supply rise time1	tR1	VDD = VSS ~ 5.5 V	1		10	ms / V
Access wait time (after initial power on)	tCL	After VDD = VDET	30			ms
Power supply fall time	tF	VDD = 5.5 V ~ VDET	100			µs / V
Power supply rise time	tR2	VDD = VDET ~ 5.5 V	15			µs / V
Setup time from finish of I2C-Bus	tCD	Before VDD = VDET	0			µs

- **About Access at the Time of Backup Return and Initial Power Supply**

(1) Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized. Please initialize the RTC at the time the power supply voltage returns (VLF = 1) after the oscillation has stabilized (after oscillation start time tSTA).

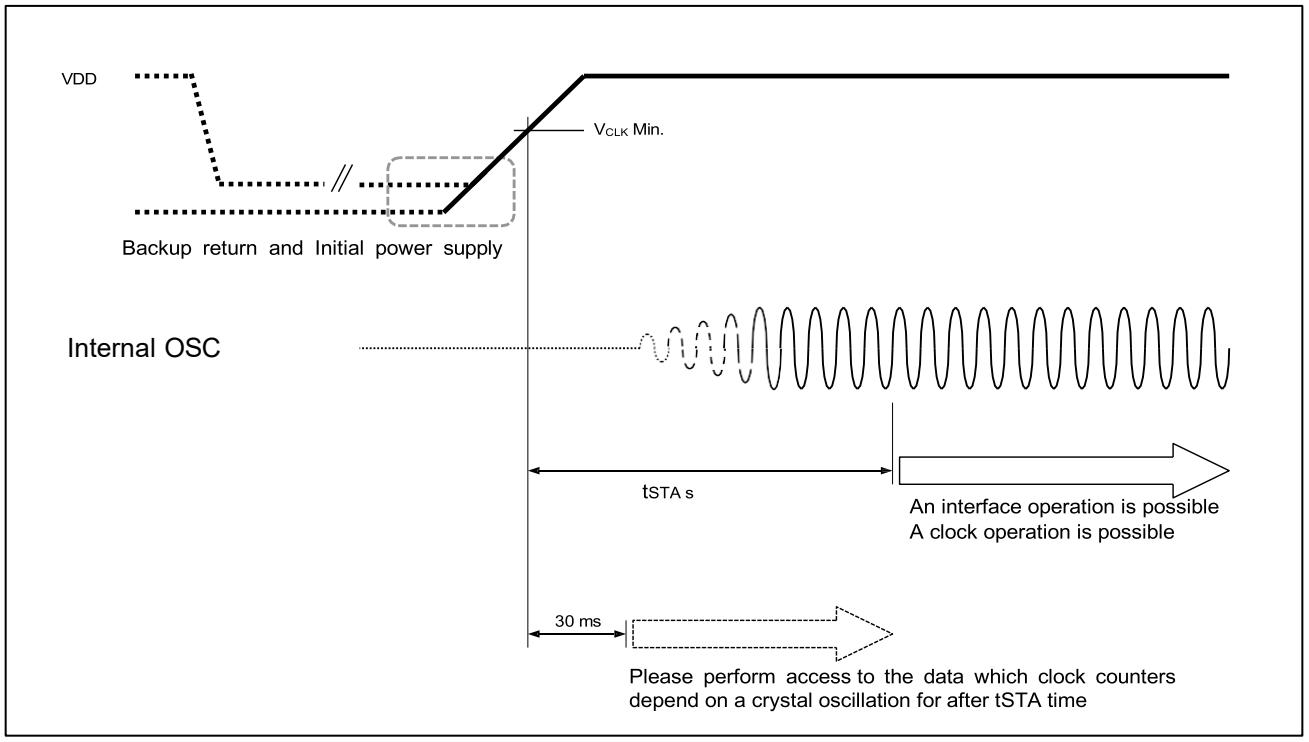
(2) If intending to access the RTC after the main supply voltage returns, please note following points: Please begin to read VLF-bit first.

(3) If VLF-bit returns “1”, please initialize all registers. Please perform initial setting only tSTA (oscillation start time), when the

(4) built-in oscillation is stable.

(5) Access is prohibited about 30 ms, from the VCLK voltage. VCLK (clock supply voltage (V_{DD} >1.5 V). If VLF-bit returns “0”, access is possible without waiting time.

(6) Before the internal crystal oscillator has stabilized (tSTA), no clock operation is possible, and time is not counted.



I2C-Bus Interface

● Overview

The I2C-Bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.

The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.

The I2C-Bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.
Slave addresses have a fixed length of 7 bits. The slave address is [**0110010**].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	R/W
0	1	1	0	0	1	0	1 = Read
							0 = Write

● System Configuration

All ports connected to the I2C-Bus must be either open drain or open collector ports in order to enable “AND- connections” to multiple devices.

SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

Any device that controls the data transmission and data reception is defined as a “Master”. And any device that is controlled by a master device is defined as a “Slave”.

The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a “receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

● Read mode

In this mode, the master reads the slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the

master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

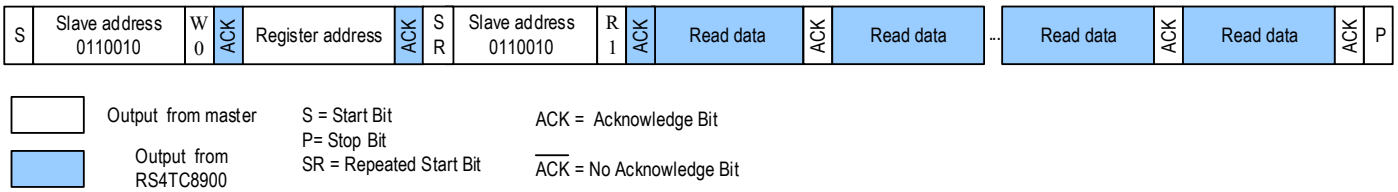


Figure 6 Read Mode Sequence

- **Write mode**

In this mode the master transmitter transmits to the slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

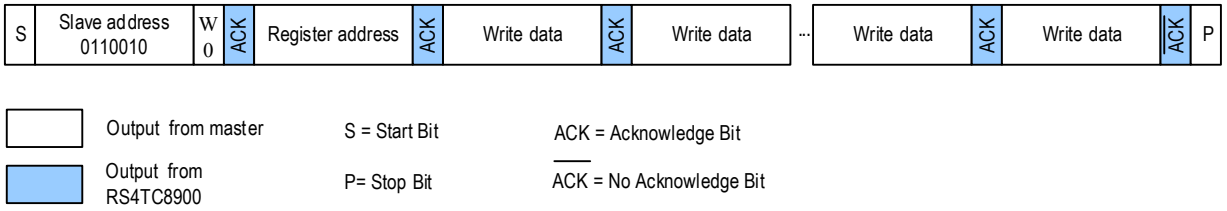
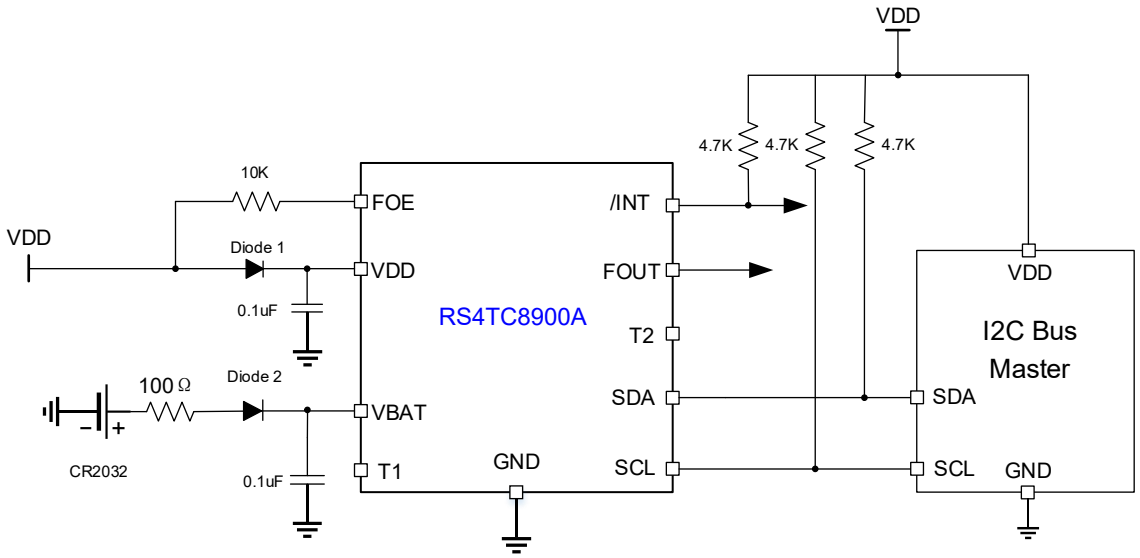


Figure 7 Write Mode Sequence

Application Circuit



Note 1: **Pull-up resistor connections for SCL、SDA and /INT**

(1) SCL、SDA and /INT Connect to the system-power supply.

(2) Install 2 bypass condensers in nearest position of a limit to pin of both VDD and VBAT.

Note 2: Use a non-rechargeable battery or rechargeable battery

(1) When using a non-rechargeable battery, be sure to use a diode. Contact the battery manufacturer for details regarding applied resistance values.

(2) A diode is not required when using a rechargeable battery

Note 3: Diodes K1 and K2 inside the chip can respectively replace Diode1 and Diode2

(1) This means that when the backup power source is a non-rechargeable battery, 0x21 can be set to 04 and Diode2 should be removed.

(2) When the backup power source is a rechargeable battery, 0x21 can be set to 00 and Diode2 should be removed.

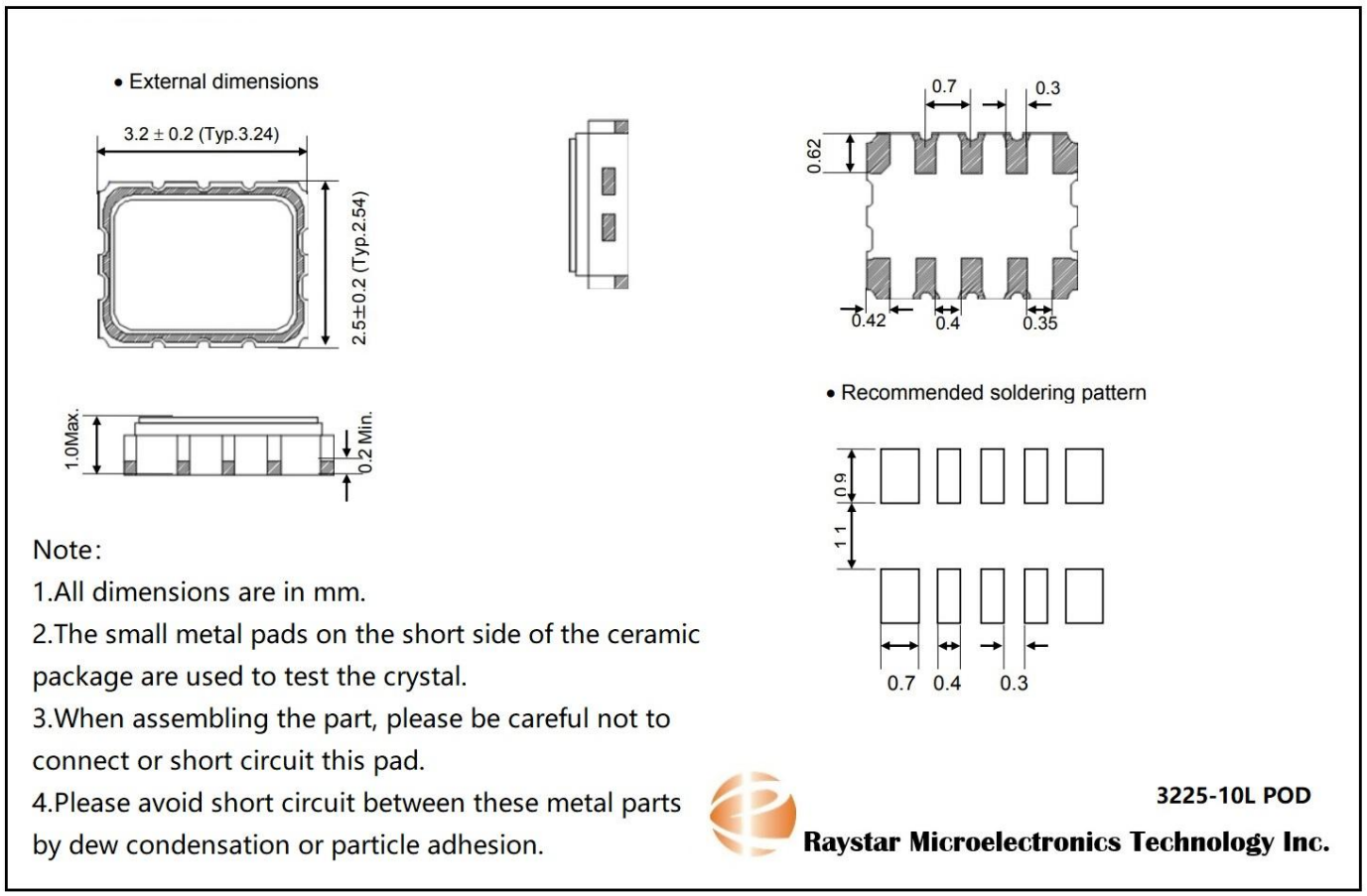
(3) The default value of 0x21 is 00.

Note 4: Applications with VDD voltage lower than 2.5V

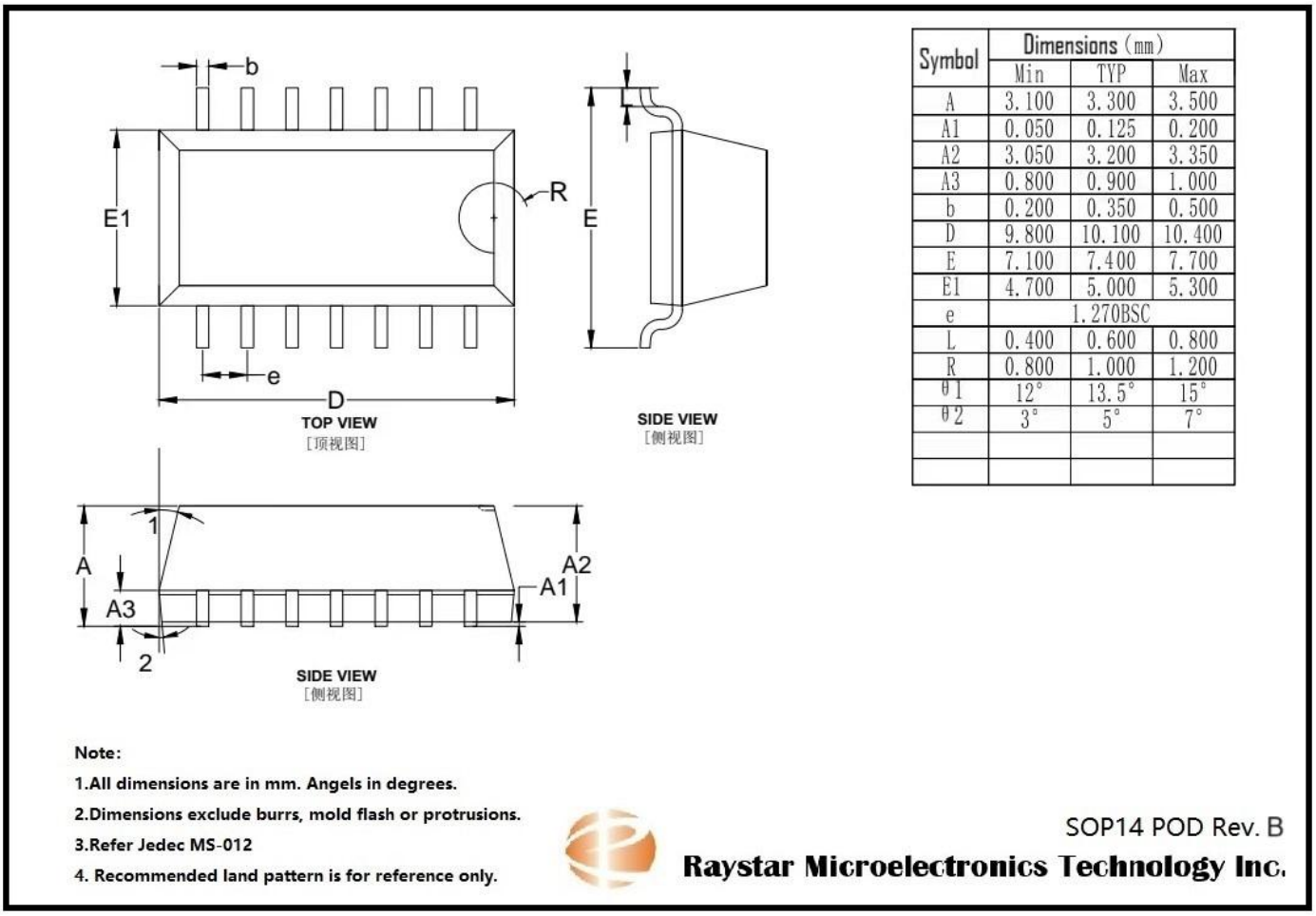
(1) When the VDD voltage is less than 2.5V (for example, when VDD = 1.8V is used), VDD should be connected to VBAT, or set 0x18 = 08, and add Diode1.

Package Information

3225 -10 pin



SOP-14



Symbol	Dimensions (mm)		
	Min	TYP	Max
A	3.100	3.300	3.500
A1	0.050	0.125	0.200
A2	3.050	3.200	3.350
A3	0.800	0.900	1.000
b	0.200	0.350	0.500
D	9.800	10.100	10.400
E	7.100	7.400	7.700
E1	4.700	5.000	5.300
e	1.270BSC		
L	0.400	0.600	0.800
R	0.800	1.000	1.200
θ1	12°	13.5°	15°
θ2	3°	5°	7°

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP14 POD Rev. B

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary	2025/09/30
1.0	Initial Release	2025/12/15