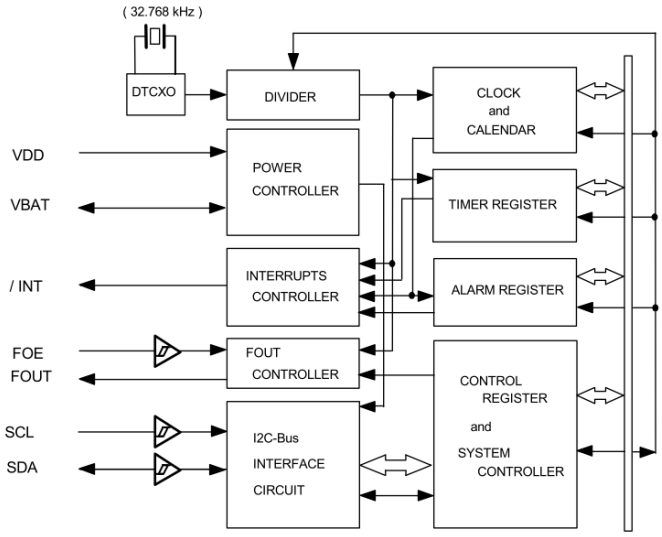
Features

- Built-in 32.768 kHz DTCXO
- High Stability:
  ±3.0 ppm / -40 to +85℃
  ±5 ppm / +85 to +105℃
- Supports I2C-Bus's high-speed mode (Up to 400 kHz)
- Alarm interrupt function for day, date, hour, and minute settings
- Wakeup timer interruption
- Time update interrupt function for Seconds, minutes
- Temperature compensated 32.768 kHz output with OE function (FOE and FOUT pins)
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 2.5V ~ 5.5V
- Wide time-keeping voltage range:1.6V~ 5.5V
- Low current consumption: 0.54uA / 3 V (Typ.)
- Built-in Backup switchover circuit (trickle charge)
- AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
- Grade 2 temperature range (- 40℃ ~ +105 ℃)

Block Diagram



Description

This module is an I2C bus interface-compliant real time clock which includes a 32.768 kHz DTCXO.

In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, Wakeup timer function, time update interrupt function, and 32.768 kHz output function.

By the battery backup switchover function and the interface power supply input pin, RS4TC8900Q can support various power supply circuitries.

The devices in this module are fabricated via a CMOS process for low current consumption, which enables long-term battery back-up.

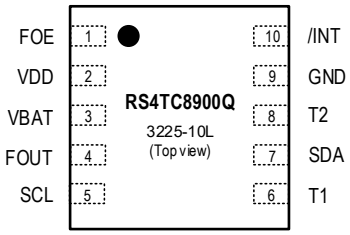
RS4TC8900Q is suitable for automotive applications requiring specific change control.

Package and Ordering Information

Part Number	Package	Description	Δf / f Frequency stability				Unit
			Condition	MIN	TYP	MAX	
RS4TC8900QCE	3225-10L	3.2mmX2.5mm	Ta= -40 to +85℃, VDD=3.0 V Ta= 85℃ to +105℃, VDD=3.0 V	-3 -5		3 5	ppm
RS4TC8900QCE-B	3225-10L	3.2mmX2.5mm	Ta= -40 to +85℃, VDD=3.0 V Ta= 85 to +105℃, VDD=3.0 V	-5 -10		5 10	
RS4TC8900QCE-C	3225-10L	3.2mmX2.5mm	Ta= -40 to +85℃, VDD=3.0 V Ta= 85 to +105℃, VDD=3.0 V	-5 -20		-5 20	
RS4TC8900QCE-F	3225-10L	3.2mmX2.5mm	Ta= 0 to +50℃, VDD=3.0 V Ta= -40~0℃,50 to +105℃, VDD=3.0 V	-5 -30		5 30	

Notes:
[1] E = Pb-free and Green

Pin Configuration



Pin Name	Pin No.	Type	Description
FOE	1	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
VDD	2	Power	This pin is connected to a positive power supply.
VBAT	3	Power	This is the power supply pin for backup battery. Connect this pin to a large-capacity capacitor, a secondary battery or similar. When the battery switchover function is not needed, VBAT must be connected to VDD.
FOUT	4	Output	This is the CMOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
SCL	5	Input	This is the serial clock input pin for I2C Bus communications.
T1	6	Input	Only used by the manufacturer for testing.
SDA	7	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I2C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull- up resistance relative to the signal line capacity.
T2	8	Input	Used by the manufacturer for testing. (Do not connect externally.)
GND	9	Power	Ground of Power
/INT	10	Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	−55	-	125	°C
V_{DD}	Operating supply voltage	-0.3	-	6.5	V
V_{BAT}	Battery Supply voltage	-0.3	-	6.5	V
V_I	Input Voltage on FOE,SCL,SDA	GND-0.3	-	6.5	V
V_{O1}	Output Voltage on FOUT	GND-0.3		VDD+0.3	V
V_{O2}	Output Voltage on SDA and /INT	GND-0.3		6.5	V
LU	Latch-Up			±200	mA
CDM	Charged Device Model			1000	V
HBM	Human Body Model			4000	V

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	Operating supply voltage in normal mode	2.5	3.0	5.5	V
V_{BAT}	Backup power supply voltage	1.6	3.0	5.5	V
V_{TEM}	Temp. compensation voltage	2.0	3.0	5.5	V
T_{OPR}	Operating temperature	-40		105	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 105℃.

Symbol	Parameter	Condition		MIN	TYP	MAX	Unit
I_{DD1}	Average Current consumption (1)	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND, V_{DD} = V_{BAT} FOUT : output OFF (High Z) Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		0.59	3.8	µA
I_{DD2}	Average Current consumption (2)		V_{DD} = 3 V		0.54	3.6	
I_{DD3}	Average Current consumption (3)	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = V_{DD}, V_{DD} = V_{BAT} FOUT :32.768 kHz, CL =0pF Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		1.60	5.3	µA
I_{DD4}	Average Current consumption (4)		V_{DD} = 3 V		1.15	4.5	
V_{IH}	High-level input voltage	SCL, SDA, FOE pins		0.8 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage	SCL, SDA, FOE pins		GND – 0.3		0.2 × V_{DD}	V
V_{OH1}	High-level output voltage	FOUT pin	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
V_{OH2}			V_{DD}=3 V, I_{OH}=–1 mA	2.2		3.0	
V_{OH3}			V_{DD}=3 V, I_{OH}=–100 µA	2.9		3.0	
V_{OL1}	Low-level output voltage	FOUT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.5	V
V_{OL2}			V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.8	
V_{OL3}			V_{DD}=3 V, I_{OL}=100 µA	GND		GND+0.1	
V_{OL4}		/ INT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
V_{OL5}			V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.4	
V_{OL6}		SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
I_{LK}	Input leakage current	FOE, SCL, SDA pins, V_{IN} = V_{DD} or GND		–0.5		0.5	µA
I_{OZ}	Output leakage current	/ INT, SDA, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	µA

AC Characteristics - Frequency

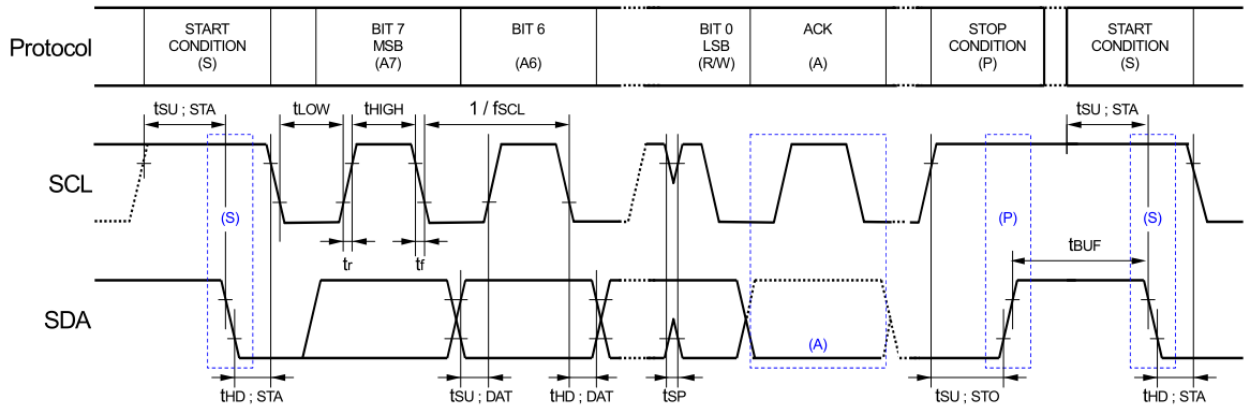
Unless otherwise specified, -40°C≤T_A≤ 105℃.

Symbol	Paramater	Suffix	Condition	MIN	TYP	MAX	Unit
Δf / f	Frequency stability		Ta= -40 to +85℃, VDD=3.0 V Ta= 85 to +105℃, VDD=3.0 V	-3.0 -5		3.0 5	ppm
		B	Ta= -40 to +85℃, VDD=3.0 V Ta= 85 to +105℃, VDD=3.0 V	-5 -10		5 10	
		C	Ta= -40 to +85℃, VDD=3.0 V Ta= 85 to +105℃, VDD=3.0 V	-5 -20		-5 20	
		F	Ta= 0 to +50℃, VDD=3.0 V Ta= -40~0℃， 50 to +105℃, VDD=3.0 V	-5 -30		5 30	
f / V	Frequency/voltage characteristics		Ta= +25℃ , VDD=2.0 V to 5.5 V	-1.0		1.0	ppm
tSTA	Oscillation start time		Ta= +25℃, VDD=1.6 V to 5.5 V			1.0	s
			Ta= -40 to +105℃, VDD=1.6 V to 5.5 V			3.0	
fa	Aging		Ta= +25℃ , VDD=3.0 V, first year	-3.0		3.0	ppm
Tsensor	Temperature Sensor Accuracy		VDD=3.0 V	-4.0		4.0	℃
Duty	FOUT duty		50% of VDD level	40	50	60	%

AC Characteristics – I2C Bus

Unless otherwise specified, -40°C≤T_A≤ 105℃.

Symbol	Paramater	Condition	MIN	TYP	MAX	Unit
f_{SCL}	SCL clock frequency	Fast mode			400	kHz
$t_{SU;STA}$	Start condition setup time	Fast mode	0.6			μs
$t_{HD;STA}$	Start condition hold time	Fast mode	0.6			μs
$t_{SU;DAT}$	Data setup time	Fast mode	100			ns
$t_{HD;DAT}$	Data hold time	Fast mode	0			ns
$t_{SU;STO}$	Stop condition setup time	Fast mode	0.6			μs
t_{BUF}	Bus idle time between start condition and stop condition	Fast mode	1.3			μs
t_{LOW}	Time when SCL = "L"	Fast mode	1.3			μs
t_{HIGH}	Time when SCL = "H"	Fast mode	0.6			μs
t_r	Rise time for SCL and SDA	Fast mode			0.3	μs
t_f	Fall time for SCL and SDA	Fast mode			0.3	μs
t_{SP}	Allowable spike time on bus	Fast mode			50	ns



Register Table

Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00 or 10	SEC	○	40	20	10	8	4	2	1	R/W
01 or 11	MIN	○	40	20	10	8	4	2	1	R/W
02 or 12	HOUR	○	○	20	10	8	4	2	1	R/W
03 or 13	WEEK	○	6	5	4	3	2	1	0	R/W
04 or 14	DAY	○	○	20	10	8	4	2	1	R/W
05 or 15	MONTH	○	○	○	10	8	4	2	1	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W
07	RAM	●	●	●	●	●	●	●	●	R/W
08	MIN Alarm	AE	40	20	10	8	4	2	1	R/W
09	HOUR Alarm	AE	●	20	10	8	4	2	1	R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	20	10	8	4	2	1	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	R/W
0E or 1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	R/W

Note:

1. After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.

Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

2. During the initial power-up, the following are the default settings for the register values
   Initial value_0 :
   TEST,WADA,USEL,TE,FSEL1,FSEL0,TSEL0,UF,TF,AF,CSEL1,UIE,TIE,AIE,RESETVDETOFF,SWOFF,BKSMP1,BKSMP0
   Initial value_1 :
   TSEL1,VLF,VDET,CSEL0
   At this point, all other register values are undefined, so be sure to perform a reset before using the module.
3. Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.
4. Any bit marked with "○" should be used with a value of "0" after initialization.
5. Any bit marked with "●" is a RAM bit that can be used to read or write any data.
6. The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.
7. If an alarm function is not used, registers 08h-0Ah can be used as RAM. (AIE : "0")
8. Reading register value of address 0Bh-0Ch is pre-set data.
9. If a timer function is not used, register of 0Bh-0Ch can be used as RAM. (TE,TIE : "0")

Temperature Data, Backup power supply control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17	TEMP	128	64	32	16	8	4	2	1	READ
18	Backup Function	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	R/W
19	Not use	○	○	○	○	○	○	○	○	READ
1A	Not use	○	○	○	○	○	○	○	○	READ

The temperature data are updated during operation of the temperature compensation circuit.

Details of Registers

Clock counter (SEC - HOUR)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00 or 10	SEC	○	40	20	10	8	4	2	1	R/W
01 or 11	MIN	○	40	20	10	8	4	2	1	R/W
02 or 12	HOUR	○	○	20	10	8	4	2	1	R/W

Note:
1. "○" indicates write-protected bits. A zero is always read from these bits.
2. The clock counter counts seconds, minutes, and hours.
3. The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.
4. Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

Second counter

This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.

Minute counter

This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

Hour counter

This hour counter counts from "00" hours to "01," "02," and up to 23 hours, after which it starts again from 00 hours.

Calendar counter (WEEK - YEAR)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
03 or 13	WEEK	○	6	5	4	3	2	1	0	R/W

Day of the WEEK counter
The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
The day data values are counted as follows: Day 01h , Day 02h ,Day 04h ,Day 08h ,Day 10h ,Day 20h Day 40h ,Day 01h, Day 02h, etc.

Week	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Date counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
04 or 14	DAY	○	○	20	10	8	4	2	1	R/W

The updating of dates by the date counter varies according to the month setting.
A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

Month	Date update pattern
1, 3, 5, 7, 8, 10, or 12	1～31
4, 6, 9, or 11	1～30
February in normal year	1～28
February in leap year	1～29

Month counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
05 or 15	MONTH	○	○	○	10	8	4	2	1	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W

The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

Year counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W

The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.
Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
08	MIN Alarm	AE	40	20	10	8	4	2	1	R/W
09	HOUR Alarm	AE	○	20	10	8	4	2	1	R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		○	20	10	8	4	2	1	R/W

The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and "1" is set to the AF bit to report that an alarm interrupt event has occurred.

Note: AE-bit is low active, so in order to enable 1 interrupt every hour once the actual minutes match the alarm setting, it is necessary to set the AE of register 08h to 0 and the AE of 09h and 0Ah to 1.
In order to generate an alarm interrupt only once a week, all 3 AE-bits have to be set “0
∗1) The alarm function is not a HW feature but software function inside the RTC!
*2) In case “AE” bit of register 0Ah is set to "1", the day will be ignored and an interrupt occurs ones the actual time matches the minutes and/or hour setting of the alarm register.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 0Ah):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets. As a result, alarm occurs if only the hour and minute values match the alarm data.
∗3) If all three AE bit values are "1" the week/date and time settings are ignored, and an alarm interrupt event will occur once per

minute.

Fixed-cycle timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	○	○	○	○	2048	1024	512	256	R/W

Note:
These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function. The TE, TF, TIE, and TSEL0/1 bits are also used to set the fixed-cycle timer interrupt function.
When fixed-cycle timer interrupt event has occurred, the /INT pin goes to low level and "1" is set to the TF bit .

Extension registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	○	○	○	○	2048	1024	512	256	R/W
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	R/W

Note:
1. The default value is the value that is read (or is set internally) after powering up from 0 V
2. "0" mandatory" 0" Make sure to always write 0 into this bit.
3. "-" indicates a default value is undefined.

This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

TEST bit

This is the manufacturer's test bit. Its value should always be "0". Be careful to avoid writing a "1" to this bit when writing to other bits.

TEST	Data	Description
Write/Read	0	Normal operation mode (Default)
	1	Setting prohibited (manufacturer's test bit)

WADA (Week Alarm/Day Alarm) bit

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies a DAY alarm, meaning the alarm interrupt is initiated independent of the actual day when the set time is reached.
Writing a "0" to this bit specifies a WEEK alarm, so an alarm interrupt is only generated when the set time is reached on a dedicated day of a week.

USEL (Update Interrupt Select) bit

This bit is used to define if the RTC should output a "second update" or "minute update" interrupt, allowing to synchronize external clocks with the time registers of the RTC.

USEL	Data	update interrupts	Auto reset time tRTN
Write/Read	0	second update（Default）	500 ms
	1	minute update	Min. 7.813 ms

TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a "1" to this bit specifies starting of the fixed-cycle timer interrupt function (a countdown starts from a preset value).
Writing a "0" to this bit specifies stopping of the fixed-cycle timer interrupt function.

FSEL0,1 (FOUT frequency Select 0, 1) bits

The combination of these two bits is used to set the FOUT frequency. Note: All frequencies are temperature compensated

FSEL1	FSEL0	FOUT
0	0	32768Hz
0	1	1024Hz
1	0	1Hz
1	1	32768

TSEL0,1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function.

TSEL1	TSEL0	Timer		Auto reset time tRTN (Min.)	Effect of RESET bit
0	0	4096 Hz	Once per 244.14 μs	122 us	——
0	1	64 Hz	Once per 15.625 ms	7.813 ms	Does not operate when the RESET bit value is "1".
1	0	"Second" update	Once per second	7.813 ms	
1	1	"Minute" update	Once per minute	7.813 ms	

Flag register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0E or 1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W

Default is values loaded automatically after power ON from 0V.
"o" indicates write-protected bits. A zero is always read from these bits.
"-" indicates a default value is undefined.

UF (Update Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a time update interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

TF (Timer Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

AF (Alarm Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to 1" when an alarm interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

VLF (Voltage Low Flag) bit

VLF indicates the retained reliability of clock functions and internal data.
When VLF was set to "1", it indicates possibility that was lost of both memorized data and clock calendar data. The factor of VLF are 2 kinds.

1. Supply voltage drop less than 1.6V(VCLK) was detected. VLF-voltage-detector is active in anytime. Detection velocity is about 1ms to 10ms.
2. The internal crystal oscillation was stopped. This detector is active in anytime. Detection velocity is about 100ms.

Once VLF value was set to "1", its "1" is retained until a "0" is written to it. After initial power ON from 0 V, make sure VLF was set to "1".

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	No supply voltage drop occurred, so data are not compromised.
	1	Low voltage has been detected, so data loss might have occurred, and time information might be compromised. All registers must be initialized. (This setting is retained until a "zero" is written to this bit.)

VDET (Voltage Detection Flag) bit

VDET indicates the retained reliability of temperature compensation.
When VET was set to "1", it indicates possibility that was lost of clock stability history. The factor of VDET. Supply voltage drop less than 1.95V(VDET) was detected.
VDET is detected in every temperature compensation timing. Detection velocity is about 1ms to 10ms.
Once VDET value is "1", VDET is retained until a "0" is written to it.
After powering up from 0 V, make sure to set this bit's value to "1".

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Temperature compensation is normal.
	1	Temperature compensation has been stopped.

Control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	R/W

Notes
1. The default value is the value that is read (or is set internally) after powering up from 0 V.
2. "o" indicates write-protected bits. A zero is always read from these bits.
3. "-" indicates no default value has been defined.

This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

CSEL0,1 (Compensation interval Select 0, 1) bits

The combination of these two bits is used to set the temperature compensation interval.

CSEL1	CSEL0	Compensation Interval
0	0	0.5s
0	1	2.0s (default)
1	0	10s
1	1	30s

UIE (Update Interrupt Enable) bit

When a time update interrupt event is generated (when the UF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs

UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is notgenerated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated(/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared(/INT status changes from low to Hi-Z) earliest 7.813 ms after the interrupt occurs.

TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z). When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is notgenerated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal isgenerated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pinoccurs only when the value of the control register's TIE bit is "1". Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi- Z).

AIE (Alarm Interrupt Enable) bit

When an alarm timer interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generatedor is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated(/INT status changes from Hi-Z to low). * When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is "1". This setting is retained until the AFbit value is cleared to zero. (No automatic cancellation)

RESET bit

RESET bit was prepared for the synchronized starting of time or timer. The detailed function of reset.

For example.
S is start condition. P is stop condition. RS is re-start condition.
S---Slave address(w)---ACK1---0Fh---ACK2---01h---ACK3---RS---R/W access---P.
RESET-bit is set at ACK3, but RESET doesn't execute.
after set of RESET, RESET-function executes momentarily at next P, and RESET-bit clears automatically.
RESET area of circuit is the count-down-chain of 2Hz from 16kHz, are cleared.
Next update timing of a Seconds counter from RESET. That range is 1000ms-30.5 μs from just 1000ms.
RESET affects to time update interruption, alarm, and timer.

Note:
RESET is not released by the reception of a RE-START condition before receiving a STOP condition. Unnecessary use of RESET will be the cause of delay error of Calendar and Clock.

Temperature Data register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17	TEMP	128	64	32	16	8	4	2	1	READ

Notes:
1. This register can be used to read digital temperature data.
2. The temperature data are updated during operation of the temperature compensation circuit.
3. You can make a conversion to a centigrade by temperature data by calculating in the following expression.

Backup power supply control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
18	Backup Function	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	R/W

This register controls the functionality of the power switchover and backup function.

VDETOFF bit (Voltage Detector OFF)

This bit controls the voltage detection circuit of the main power supply VDD.

SWOFF bit (Switch OFF)

This bit controls the internal P-MOS switch for preventing back flow between v_{core} and VBAT.

BKSMP1, BKSMP0 bit (Backup mode Sampling time)

These bits control the operation time when to be intermittently driven the VDD voltage detection.

SW2OFF bit (Switch OFF)

This bit controls the internal P-MOS switch for preventing back flow from VBAT.

The power switchover control.

To enable the battery backup switchover function, the voltage comparator (VDD Detector) should be activated by means of the VDETOFF bit. If VDETOFF=0, the power switchover function is activated and in case VDETOFF=1 this function is OFF.
In case the power switchover function is activated, the internal COMPEN signal is generated 62.5msec after the second counter incremented and thus the voltage comparator becomes active.

The comparator active period (VDD measurement period) is controlled through BKSMP0, BKSMP1 bits. There are two modes, VDET3 < VDD (Normal Mode), VDD ≤ VDET3 (Backup Mode).

Normal Mode

VDD voltage is detected every one second.
Comparator function intermittently ON, Pch-Switch intermittently OFF
In case of VDD ≤VDET3, it moves to Backup Mode.

Backup Mode

VDD voltage is detected every one second.
Comparator function intermittently ON, Pch-Switch OFF in Backup Mode
In case of VDET3 < VDD, it moves to Normal Mode.

I²C Bus Interface

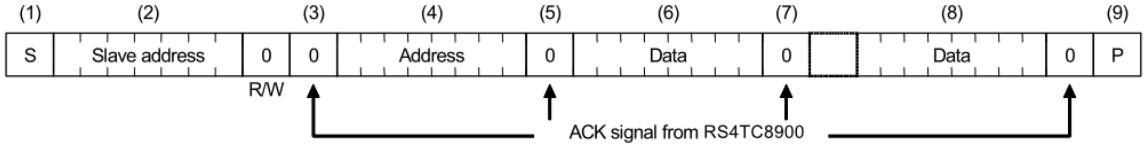
The RS4C1338 supports the I2C protocol. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The RS4TC8900 operates as a slave on the I2C bus. Within the bus specifications, a standard mode (100kHz cycle rate) and a fast mode (400kHz cycle rate) are defined. The RS4TC8900 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is [0110010].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

	Transfer Data	Slave Address							R/W bit
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	65 h	0	1	1	0	0	1	0	1= Read
Write	64 h								0 = Write

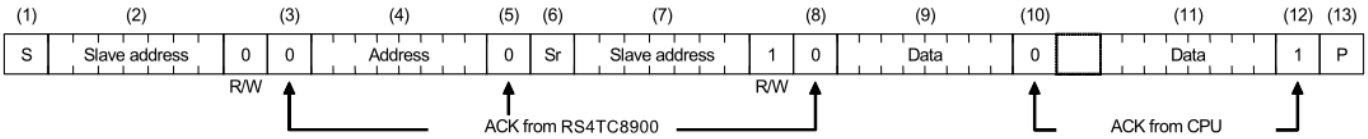
I2C write sequence

Since the RS4TC8900 includes an address auto increment function, once the initial address has been specified, theRS4TC8900 increments (by one byte) the receive address each time data is transferred.
(1) CPU transfers start condition [S].
(2) CPU transmits the RS4TC8900's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RS4TC8900.
(4) CPU transmits write address to RS4TC8900.
(5) Check for ACK signal from RS4TC8900.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RS4TC8900.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



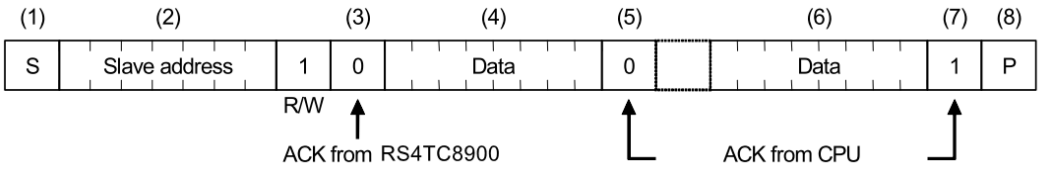
I2C read sequence

After using write mode to write the address to be read, set read mode to read the actual data.
(1) CPU transfers start condition [S].
(2) CPU transmits the RS4TC8900's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RS4TC8900.
(4) CPU transfers address for reading from RS4TC8900.
(5) Check for ACK signal from RS4TC8900.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RS4TC8900's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RS4TC8900 (from this point on, the CPU is the receiver and the RS4TC8900 is the transmitter).
(9) Data from address specified at (4) above is output by the RS4TC8900.
(10) CPU transfers ACK signal to RS4TC8900.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].



Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.
(1) CPU transfers start condition [S].
(2) CPU transmits the RS4TC8900's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RS4TC8900
(from this point on, the CPU is the receiver and the RS4TC8900 is the transmitter).
(4) Data is output from the RS4TC8900 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RS4TC8900.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RS4TC8900.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].



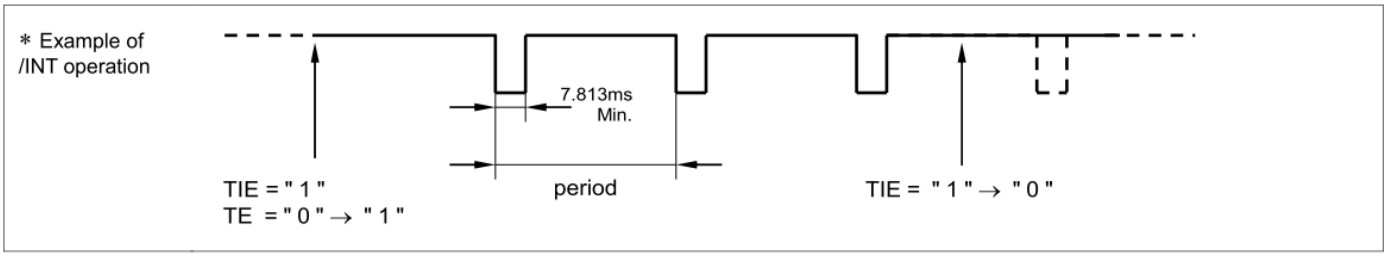
Address auto increment in Read/Write

In Basic time and calendar resister.
Address：08 - 09 - 0A - 0B - 0C - 0D - 0E - 0F - 00 - 01 - 02 -
In Extension resister
Address ： 18 - 19 - 1A - 1B - 1C - 1D - 1E - 1F - 10 - 11 - 12 -

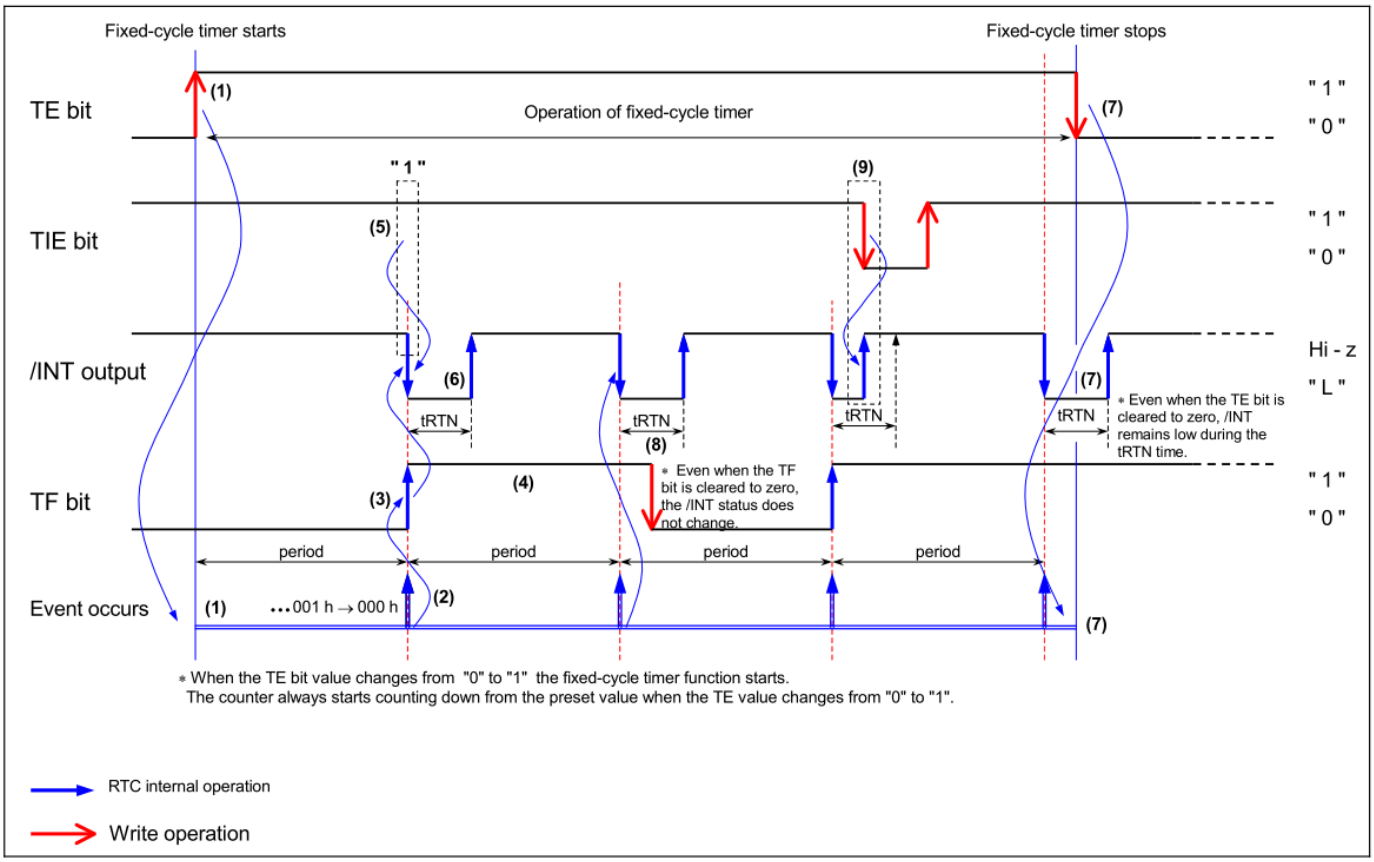
Function Description

Fixed Cycle Timer Interrupt Function

This interruption is released automatically, that is most suitable for a wakeup timer or an interval operation system.
The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14us and 4095 minutes.
When an interrupt event is generated, the /INT pin goes to low level and "1" is set to the TF bit to report that an event has occurred. However, when a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low-level to Hi-Z).



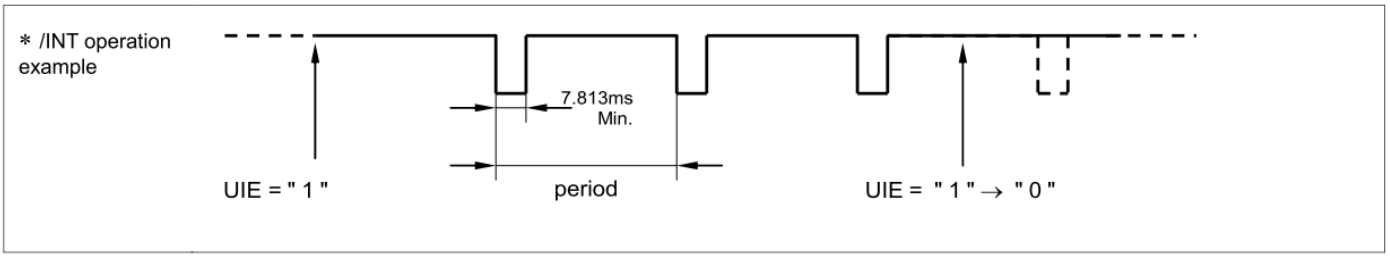
Fixed-cycle Timer Interrupt Timing Chart.

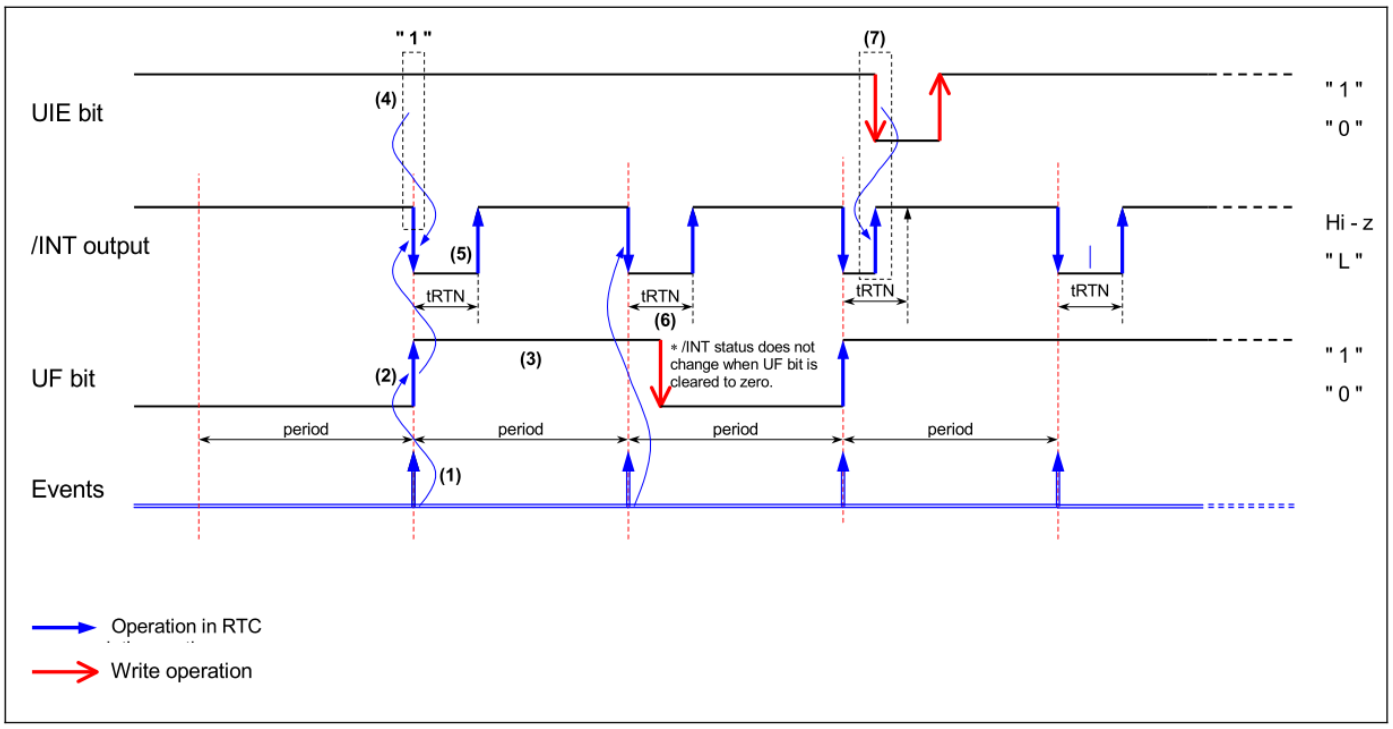


(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.
(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). After the interrupt event occurs, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)
(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.
(4) When the TF bit = "1" its value is retained until it is cleared to zero.
(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /INT pin output goes low. If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.
(6) Output from the /INT pin remains low during the t_{RTN} period following each event, after which it is automatically cleared to Hi-Z status. /INT is again set low when the next interrupt event occurs.
(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped, and the /INT pin is set to Hi-Z status. When /INT=low, the fixed-cycle timer function is stopped. The t_{RTN} period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.
(8) As long as /INT=low, the /INT pin status does not change when the TF bit value changes from "1" to "0".
(9) When /INT= low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) earliest 7.813ms (fixed value) after the interrupt occurs.

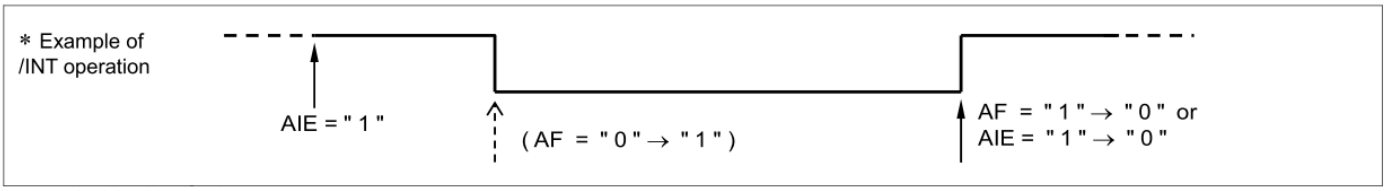


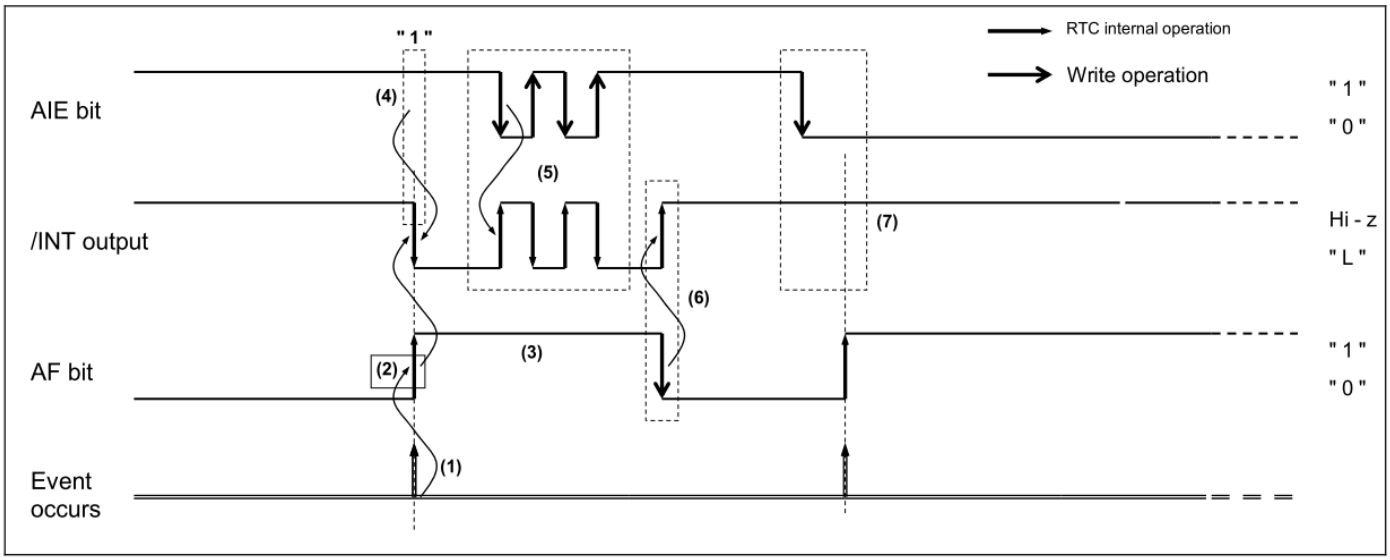


(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.
(2) When a time update interrupt event occurs, the UF bit value becomes "1".
(3) When the UF bit value is "1" its value is retained until it is cleared to zero.
(4) When a time update interrupt occurs, /INT pin output is low if UIE ="1".
If UIE ="0" when a timer update interrupt occurs, the /INT pin status remains Hi-Z.
(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.813 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
/INT pin output goes low again when the next interrupt event occurs.
(6) As long as /INT=low, the /INT pin status does not change, even if the UF bit value changes from "1"to "0".
(7) When /INT=low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.





(1) The minute, hour, day and date, when an alarm interrupt event is supposed to occur has to be set in advance, along with the WADA bit (Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
(2) When a time update interrupt event occurs, the AF bit values becomes "1".
(3) When the AF bit = "1", its value is retained until it is cleared to zero.
(4) If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low. When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.
(5) If the AIE value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.
(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z.
(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z.

The interrupt functions via /INT-pin or polling

1) How to identify events, when the interruption was occurred.

/INT output pin is common output terminal of interrupt events of three types (Fixed-cycle timer interrupt , Alarm interrupt, Time
update interrupt).
When INT asserted to Low, the system can determine in which interruption was occurred, by confirming status of (TF,AF, UF).

2) The method of detection of interruption with not using an INT output.

1. be left open INT.
2. be clears to 0 in TIE, AIE, and UIE bits.
3. monitor the TF, AF, UF. (Polling).

Temperature compensation function

During the production process of the RTC, we are programming the individual characteristics of the built-in crystal into the non-volatile memory of the RTC. The build-in temperature sensor measures the actual temperature of the module and compensates the oscillation frequency of the crystal oscillator using the stored compensation data. This way not only the time information is temperature compensated, but as well the FOUT signal, even when outputting 32.768kHzThis function works in the supply voltage range VTEM.
Even if the power supply voltage falls below VTEM and a VDET bit is set to "1", the temperature compensation operation is performed again if the supply voltage raises above VTEM.

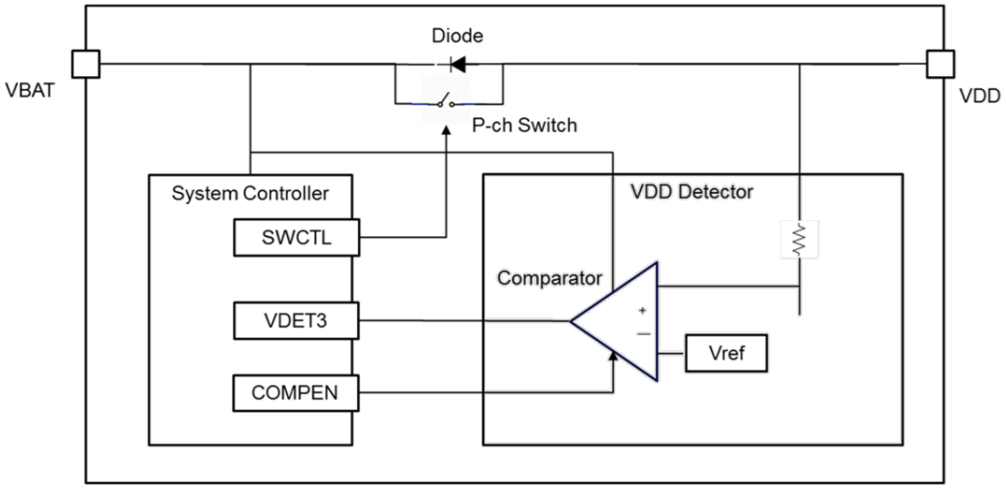
Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0F,1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET

CSEL1, CSEL0 bit (Compensation Interval Select 1,0)
This bit sets an interval of a temperature compensation operation.
Current consumption decreases when increasing the Compensation Interval by means CSEL1,0. CSEL1,0 is set at the time of initial power-up to ("0","1").

CSEL1	CSEL0	Compensation Interval
0	0	0.5s
0	1	2.0s (default)
1	0	10s
1	1	30s

Battery backup switchover function

This function consists of a supply voltage detector, which detects if the main supply voltage "VDD" drops below a threshold (VDET3). During the voltage detection period, the built-in P-ch switch located between the main supply voltage pin "VDD" and the backup power supply pin "VBAT" is opened, in case of VDET3 < VDD, the RTC works in Normal Mode, else (VDD≤VDET3) it switches into Backup Mode. To measure the supply voltage applied to VDD, the P-ch switch opens once every second and the diode prevents current flow from VBAT over the RTC into VDD.



Diode (between VDD and VBAT) reference characteristic's

Symbol	Characteristics	Condition
On-Resistance of Pch-Switch	100 ohm(typ.)	VDD = 3.0 V, Ta=25℃
V_f	0.60 V / 1 mA (typ) 0.85V / 10mA (typ)	VDD = 3.0 V, Ta=25℃
I_R	Less than 6 nA	VDD = 5.5 V，-40 to 105℃

Battery Backup related register setting

After power on reset, VDETOFF=0, SWOFF= 0, BKSMP0=0, BKSMP1=0 are set as default value.
So 1sec after power on reset, VDD voltage is detected and goes to Normal Mode (VDET3 < VDD) or Backup Mode (VDD ≦ VDET3).
The duration of VDD voltage detection is controlled by means of BKSMP0-bit, BKSMP1-bit and can be set to be 2msec, 16msec, 128sec or 256msec. VDD voltage is detected at the end of this time, so at the falling edge of the comparator ON signal.

Battery Backup switchover related register setting

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
18	Backup Function	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	R/W

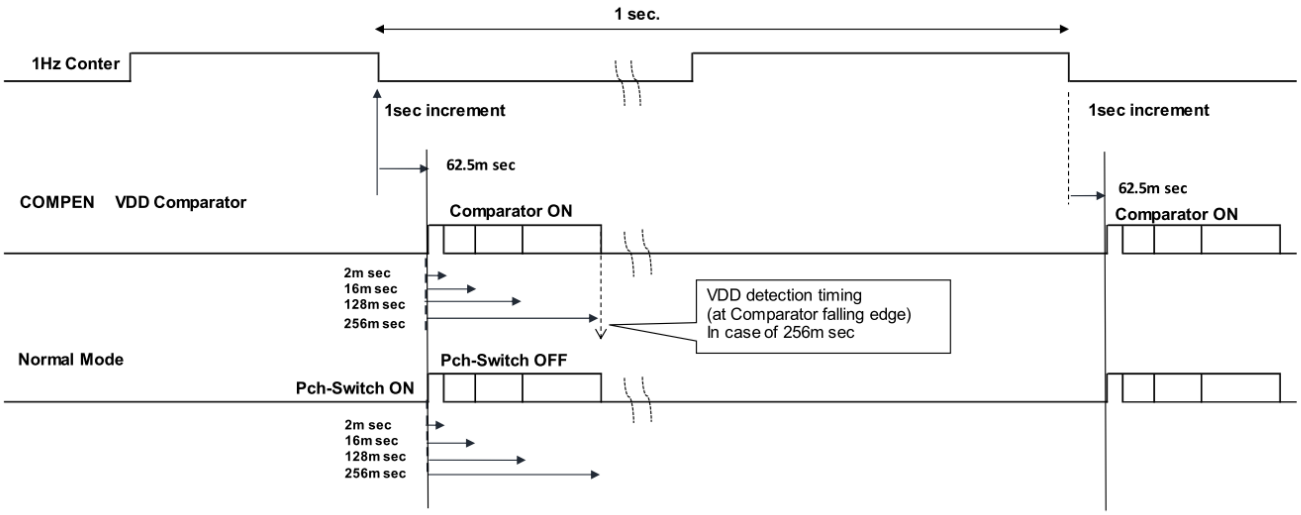
VDD detector	VDETOFF	SWOFF	BKSMP1	BKSMP0	VDET3 Samplingperiod	Pch-Switch ON/OFF	Remarks
ON	0	X	0	0	2ms	2ms OFF	VDETOFF:0,BKSMP1:0,BK SMP0:0 default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256ms OFF	
OFF	1	0	X	X	OFF	ON	VDD and VBAT short circuit via Pch-switch
		1	X	X	OFF	OFF	VDD connected via diode to VBAT

X = Don't care.

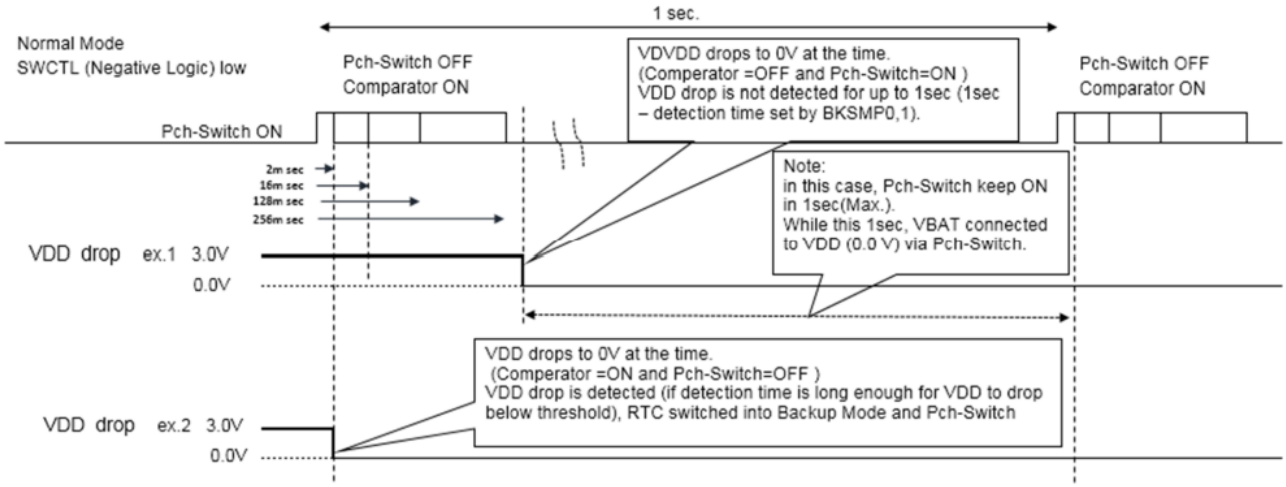
The detection period Setting

Since a VDD drop below VDET3 is only detected while the Pch-switch is open, user should carefully set the VDD detection period (by means of BKSMP0 and BKSMP1) to make sure the VDD voltage applied to the RTC VDD-pin falls below the VDET3 threshold during this time.

Term	VDD voltage detection period		Remarks
	2ms	256ms	
Current consumption (Normal Mode)	small	large	Longer detecting period increases VDD Detector current consumption.
Backup battery Charging effectiveness (Normal Mode)	Smaller detection period makes better charging effectiveness.		During detection period、Backup battery is charged through Diode.
Actual VDD voltage detecting period (Normal Mode)	Smaller detection period is better for slower VDD falling.	Longer detection period is better for prompt VDD falling.	



If the voltage detection period is not set long enough by means of BKSMP0 and BKSMP1, a steep VDD voltage drop might not be detected and thus the backup power supply is discharged into VDD. Between the voltage detection periods once per second, the Pch-switch is closed and thus the backup power supply discharges into VDD as well. To avoid this backup battery discharge, a diode might be set between VDD pin to power line.

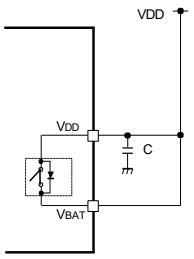


Connection examples

[Ex-1] Single power supply.

External supply should be connected to both VDD and VBAT.
In this case, interface (I2C, FOUT) are active in a supply voltage range from 1.6V to 5.5V anytime.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	1	X	X	X
Parts	X = Don't care. C = 0.1uF							

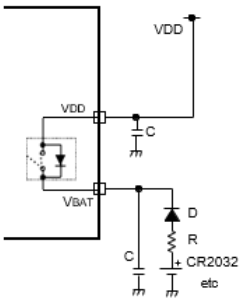


Example.1

[Ex-2] Non- rechargeable battery. ex. CR2032, AAA-battery

When VDD shut to OFF,
Battery current is leak to VDD(0.0V) while 1sec(Max.). Refer

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	0	0	X	X
Parts	C = 0.1uF. R = 100ohm(Min.) D = Schottky Barrier type							

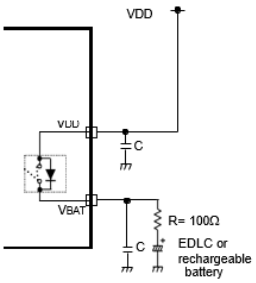


Example.2

[Ex-3] Rechargeable battery. ex. EDLC, ML-series

In this case the current limiting resistor on VBAT should be set to 100 Ohm. Smaller resistor value brings over current to the RTC.
Bigger resistor value might make the supply voltage of the RTC to drop below VLOW or VDET at the time of power-switchover.
When a bigger higher resistor value is required to control the charging current to EDLC, or while 1sec(Max.), current leak into VDD(0.0V) from VBAT is so serious in system, it is recommended to use connection Example.4.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	0	0	X	X
Parts	C = 0.1uF. R = 100ohm(Min.) X = Don't care.							

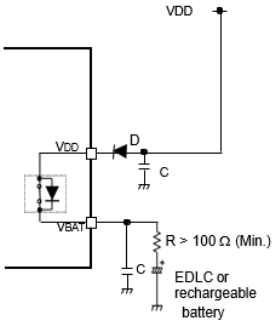


Example.3

[Ex-4] For using high value protection resistor.

This circuit is recommended in case a current flow for up to 1 sec from VBAT into VDD, before entering backup-mode is not acceptable or in case the current of the EDLC or rechargeable battery has to be limited to values which can't be assured with a R = 100 Ohm as recommended in Example.3.

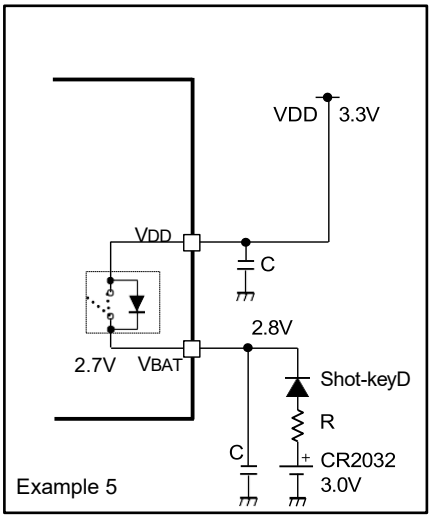
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	1	0	X	X
Parts	C = 0.1uF. (Max.) R = 100ohm(Min.) to Free. D = Schottky Barrier type. X = Don't care							



Example.4

Diode characteristics.

For example.
In connection Example 2, VDD is 3.3V and CR2032 is 3.0V. when VF of RTC's Diode is 0.6V, out of RTC's Diode is 2.7V. and VF of outside Diode is 0.2V, VBAT voltage is 2.8V.
In this case, even if VDD is active, RTC use 2.8V from CR2032 anytime. as a results, CR2032 life very shorten than an assumption.
In a choice of a diode, consider balance of the voltage carefully.



Example 5

Example of solution for above.
A Schottky diode(D2) is installed in a VDD side. and RTC's diode is bypassed.
Therefore, voltage drop of VDD depends on only V/F of D2. As a result, examination of simple circuitry is possible.

Example

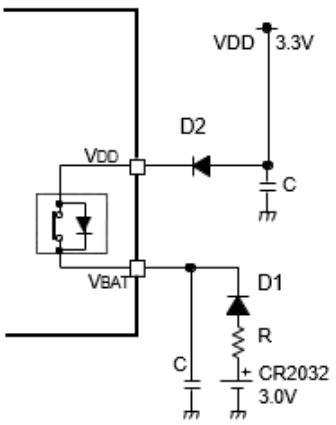
it just Diode-OR-circuit
Confirm each of V/F characteristics carefully.

Address 18h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	○	○	○	○	VDET OFF	SWOFF	BKSMP 1	BKSMP0
Data	0	0	0	0	1	0	X	X

Parts

X Bit = Don't care. C = 0.1uF.
R = 100Ω (Min.)
D1 & D2 = Schottky Barrier type.

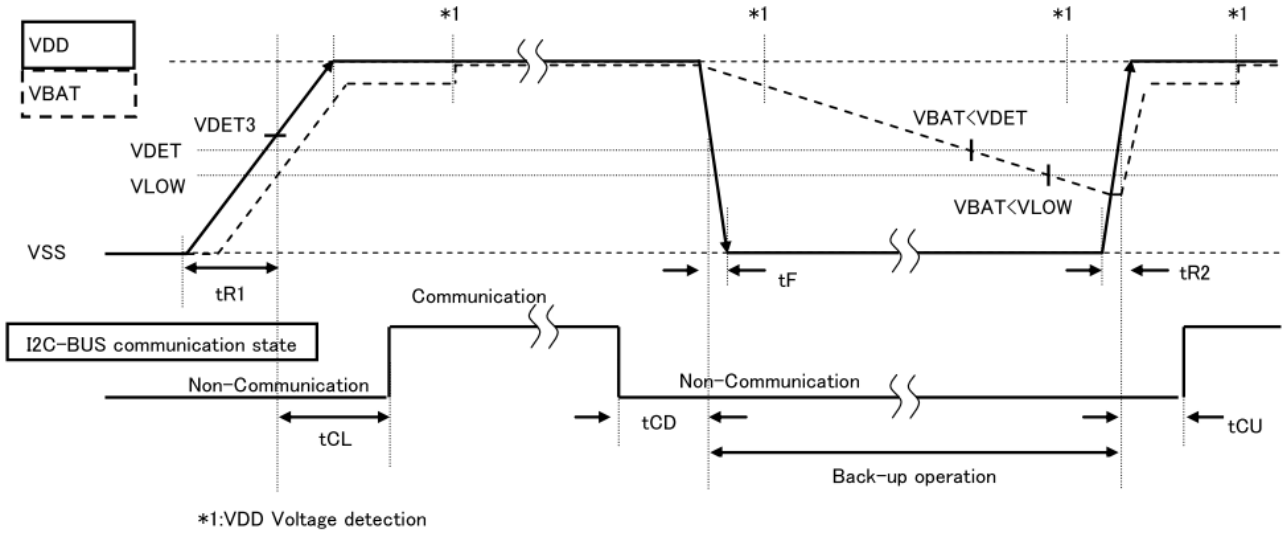
To avoid a wasted leakage current.
When VDD is OFF, I/R characteristics of Diode(D2) is important. Confirm IR characteristics of Diode with Temp characteristics.



Example.6

Backup and Recovery

This circuit is sensitive to power supply noise and supply voltage should be stabilized to avoid negative impact on the accuracy.
tR1 is needed for a proper power-on reset. If this power-on condition cannot be kept, it is necessary to send an initialization routine to the RTC by software.
In case of repeated ON/OFF of the power supply within short term, it is possible that the power-on reset becomes unstable. After power-OFF, keep VDD=VBAT=GND for more than 10 seconds for a proper power-on reset. When Power-on-reset is uncertainty, system can initialize the RTC by the software.
When a controller goes to shutdown, a CPU sent STOP condition to RTC, then that I2C communication is complete status is recommended.

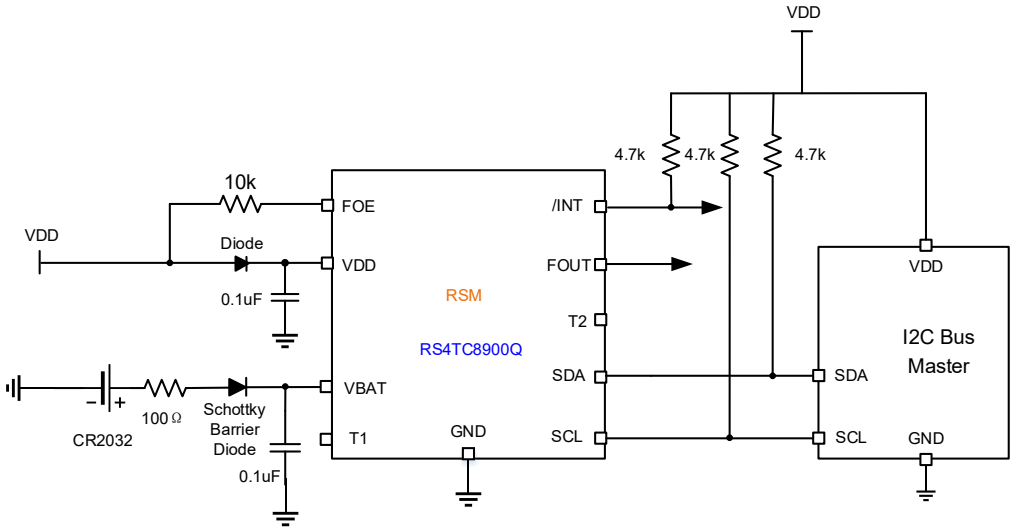


Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VDET	Detection voltage VDET-bit threshold		1.9	1.95	2	V
VLOW	Detection voltage VLF-bit threshold		1.16		1.6	V
VDET3	Detection voltage Backup-switchover voltage		2.3	2.4	2.5	V
tR1	Power supply rise time1	VDD=VSS to 2.5V	1		10	ms/V
tCL	Access wait time (After initial power on)	After VDD=2.5V	30			ms
tCD	Access disable hold time	After stop condition	0			µs/V
tF	Power supply fall time	VDD=2.5V to VSS	2			µs/V
tR2	Power supply rise time2	VDD=VSS to 2.5V	15			µs/V
tCU	Access wait time (Normal power on)	After VDD=2.5V	0			µs

Backup return and power on initialize

Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized.
1) The first, System should confirm status of VLF-bit.
2) When VLF is "1", system must initialize all of registers.
3) When initial-power-ON was given to RTC, wait for t_{STA} (3 seconds) for setup of time and Calendar.
But readout access is permitted after 30ms from VDD=VCLK.

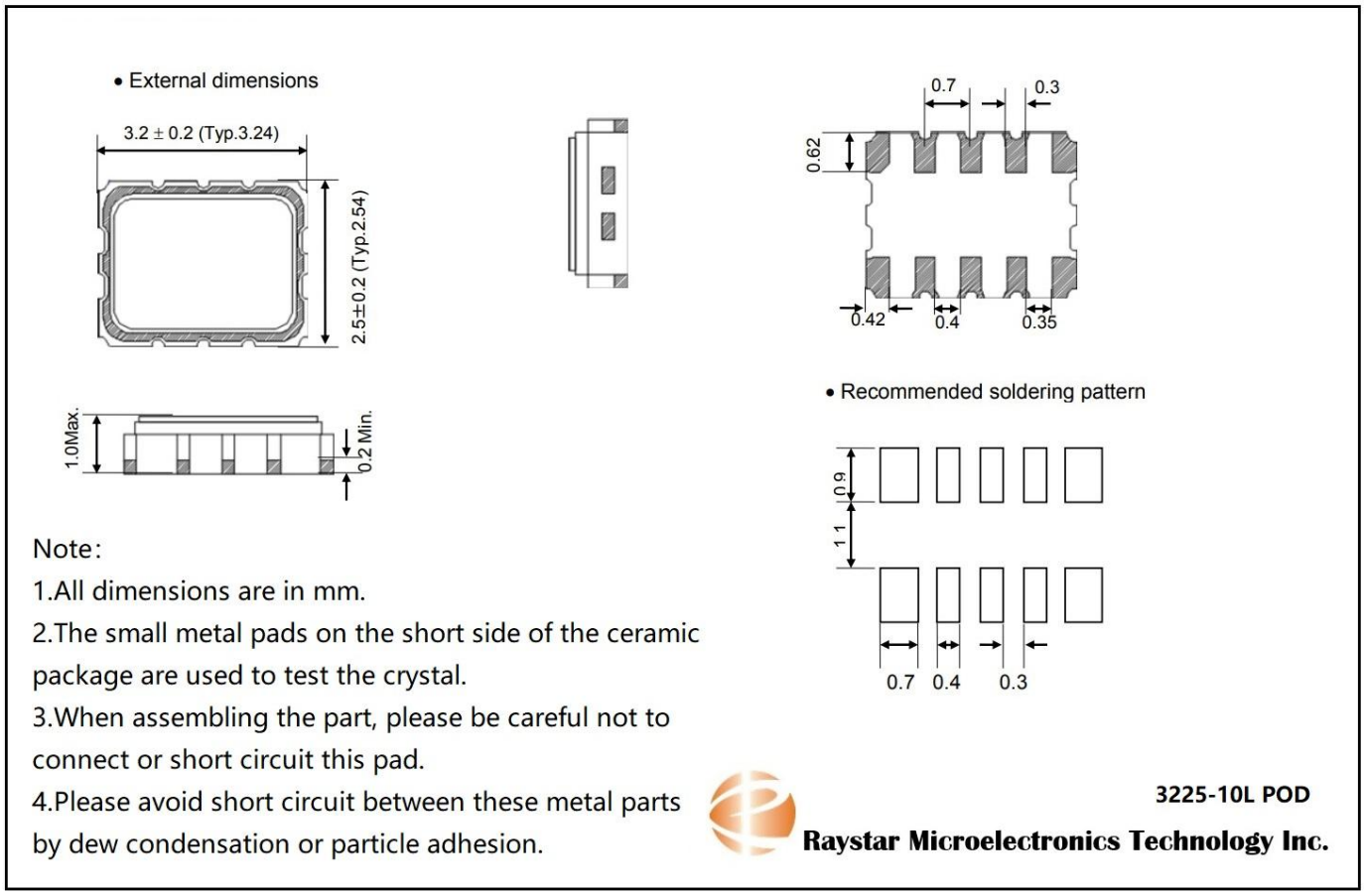
Application Circuit



Note : 1. install 2 bypass condensers in nearest position of a limit to pin of both VDD and VBAT.
2. A diode should be added to the VDD pin

Package Information

3225 -10 pin



Revision History

Revision	Description	Date
1.0	Initial release.	2023/06/13
1.1	Add AEC-Q100 qualified description.	2023/08/30
1.2	1. Modify DC characteristics IDD value. 2. Delete Connect examples of VBAT switch circuit. 3. Modify Frequency stability to 3.4ppm in -40 to 85℃.	2024/04/16
1.3	1. Modify ESD CMD and HBM voltage value 2. Modify ordering information 3. Modify IDD spec 4. ADD" AE" bit description 5. Delete temperature calculation formula 6. Modify Fix-cycle timer control register description	2024/05/21
1.4	Modify ESD HBM value	2024/06/07
1.5	Add 8900QCE-B and -C Part Number in the ordering information table. Update the table of AC Characteristics – Frequency, add Suffix B for 10 ppm and C for 20ppm	2024/09/27
1.6	Update Application Circuit	2024/11/11
1.7	Add 8900QCE-F Part Number in the ordering information table.	2025/02/26
1.8	Add the examples of VDD and VBAT switch circuit.	2025/04/01
1.9	Update the table of AC Characteristics – Frequency and ordering information table.	2025/09/29