Features

- Built in frequency adjusted 32.768 kHz crystal unit.
- Interface typ: IIC Bus interface (up to 400 kHz)
- Wide operating voltage range: 1.6 V to 5.5 V
- Wide timekeeper voltage range: 1.1 V to 5.5 V
- Auto power switching function: Switchover by main power supply monitor.
- Backup battery charge control function: For rechargeable lithium batteries.
- Low leak current: A leak current from a backup power supply pin. 5 nA Max.
- Reset function: At low supply voltage, external reset signal is generated.
- Low voltage detection: Supply voltage and backup voltage detection
- Time correction: Digital offset function
- The various function including full calendar, alarm, timer, etc.

Applications

- small electronic devices
- low power IoT devices

Description

RS5C8130B is a real-time clock module of the IIC serial interface system, 32.768 kHz crystal and oscillator is built-in it. The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, wakeup timer, and time update interruption, among other features. By the backup battery charge control function and the interface power supply input pin, RS5C8130Bcan support various power supply circuitries.
All these many functions are implemented in a thin, compact ceramic package, which makes it suitable for various kinds of small electronic devices, low power IoT devices etc.

Ordering Information

Ordering Code	Package	Description
RS5C8130B	3225	3.2mm x 2.5mm

Block Diagram

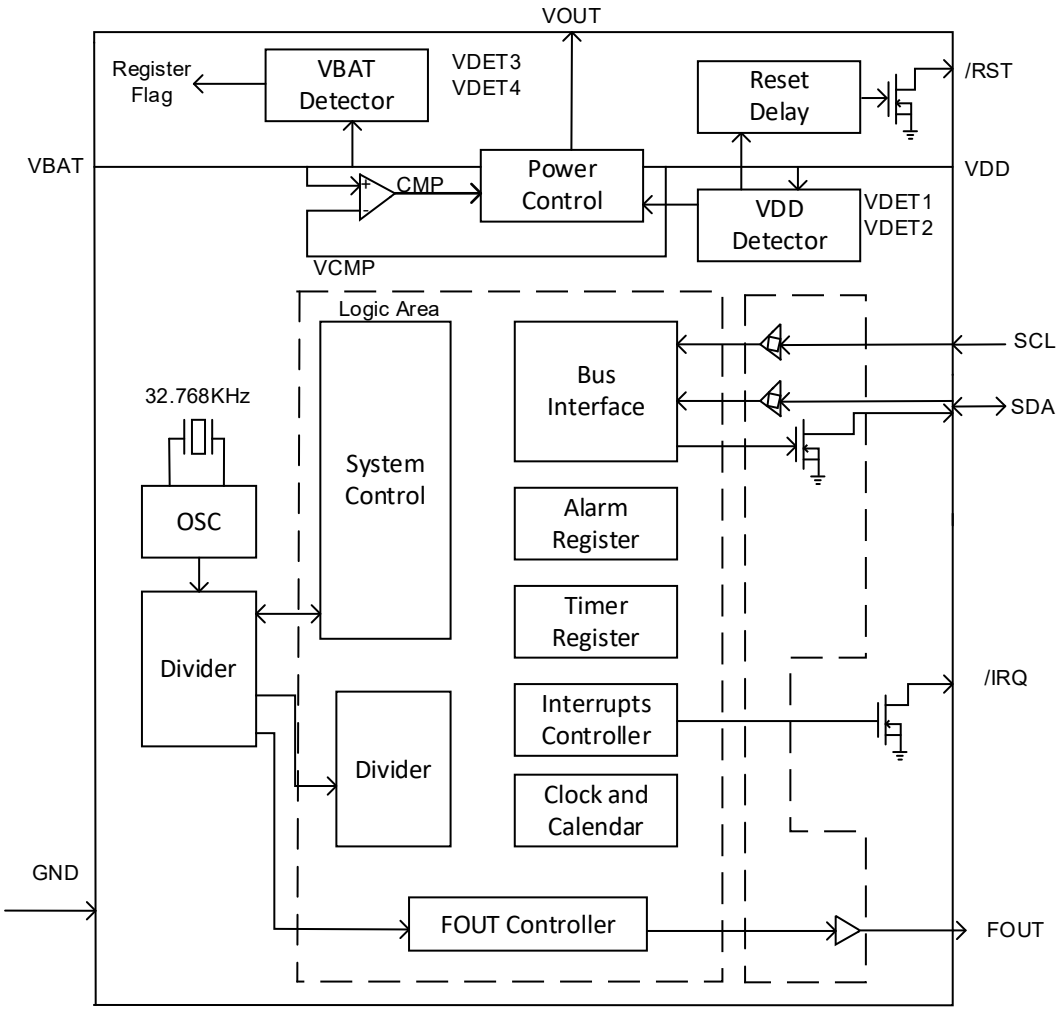


Figure 1 Block Diagram

Typical Application Circuit

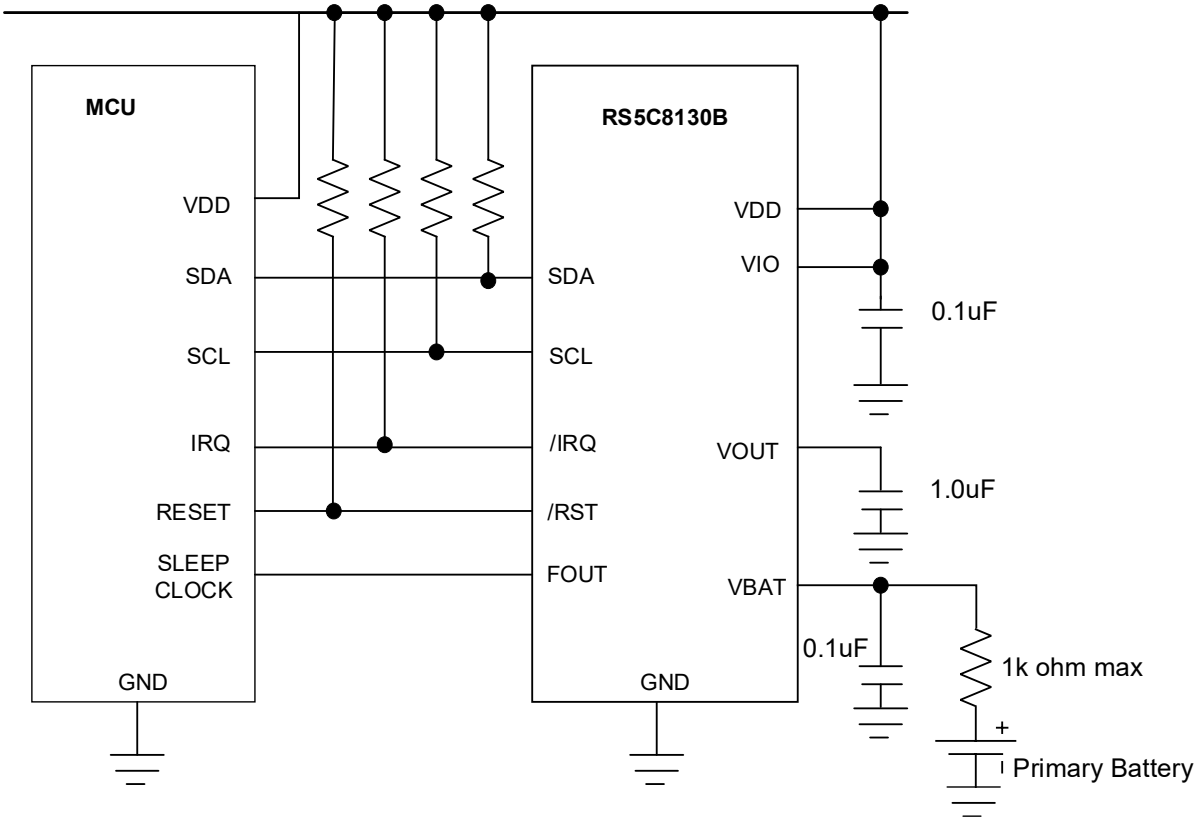


Figure 2 Typical Application Circuit

Pin Configuration

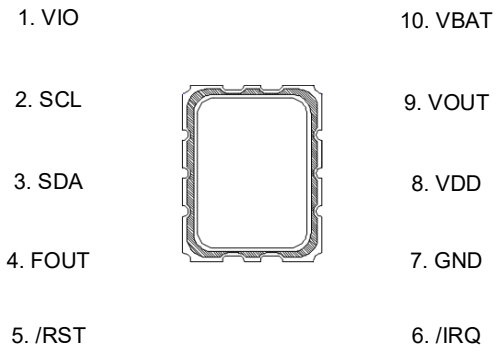


Figure 3. Pin Configuration

Signal name	I/O	Function
SCL	Input	Serial clock input pin.
SDA	Bi-directional	Data input and output pin.
FOUT	Output	Frequency output pin with output control function. (CMOS) Output frequency can be selected as 32.768 k Hz, 1024 Hz, 1 Hz.
/ RST	Output	Even in the backup mode, this pin can operate. In case of VDD voltage drop detection, a reset signal is outputted. (N-ch open drain) In case of VDD voltage rise detection, it releases the reset signal after 60ms.
/ IRQ	Output	Interrupt output by Alarm and Timer events.(N-ch open drain) This pin can output even a backup mode.
VDD	-	This is a power-supply pin for the internal logic.
VIO	-	This is an interface power supply pin. Connect the same power supply as the MCU.
VOUT	-	Internal voltage output pin. Connect smoothing capacitor of 1.0uF
VBAT	-	This is a power supply pin for backup battery. This is a pin to connect a large-capacity capacitor, a secondary battery, and a primary battery. In a backup mode, the voltage is supplied inside by this pin.
GND	-	Connected to a ground.

Note:

1、 Connect a bypass capacitor rated at least 0.1μF between power supply pins and GND pin.

2、 Use the FOUT, /RST, /IRQ terminals as Open when not in use. Don't connected to GND or VDD

Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage	VDD	-	-0.3 ~ +6.5	V
Internal voltage	VOUT	-	-0.3 ~ +6.5	V
Backup supply voltage	VBAT	-	-0.3 ~ +6.5	V
Interface supply voltage	VIO	-	-0.3 ~ +6.5	V
Input voltage 1	VIN1	SCL, SDA	-0.3 ~ +6.5	V
Output voltage 1	VOUT1	/RST, /IRQ, SDA	-0.3 ~ +6.5	V
Output voltage 2	VOUT2	FOUT	-0.3 ~ VIO+0.3	V
		When stored separately, without packaging	-55 ~ 125	°C

Recommended Operating Conditions

Unless otherwise specified, GND = 0 V , Ta = -40° C to +85° C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VDD	INIEN = 0	1.25	3.0	5.5	V
		INIEN = 1	VDET1	3.0	5.5	V
Interface supply voltage	VIO	INIEN=0	1.6	3.0	5.5	V
		INIEN=1 VDD > VDET1				
Clock supply voltage	VCLK	Backup operation mode (VOUT)	1.1	3.0	5.5	V
Operating temperature	T use	No condensation	-40	+25	+85	° C

Frequency Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output frequency	fo		Typ 32.768			kHz
Frequency stability	Δ f / f	Ta = +25 °C VDD = 3.0 V	5 ± 23			× 10^{-6}
Frequency/voltage characteristics	f / V	Ta = +25 °C VDD = 1.1 V ~ 5.5 V	−2		+2	× 10^{-6} / V
Frequency/temperature characteristics	Top	Ta = −20 °C ~ +70 °C VDD = 3.0 V ; +25 °C reference	−120		+10	× 10^{-6}
Oscillation start time	t_str	VDD = 2.75 V ~ 5.5 V Internal Crystal oscillation start		0.19	1.0	s
Aging	fa	Ta = +25 °C , VBAT = 3.0 V; first year	−5		+5	× 10^{-6} / year

DC characteristics

Unless otherwise specified, GND = 0 V, VBAT = VDD = 1.1 V ~ 5.5 V, VIO = 1.6 V ~ 5.5 V Ta = –40 °C to 85° C

Item	Symbol	Condition		Min	Typ	Max	Unit
Current consumption in normal operation mode without FOUT (1)	IDD	SCL = SDA = "H" ,FOUT = OFF, /IRQ = OFF, VDD=VIO = 3.0 V, CHGEN = 0b or VBAT ≧ VDET3			1.8	2.0	uA
Current consumption in normal operation mode without FOUT (2)	I32k	SCL = SDA = "H" ,FOUT = 32768Hz, /IRQ = OFF, VDD=VIO = 3.0 V, CHGEN = 0b or VBAT ≧ VDET3			4	4.5	uA
Current consumption in backup mode (3)	IBAT	SCL = SDA = "L" , VBAT = 3.0 V ,VDD=VIO = 0.0 V			0.6	0.8	uA
Detector Threshold Voltage1 (rising edge of VDD)	+VDET11	2.75V setting Reset-releases		2.72	2.8	2.88	V
Detector Threshold Voltage1 (Falling edge of VDD)	-VDET11	2.75V setting Reset output		2.67	2.75	2.83	V
Detector Threshold Voltage2 (rising edge of VDD)	+VDET12	2.7V setting Reset-releases		2.67	2.75	2.83	V
Detector Threshold Voltage2 (Falling edge of VDD)	-VDET12	2.7V setting Reset output		2.62	2.7	2.78	V
Detector Threshold Voltage3 (rising edge of VDD)	+VDET2	Switching voltage from VBAT to VDD		1.25	1.35	1.45	V
Detector Threshold Voltage3 (falling edge of VDD)	-VDET2	Switching voltage from VDD to VBAT		1.2	1.3	1.4	V
Detector Threshold Voltage1 (rising edge of VBAT)	+VDET31	Charge stop voltage(full charge) BFVSEL=00b		2.94	3.02	3.1	V
Detector Threshold Voltage1 (Falling edge of VBAT)	-VDET31	Recharge voltage BFVSEL=00b		2.89	2.97	3.05	V
Detector Threshold Voltage2 (rising edge of VBAT)	+VDET30	Charge stop voltage(full charge) BFVSEL=10b		2.84	2.92	3	V
Detector Threshold Voltage2 (Falling edge of VBAT)	-VDET30	Recharge voltage BFVSEL=10b		2.79	2.87	2.95	V
Detector Threshold Voltage3 (rising edge of VBAT)	+VDET32	Charge stop voltage(full charge) BFVSEL=01b		3	3.08	3.16	V
Detector Threshold Voltage3 (Falling edge of VBAT)	-VDET32	Recharge voltage BFVSEL=01b		2.95	3.03	3.11	V
VBAT end voltage	-VDET4	Low VBAT detection Register flag VBLF=1b		2.32	2.4	2.48	V
VDD-VOUT Off – leak current	ISW1	VOUT=3V VDD=0V				5	nA
VBAT – VOUT Off – leak current	ISW2	VBAT=3V VOUT=0V				5	nA
VOUT output voltage 1	VOUT1	VDD = 3.0 V IOUT = 1 mA			VDD-0.06		V
VOUT output voltage 2	VOUT2	VBAT = 3.0 V IOUT = 0.1 mA			VBAT-0.02		V
High-level input voltage	VIH1	SCL, SDA		0.8 x VIO		5.5	V
Low-level input voltage	VIL	SCL, SDA		GND- 0.3		0.2 x VIO	V
High-level output voltage	VOH	FOUT	IOH= -1mA	VIO-0.5		VIO	V
Low-level output voltage	VOL1	FOUT	IOL= 1mA	GND		GND+0.5	V
	VOL2	/RST,/IRQ	VOL=5V,IOL=1mA	GND		GND+0.25	V
	VOL3		VOL=3V,IOL=1mA	GND		GND+0.4	V
	VOL4	SDA	VIO≥2V,IOL=3mA	GND		GND+0.4	V

AC characteristics

Unless otherwise specified GND = 0 V VIO = 1.6 V ~5.5 V Ta = -40°C ~ +85°C

Item	Symbol	Standard-Mode (fSCL=100 kHz)		Fast-Mode (fSCL=400 kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL		100		400	kHz
Start condition setup time	tSU;STA	4.7		0.6		µs
Start condition hold time	tHD;STA	4.0		0.6		µs
Data setup time	tSU;DAT	250		100		ns
Data hold time	tHD;DAT	0		0		ns
Stop condition setup time	tSU;STO	4.0		0.6		µs
Bus idle time between start condition and stop condition	tBUF	4.7		1.3		µs
Time when SCL = "L"	tLOW	4.7		1.3		µs
Time when SCL = "H"	tHIGH	4.0		0.6		µs
Rise time for SCL and SDA	tr		1.0		0.3	µs
Fall time for SCL and SDA	tf		0.3		0.3	µs
Allowable spike time on bus	tSP		50		50	ns

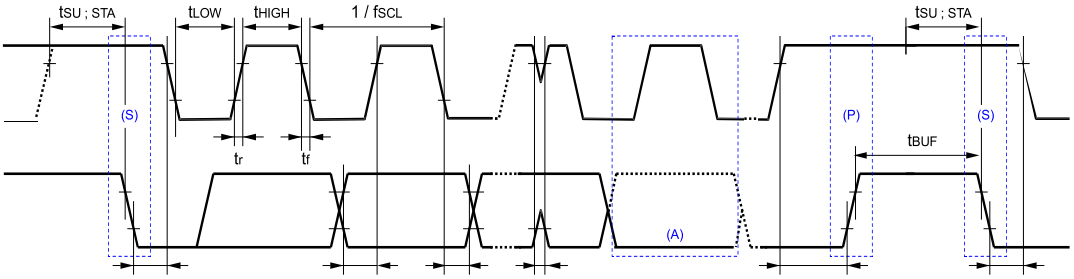


Figure 4 Timing Diagram

Warning: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds.
If such communication requires 0.95 seconds or longer, the IIC-Bus interface is reset by the internal bus timeout function. When bus-time-out occur, SDA turns to Hi-Z input mode.

Note: During access to the time registers, the time counting is on hold. This means that up to 1 second can be “lost” in case of unsuccessful communication as mentioned above.
Please make sure to send IIC start condition before actual transmission of the RTCs slave address as otherwise the slave address appears to be shifted by 1 bit.

AC characteristics (FOUT)

Unless otherwise specified GND = 0 V , VIO = 1.6 V ~ 5.5 V , Ta= –40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT symmetry	SYM	50% VIO Level	40		60	%

AC Characteristics (Reset)

Item	symbol	Min.	Typ.	Max.	unit
Reset internal delay time	tDELAY		60		ms
Reset delay time (Initial power ON)	tDELAY_F		250 (t_str + tDELAY)		ms

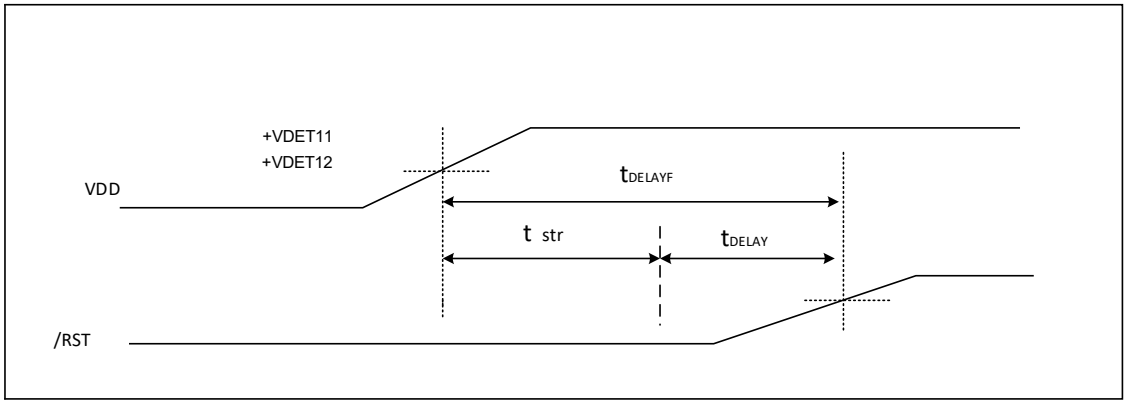


Figure 5 Reset signal timing chart (Power Initial Supply)

Reset timing

Item	symbol	Min.	Typ.	Max.	unit
Voltage detection time to reset release.	t_int			35	ms
Reset delay time (Recovery from Backup) t_int + t_DELAY	tDELAY_B	60		95	ms

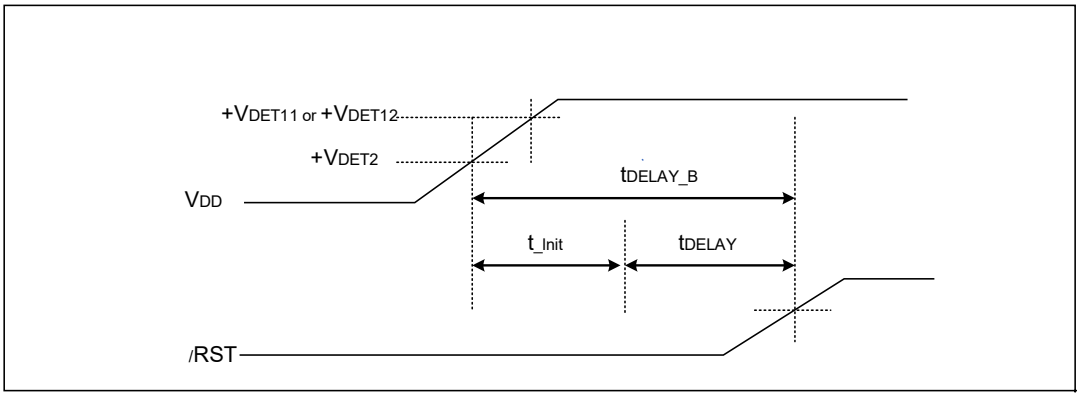


Figure 6 Reset signal timing chart (Backup resure)

Interface timing when power is turned ON / OFF

Restrictions of IIC-Bus interface in the initial power on

The operation of the RTC register is linked to the oscillation clock of the built-in crystal unit.
Therefore, it will not operate normally when the oscillation is stopped.
It is recommended that the initialization at the time of initial power-on is performed after the oscillation start time t_str characteristic.

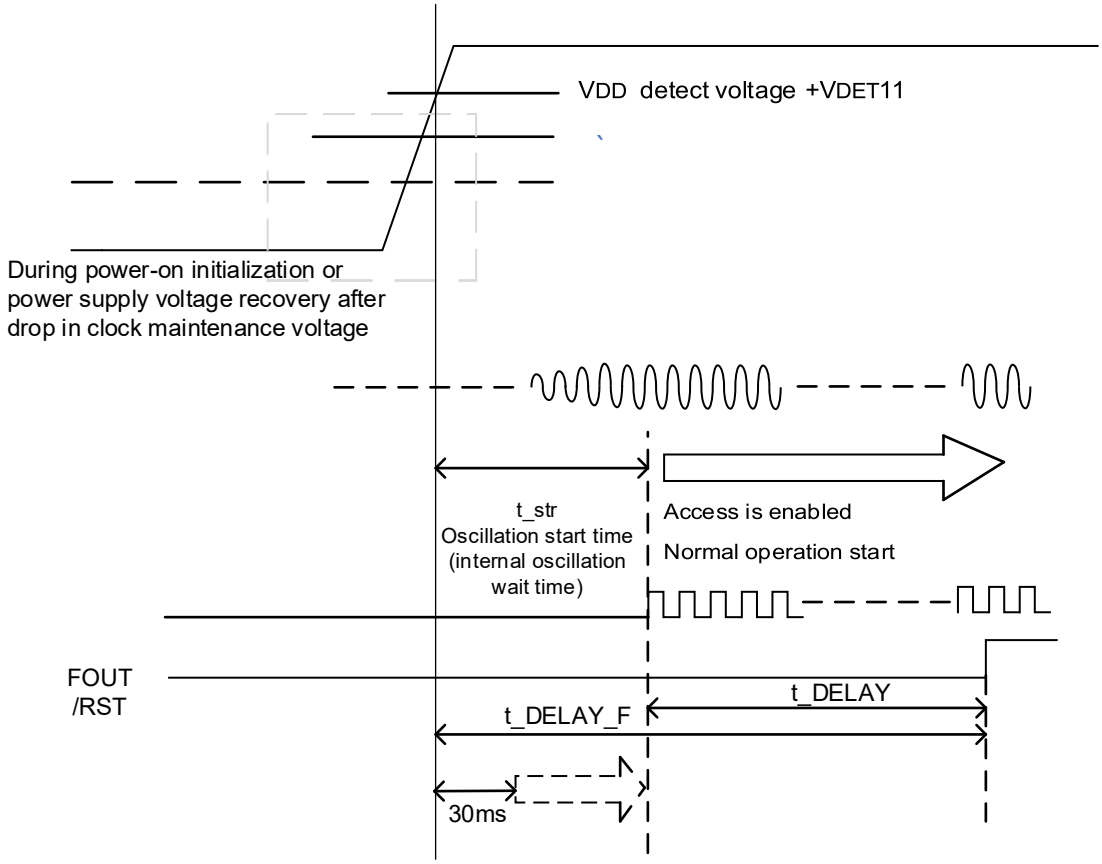


Figure 7 Power supply initial sequence

Precautions for power ON / OFF

1: To ensure that the power-on reset works at the initial power-on keep VDD=VBAT=GND for 10 seconds or more before VDD = ON.
2: Initial power-on tR1 is a necessary condition for enabling power-on reset.
If this condition is not satisfied, power-on reset may not work. As a result, the time accuracy and current consumption may not meet the specifications. Please reset by software.
3: When fluctuation of VDD is out of specifications, tF or tR2, it may be occur the followings, a momentary stop of crystal oscillation, a set of VLF by VOUT voltage drop lower than VCLK and so on.
4: The timing at which the IIC Bus interface is enabled differs in when the initial power of VDD is turned on and when VDD is turned on from backup mode.See the tCL and tCU specifications in the chart below.
5: These specifications don't mean a noise characteristic of a power supply of RTC. Do not use amplitude signal output from a signal generator etc, as a power source.

VDD ON / OFF when using power switching (INIEN = 1)

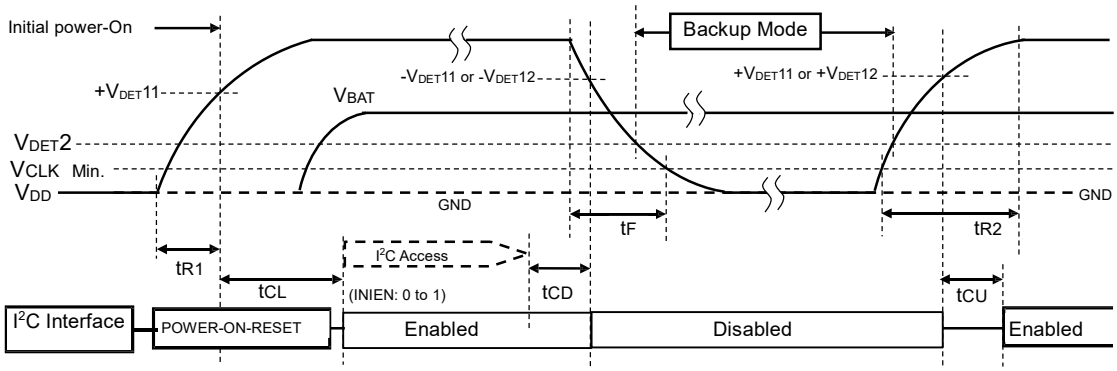


Figure 8 Power-On sequence1

VDD ON / OFF when power switching is not used (INIEN = 0)

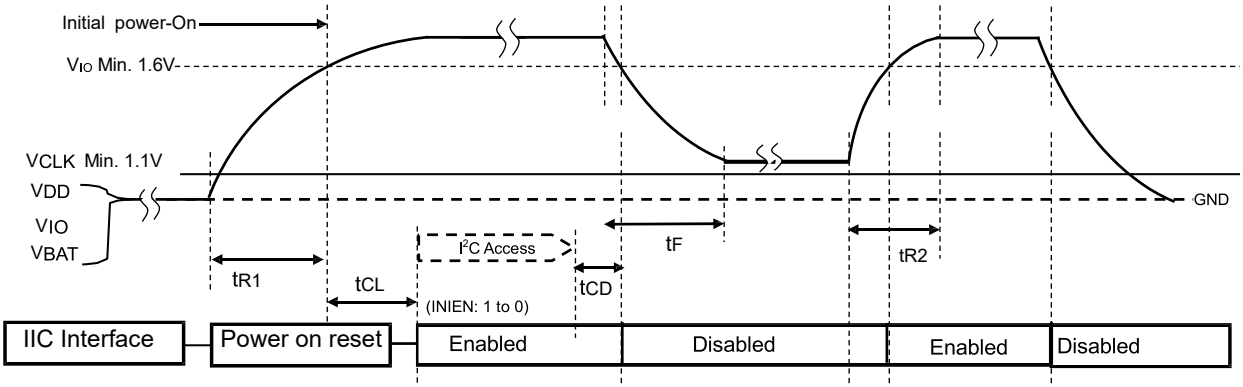


Figure 9 Power-On sequence2

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	tR1	From GND to VDD = +VDET11	0.1	-	10	ms / V
Access wait time	tCL	VDD = +VDET11 to Access start		-	-30	ms
Access suspended time	tCD	The time from the end of IIC access to the disable of IIC	0	-	-	ms
Power supply fall time	tF	From VDD to VDD = VCLK	1	-	-	ms / V
Power supply rise time	tR2	Time to restore VDD to operating voltage	1	-	-	ms / V
Access wait time	tCU	VDD=+VDET1x to Access start		-	35	ms

tR1, tR2, and tF specify that there is no voltage fluctuation faster / slower than the Min / Max specifications within the specified section. The risk when specifications were not satisfied, refer to the following.

Item	Risk of fast fluctuations	Risk of slow fluctuations
tR1	Power on reset don't occur	
tR2	The FOUT waveform disappears momentarily, and clock time is momentarily delayed A data of RTC loss. A set of VLF	None
tR3		

Power-on order

VDD and VIO separate and can give different power supplies.
In specifications range, the voltage relations(VDD and VIO) are free.
In the status that the voltage more than VDET+ was supplied to main power-source VDD, if VIO is unstable with the middle voltage between GND-VDD, a through-current will occur.
This leak current may 10uA by through-current.
If can't permit this 10uA, the below power-up sequence chart is recommended.
When the power-source supply of VDD is carried out earlier than VIO, please start VIO from a GND level not to become unstable. If can permit this 10uA, VDD and VIO and VBAT input it by an independent timing and do not have any problem. However by this through-current, RTC does not got damage and the malfunction does not occur.

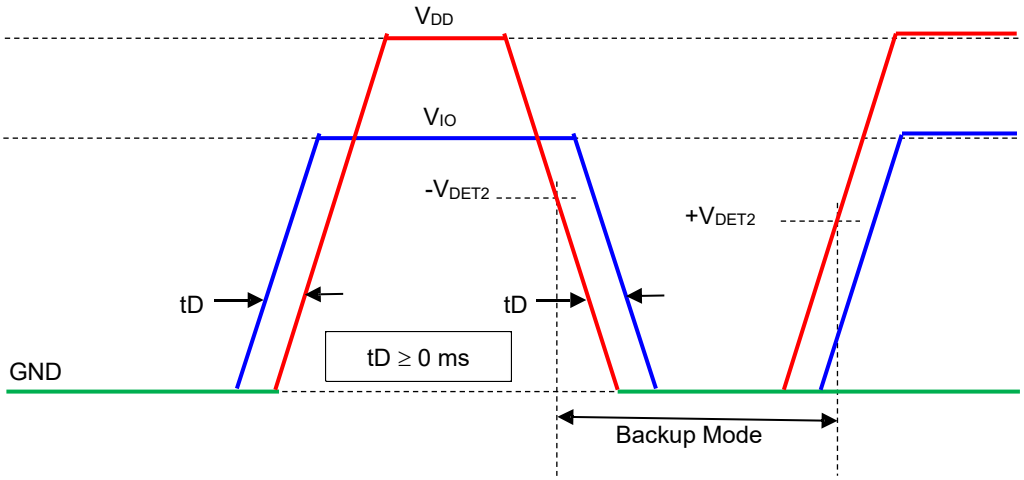


Figure 10 Power on order

Application Notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 uF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electronic noise near this module.

(3) Voltage levels of input pins

When the voltage of out of the input voltage specifications range input into an input terminal constantly, a penetration electric current occurs. Thus, current consumption increases very much. This causes Latch-up, and there is the case that, as a result, a built-in IC is destroyed. Please use an input terminal according to input voltage specifications.

Furthermore, please input the VIO or GND most recent voltage as much as possible.

(4) Handling of unused pins

Disposal of unused input terminals. When an input terminal is open state, it causes increase of a consumption electric current and the behavior that are instability. Please fix an unused input terminal to the voltage that is near to VIO or GND.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260° C, the characteristics of the crystal oscillator will be degraded and it may be damaged. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

(6) Installation of charged battery.

When a charged backup battery is installed by soldering, battery connection terminal of this device should connect to GND, beforehand.

Overview of Functions and Registers

Overview of Functions

1) Clock functions

This function is used to set and read out second, minute, hour, day, month, year (to the last two digits), and date data.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.
At the start of a IIC communication, the time and clock counting stops (which causes loss of time), and clock starts automatically again at the end of the IIC communication.

2) Wakeup Timer Interrupt function

The wakeup timer interrupt function generates an interrupt event periodically at any wakeup set between 244.14 us and 65535 hours.
When an interrupt event is generated, the /IRQ pin goes to low level and "1" is set to the TF bit to report that an event has occurred.

3) Long-Timer function

It is able to use wakeup timer interrupt function as Long-Timer or usage counter.
This function measures the operation time on the main power supply and the operation time on the backup power supply and can automatically sum them up.

4) Alarm interrupt function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.

5) Time Update Interrupt Function

The time update interrupt function generates interrupt in one-second or one-minute intervals which are synchronized to the update of the second or minute time register of the RTC When an interrupt event is generated, the /IRQ pin goes to low level and "1" is set to the UF bit to report that an event has occurred.

6) Frequency stop detection function

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss might have occurred due to a low supply voltage.

7) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin. Output could also be 1 Hz, or 1024 Hz.

8) User RAM

RAM register is read/write accessible for any data.

9) Digital offset function

The clock precision can be increased by adding a time offset.

Register Table

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	40	20	10	8	4	2	1
11	MIN	0	40	20	10	8	4	2	1
12	HOUR	0	0	20	10	8	4	2	1
13	WEEK	0	6	5	4	3	2	1	0
14	DAY	0	0	20	10	8	4	2	1
15	MONTH	0	0	0	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	MIN Alarm	AE	40	20	10	8	4	2	1
18	HOUR Alarm	AE	•	20	10	8	4	2	1
19	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1E	Control Register0	TEST	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE
1F	Control Register1	SMP TSEL1	SMP TSEL0	CHGEN	INIEN	0	RS VSEL	BF VSEL1	BF VSEL0
20 - 23	RAM	User Register 32 bits (4-word x 8 bit)							
30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1
31	Extension Register1	-	-	-	-	-	-	-	VBLFE

After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.

Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing. Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing

“0” means that writing is invalid and the read value is always 0.

Any bit marked with "•" is a RAM bit that can be used to read or write any data

User Register is a free register which can be used as user RAM.

The above table shows only the user registers. Due to functional reasons, RTC has different registers not mentioned above table which are programmed by the manufactorer. Please make sure to only access above mentioned user registers.

“-“ bit is TEST bit. As initialization “0” should be set and be kept “0”.

Register initial value and Read/Write operation Table

After power-on-reset, registers bits of RTC are configured automatically as below. The value will be the same even after Software Reset is executed.

X: Undefined in 0 or 1. usually it keeps data of before Power-On-Reset.
0: Reset state
1: Set state

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	X	X	X	X	X	X	X
11	MIN	0	X	X	X	X	X	X	X
12	HOUR	0	0	X	X	X	X	X	X
13	WEEK	0	X	X	X	X	X	X	X
14	DAY	0	0	X	X	X	X	X	X
15	MONTH	0	0	0	X	X	X	X	X
16	YEAR	X	X	X	X	X	X	X	X
17	MIN Alarm	X	X	X	X	X	X	X	X
18	HOUR Alarm	X	X	X	X	X	X	X	X
19	WEEK Alarm	X	X	X	X	X	X	X	X
	DAY Alarm		X	X	X	X	X	X	X
1A	Timer Counter 0	X	X	X	X	X	X	X	X
1B	Timer Counter 1	X	X	X	X	X	X	X	X
1C	Extension Register	0	0	0	0	0	1	0	0
1D	Flag Register	0	0	0	0	0	1	1	0
1E	Control Register0	0	0	0	0	0	0	0	0
1F	Control Register1	0	0	0	0	0	0	0	0

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20-23	RAM	X	X	X	X	X	X	X	X

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	0	0	0	0	0	0	0	0
31	Extension Register1	0	0	0	0	0	0	0	0

Note:
The initialization of the register is necessary about the unused function.

lock calendar explanation

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end. Therefore, it recommends that the access to a clock calendar has continuous access by the auto increment function.

[SEC] [MIN] register

These registers are 60-base BCD counters. These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.

When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512 Hz 1 Hz) is cleared to 0.

[HOUR] register

This register is a 24-base BCD counter (24-hour format).These registers are incremented at the timing when carry is generated from a lower register

[WEEK] register

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.

The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.

It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data h
Sunday	0	0	0	0	0	0	0	1	01 h
Monday	0	0	0	0	0	0	1	0	02 h
Tuesday	0	0	0	0	0	1	0	0	04 h
Wednesday	0	0	0	0	1	0	0	0	08 h
Thursday	0	0	0	1	0	0	0	0	10 h
Friday	0	0	1	0	0	0	0	0	20 h
Saturday	0	1	0	0	0	0	0	0	40h

Note:
Do not set "1" to more than one day at the same time.

[DAY] [MONTH] register

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is a 12-base BCD counter triggered by carryover of the day register.

[YEAR] register

This register is a BCD counter for years 00 to 99.

The leap year is automatically determined and influences the DAY register. This RTC processes following years as leap years: 00,04,08,12,,, 96.

User software correction is needed in the years 2100,2200,2300 as they are common years.

Wakeup Timer Interrupt Function

The wakeup timer interrupt function generates an interrupt event periodically at any wakeup set between 244.14 μs and 65535 hours. This function can stop at one time and is available as an accumulative timer. After the interrupt occurs, the /IRQ outputs is released in tRTN2 automatically

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	**TSEL2**	**TSEL1**	**TSEL0**
1D	Flag Register	VBLF	0	UF	**TF**	AF	RSF	VLF	VBFF
1E	Control Register0	**TEST**	STOP	UIE	**TIE**	AIE	**TSTP**	**TBKON**	**TBKE**

Before entering operation settings, we recommend first reset the TE bit to "0".
When the wakeup timer function is not being used, the wakeup Timer Counter0,1 register can be used as a RAM register. In such cases, stop the wakeup timer function by writing "0" to the TE and TIE bits.

Down counter for wakeup timer(Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1(0001h) to 65535(FFFFh)can be set.
Be sure to write "0" to the TE bit before writing the preset value. When TE=0, read out data of timer counter is default (Preset) value.
And when TE=1, read out data of timer counter is counting down value. But when access to timer counter data, counting value is not held.
Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is recommended.

TSEL2, TSEL1, TESL0 bit

The combination of these three bits is used to set the countdown period (source clock) for this function.

TSEL2 (bit 2)	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock		Auto release time tRTN2 (Min.)
0	0	0	4096 Hz	/Once per 244.14 μs	122 μs
0	0	1	64 Hz	/Once per 15.625 ms	7.57 ms
0	1	0	1 Hz	/Once per second	7.57 ms
0	1	1	1/60 Hz	/Once per minute	7.57 ms
1	0	0	1/3600 Hz	/Once per hour	7.57 ms

The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting. The first countdown shortens than a source clock.

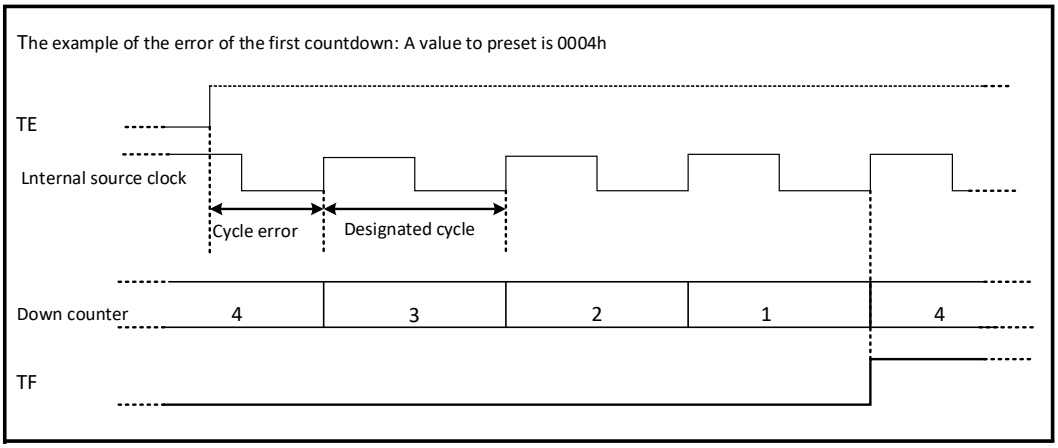


Figure 11 Wakeup timer initial sequence

When selected 4,096 Hz / 64 Hz / 1Hz as a source clock, one period of error occurs at the maximum.
When selected1/60 Hz / 1/3600 Hz as a source clock, 1 Hz of error occurs at the maximum.

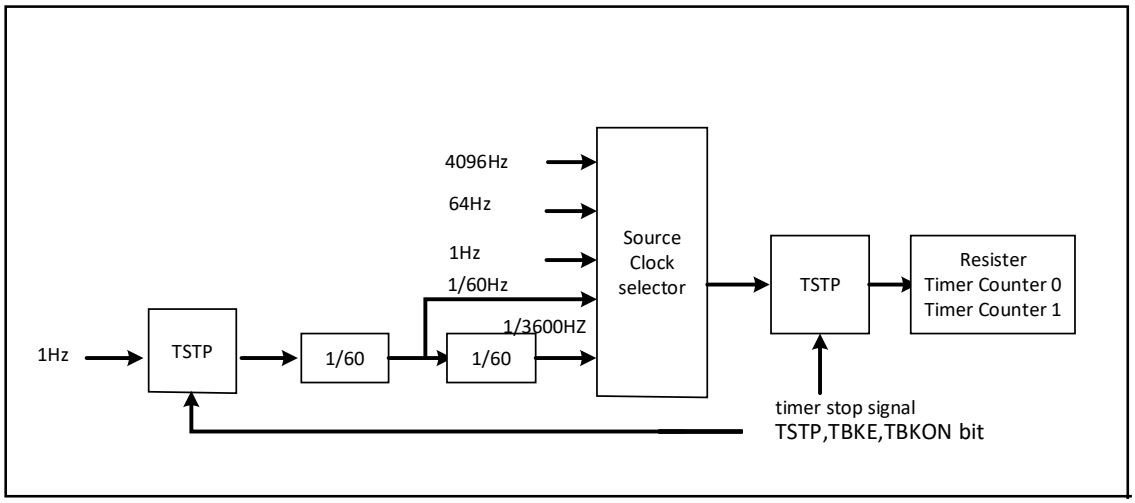


Figure 12 Wakeup timer block diagram

Note: The resolution of the count value depends on the source clock

TE bit (Timer Enable)

TE bit use for start Timer or stop.
When TE bit is "0", the preset value of the timer can be checked by reading this register.

TE	Data	Description
Write	0	The wakeup timer interrupt function is stopped. The wakeup timer interrupt output is released to Hi-Z immediately. Preset values are loaded on timer counters 0 and 1. New preset values can be set for timer counters 0 and 1.
	1	The wakeup timer interrupt function starts operating. When TE is set from 0 to 1,the timer counter starts counting down from the preset value.

TF bit (Timer flag)

This is a flag bit that retains the result when a wakeup timer interrupt event is occurred.

TF	Data	Description
Write	0	The /IRQ low output is released immediately.
	1	Invalid (writing a 1 will be ignored)
Read	0	Wakeup timer interrupt was not occurred.
	1	Wakeup timer interrupt was occurred. Result is retained until this bit is cleared to zero.

TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a wakeup timer interrupt event has occurred.

TIE	Data	Description
Write	0	Even if wakeup timer interrupt event occurs, an interrupt signal is not generated. When a /IRQ was output Wakeup timer interruption already, the wakeup timer interrupt signal is released to Hi-Z from low.
	1	When a wakeup timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes to low from Hi-z.

TBKON, TBKE bit

This function selects the operation time with the main power supply or the operation time with the backup power supply. The count value is added.

operation	TBKE	TBKON	Description
Write	0	X	This setting counts normal mode and backup mode.
	1	0	This setting counts it at time of normal mode(VDD operation)
		1	This setting counts it at time of backup mode (VBAT operation)

TSTP bit (Timer Stop)

This bit is used to stop wakeup timer count down.

TE	STOP	TBKE	TSTP	Description
1	0	0	0	Countdown is restarted. The restart value of the countdown is a stopping value
			1	Count stops.
		1	X	Setting of TSTP value becomes invalid, and the count does not stop even if set it in TSTP=1.
	1	X	X	When source clock is 64 Hz,1 Hz,1/60 Hz, 1/3600 Hz, the countdown is stopped.
0	X	X	X	The preset value is loaded to timer counter1,2. Timer count down is stopped.

Wakeup timer interrupt cycles

Timer Counter setting 1 ~ 65535	Source clock				
	4096 Hz TSEL2 = 0 TSEL1, 0 = 0, 0	**64 Hz TSEL2 = 0 TSEL1, 0 = 0, 1**	**1 Hz TSEL2 = 0 TSEL1, 0 = 1, 0**	**1 / 60 Hz TSEL2 = 0 TSEL1, 0 = 1, 1**	**1 / 3600 Hz TSEL2 = 1 TSEL1, 0 = 0, 0**
0	-	-	-	-	-
1	244.14 us	15.625 ms	1 s	1 min	1 h
:	:	:	:	:	:
410	100.10 ms	6.406 s	410 s	410 min	410 h
:	:	:	:	:	:
3840	0.9375 s	60.000 s	3840 s	3840 min	3840 h
:		:	:	:	:
4096	1.0000 s	64.000 s	4096 s	4096 min	4096 h
:	:	:	:	:	:
65535	15.9998 s	1023.984 s	65535 s	65535 min	65535 h

Diagram of wakeup timer interrupt function

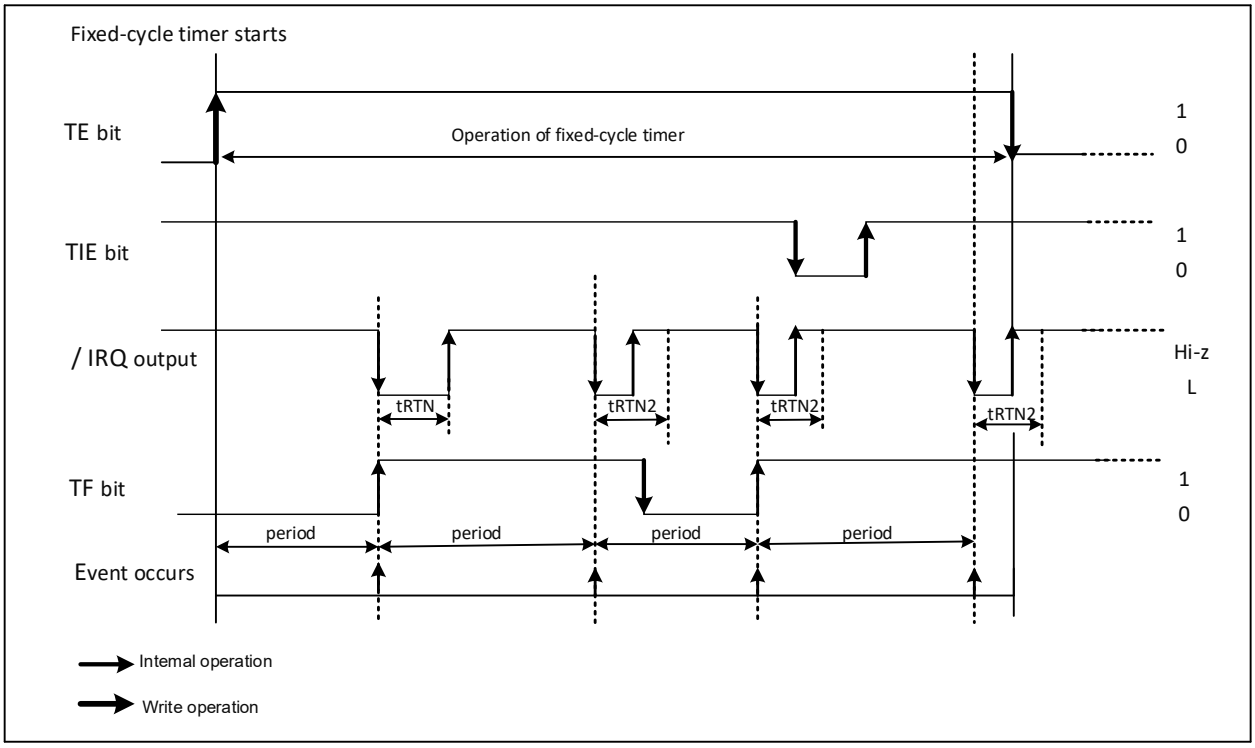


Figure 13 Wakeup timer timing chart

A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.

When a time update interrupt event occurs, the UF bit value becomes "1".

When the UF bit value is "1" its value is retained until it is cleared to zero.

When a time update interrupt occurs, /IRQ pin output is low if UIE = "1".
If UIE = "0" when a timer update interrupt occurs, the /IRQ pin status remains Hi-Z.

Each time an event occurs, /IRQ pin output is low only up to the tRTN time (which is fixed as min 7.57 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
/IRQ pin output goes low again when the next interrupt event occurs.

As long as /IRQ = low, the /IRQ pin status does not change, even if the UF bit value changes from "1" to "0".

When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred. AF bit and /IRQ output show a maximum delay of 1.46ms from the alarm event.
/IRQ="L" output when occurs alarm interruption event is not cancelled automatically unless giving intentional cancellation and /IRQ="L" are maintained.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
17	MIN Alarm	**AE**	40	20	10	8	4	2	1
18	HOUR Alarm	**AE**	•	20	10	8	4	2	1
19	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1C	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	TSEL2	TSEL1	TSEL0
1D	Flag Register	VBLF	0	UF	TF	**AF**	RSF	VLF	VBFF
1E	Control Register0	TEST	**STOP**	UIE	TIE	**AIE**	TSTP	TBKON	TBKE

Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

When the STOP bit value is "1" alarm interrupt events do not occur.

When the alarm interrupt function is not being used, the Alarm registers (Reg – 17h to 19h) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

When the AIE bit value is "1" and the Alarm registers (Reg – 17h to 19h) is being used as a RAM register, /IRQ may be changed to low level unintentionally.

AE bit

The minute, hour, day and date when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg – 19h), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.

AE-bit is low active, so in order to enable 1 interrupt every hour once the actual minutes match the alarm setting, it is necessary to set the AE of register 17h to 0 and the AE of 18h and 19h to 1.
In order to generate an alarm interrupt only once a week, all 3 AE-bits have to be set"0

1) The alarm function is not a HW feature but software function inside the RTC.

2) In case "AE" bit of register 19h is set to "1", the day will be ignored, and an interrupt occurs ones the actual time matches the minutes and/or hour setting of the alarm register.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 19h):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as

alarm comparison targets.
As a result, alarm occurs if only the hour and minute values match the alarm data.

3) If all three AE bit values are "1" the week/date and time settings are ignored, and an alarm interrupt event will occur once per minute.

WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-z) when an alarm interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)
Read	0	-
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when an Alarm interrupt event has occurred.

AIE	Data	Description
Write	0	When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-z). When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

The AIE bit is only output control of the /IRQ terminal. It is necessary to clear an AF flag to cancel alarm.

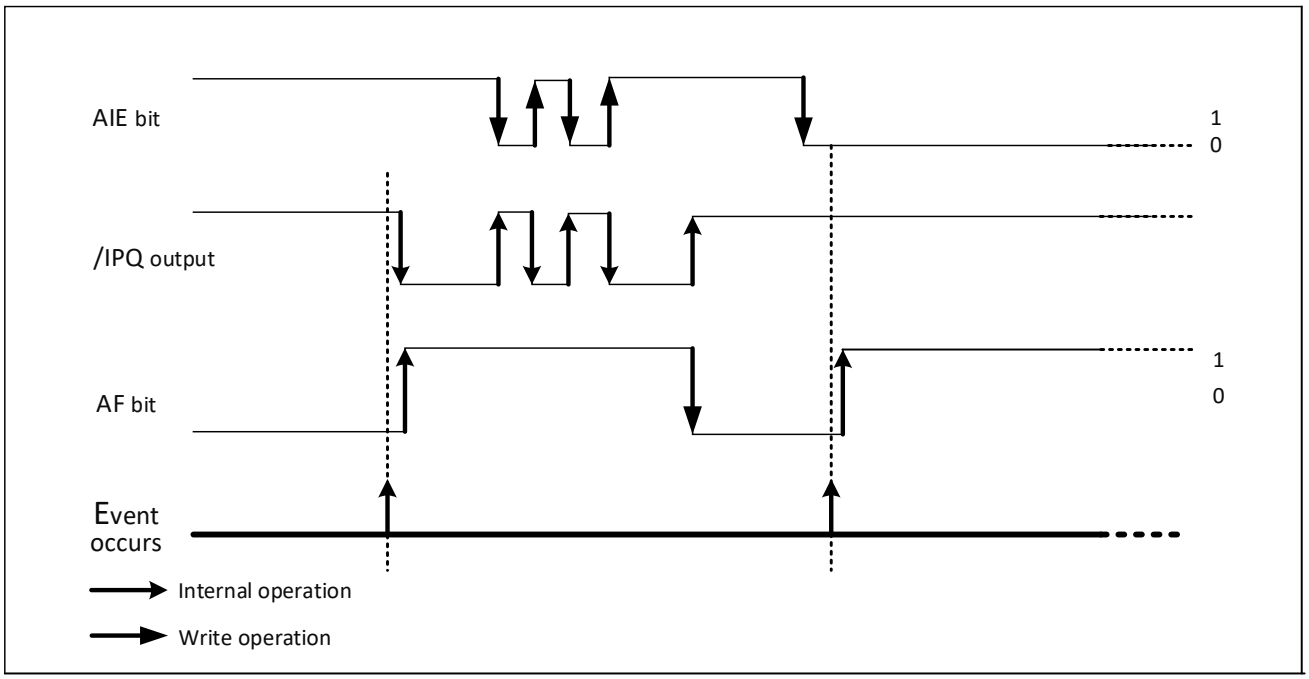


Figure 14 Alarm Interrupt time chart

Time Update Interrupt Function

The time update interrupt function generates interrupt in one-second or one-minute intervals which are synchronized to the update of the second or minute time register of the RTC When an interrupt event is generated, This /IRQ status is automatically cleared (/IRQ status changes from low level to Hi-z earliest 7.57ms (maximum 15.63ms) after the interrupt occurs). This time width is auto release time (tRTN1).

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1C	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	TSEL2	TSEL1	TSEL0
1D	Flag Register	VBLF	0	**UF**	TF	AF	RSF	VLF	VBFF
1E	Control Register0	TEST	STOP	**UIE**	TIE	AIE	TSTP	TBKON	TBKE

Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
When the STOP bit value is "1" time update interrupt events do not occur.
Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ pin status to low.

USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

UF bit (Update Flag)

This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

UF	Data	Description
Write	0	Clear this bit to zero enables /IRQ low output of time update to be canceled immediately when a time update interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored
Read	0	-
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

UIE	Data	Description
Write / Read	0	Does not generate an interrupt signal when a time update interrupt event occurs. Cancels interrupt signal triggered by time update interrupt event. Even when the UIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a time update interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). When a time update interrupt event occurs, low-level output from the /IRQ pin occurs only when the UIE bit value is "1". Earliest 7.57 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low to Hi-Z).

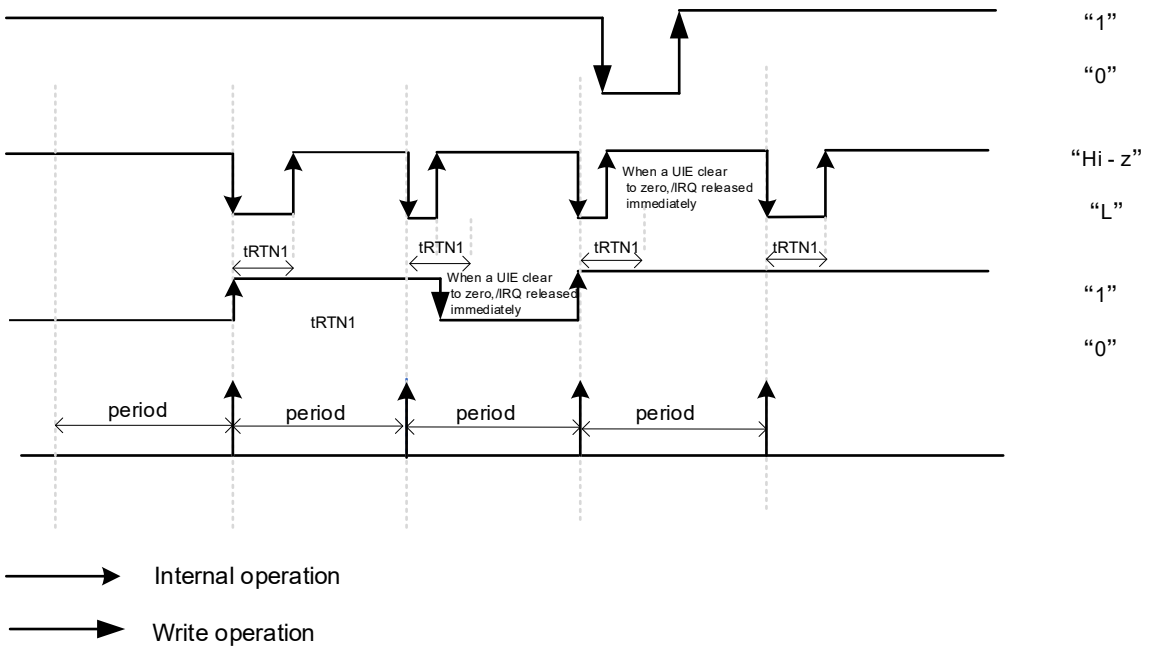


Figure 15 Time update time chart

Oscillation stop detection function

This flag bit indicates the retained status of clock oscillation stop. Its value changes from "0" to "1" when data loss might have occurred due to clock oscillation stop, power on resetting. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
During the initial power-on (from 0 V) and/or if the value of the VLF bit is "1", be sure to initialize all registers before using them.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	**0**	UF	TF	AF	RSF	**VLF**	VBFF

VLF	Data	Description
Write	0	The VLF is cleared to 0 and waiting for next low voltage detection.
	1	Invalid (writing 1 will be ignored)
Read	0	Oscillation status is normal, RTC register data are valid.
	1	Oscillation stop is detected, RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

FOUT function

The clock signal can be output via the FOUT pin. Output is stopped upon detection of the voltage drop below VDET1In this case pin output becomes Hi-z.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1C	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	TSEL2	TSEL1	TSEL0

FSEL1	FSEL0	output
0	0	32.768 kHz Output
0	1	1024 Hz Output
1	0	1 Hz Output
1	1	OFF

At the time of the initial power-on, “0” is set to FSEL1, FSEL0 by Power-On-Reset.

Note: The effect of STOP bit to FOUT functions.
When STOP = "1", 32.768 kHz and 1024 Hz output is possible. But 1 Hz output is disabled.

Battery backup switchover function

Description of Battery backup switchover function

This function consists of a supply voltage detector "VDET" which detects if the supply voltage of the main power source connected to "VDD" drops below a threshold (VDET2), and three MOS switches (SW1,SW2A and SW2B) located between the main power-source pin "VDD" and the backup power supply pin "VBAT". (Figure 26 Battery backup switchover block diagram)

The MOS-switches SW1, SW2A and SW2B are activated according to the result of the supply-voltage detection of VDET2 and the RTC changes the operating modes between normal mode (RTC power supply = VDD) or backup mode (RTC power supply = VBAT).
The RTCs backup function is built in a way to prevent reverse current flow from VBAT to VDD. While in backup- mode, the IIC-bus and FOUT function are switched off and related terminals switched to Hi-Z.
The figure below shows the switch status after power-on reset in the image of the power switching circuit.

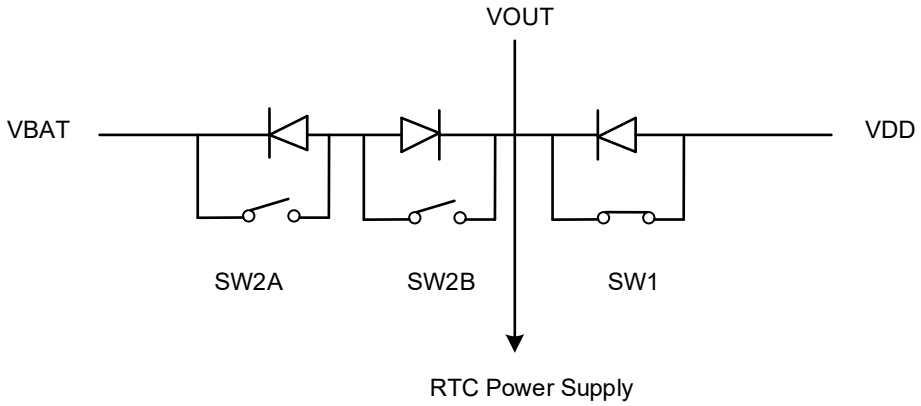


Figure 16 Battery backup switchover block diagram

Default power switch state

The figure above shows the state of the power switch after power-on reset. SW1: Always ON
SW2A: Always OFF SW2B: Always OFF
VDET2 voltage monitoring: Always OFF, power supply is not switched, power source is only VDD power supply.

Reference characteristics of switching elements.

Item	Value	Condition
Limit of current.	40 mA Max.	SW1 = SW2A = SW2B = ON, +25 °C
Diode Vf Vf / Sink Current	0.40 V / 1μA Typ. 0.70 V / 1 mA Typ. 0.9 V / 10 mA Typ.	+25 °C
Diode IR	5 nA Max.	VR = 5.5 V, -40 °C ~ +85 °C

When using a secondary battery, EDLC, Please keep charge current 40 mA or less.

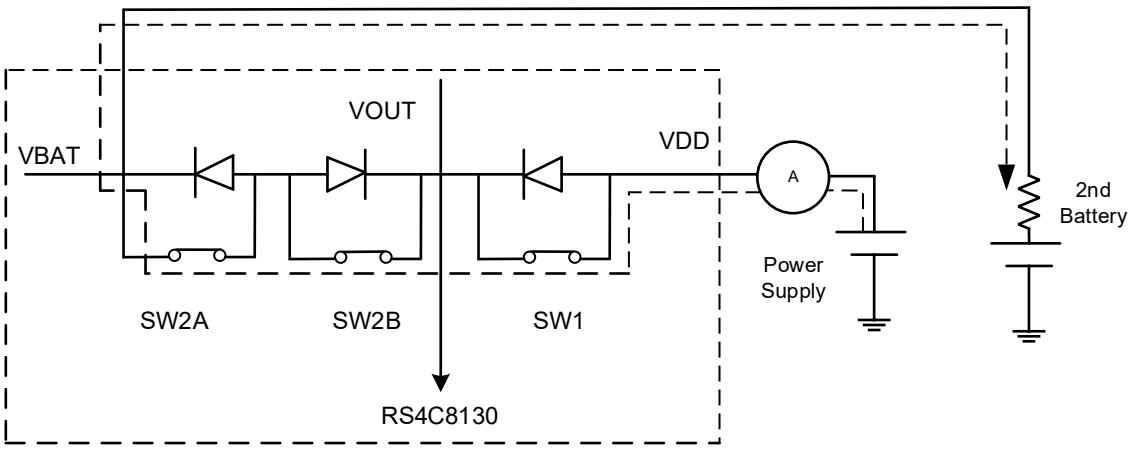


Figure 17 Re-chargeable battery connection

Related register of Battery backup switchover function

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	**VBLF**	0	UF	TF	AF	RSF	VLF	**VBFF**
1F	Control Register1	**SMP TSEL1**	**SMP TSEL0**	**CHGEN**	**INIEN**	**0**	**RS VSEL**	**BF VSEL1**	**BF VSEL0**

CHGEN bit

This bit has to be set to allow charging of a Re-chargeable battery connected to VBAT from VDD pin.

CHGEN	Data	Description
Write / Read	0	For non-re-chargeable battery use (default setting). During VDD drive SW2 is OFF, battery charging is not available.
	1	SW1, SW2 automatic controlled. For re-chargeable battery use

INIEN	Data	Description
Write / Read	0	Make sure that the IIC interface does not reach an intermediate potential. The power switching function is not operating in the 0 state due to power-on reset. If this bit is set to 1 even once, the power switching function will start operating. After that, the power switching function continues to operate even if this bit is cleared to zero.
	1	IIC, FOUT function is not available while VDD < VDET1. IIC, FOUT function is available while VDD > VDET1. CHGEN bit function is enabled.

Note:

1、When used with power-on reset INIEN = 0, power switching is stopped and the power source is fixed to VDD pin. Therefore, it is recommended to set "INIEN = 1" at least once.When the INIEN bit is set to 1, the power switching circuit is initialized and stabilized in the optimum state.

2、Setting INIEN from 0 to 1 with VDD <VDET1 disables IIC and FOUT outputs immediately.Therefore, IIC cannot clear INIEN to 0 while VDD <VDET1.In such cases, leave the INIEN bit at 0 from power on reset..

However, the power source is fixed to VDD-pin because the power switching function is stopped.

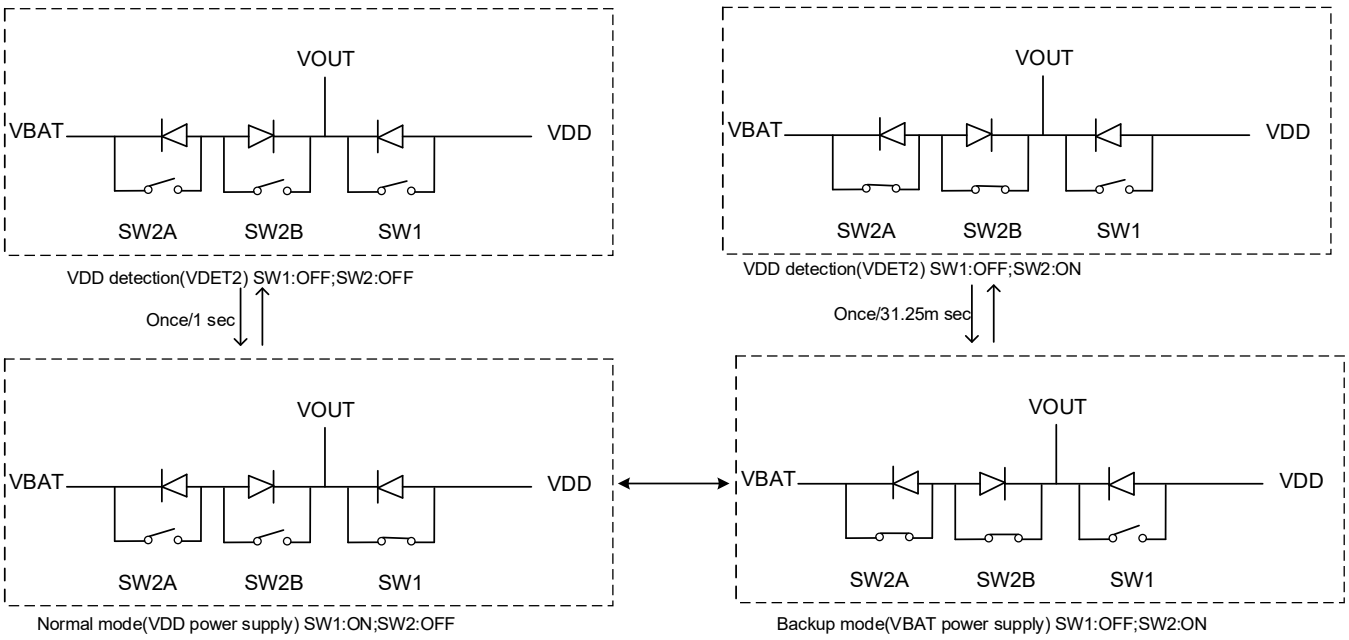


Figure 18 Non re-chargeable battery SW1, SW2 control (INIEN:1, CHGEN:0)

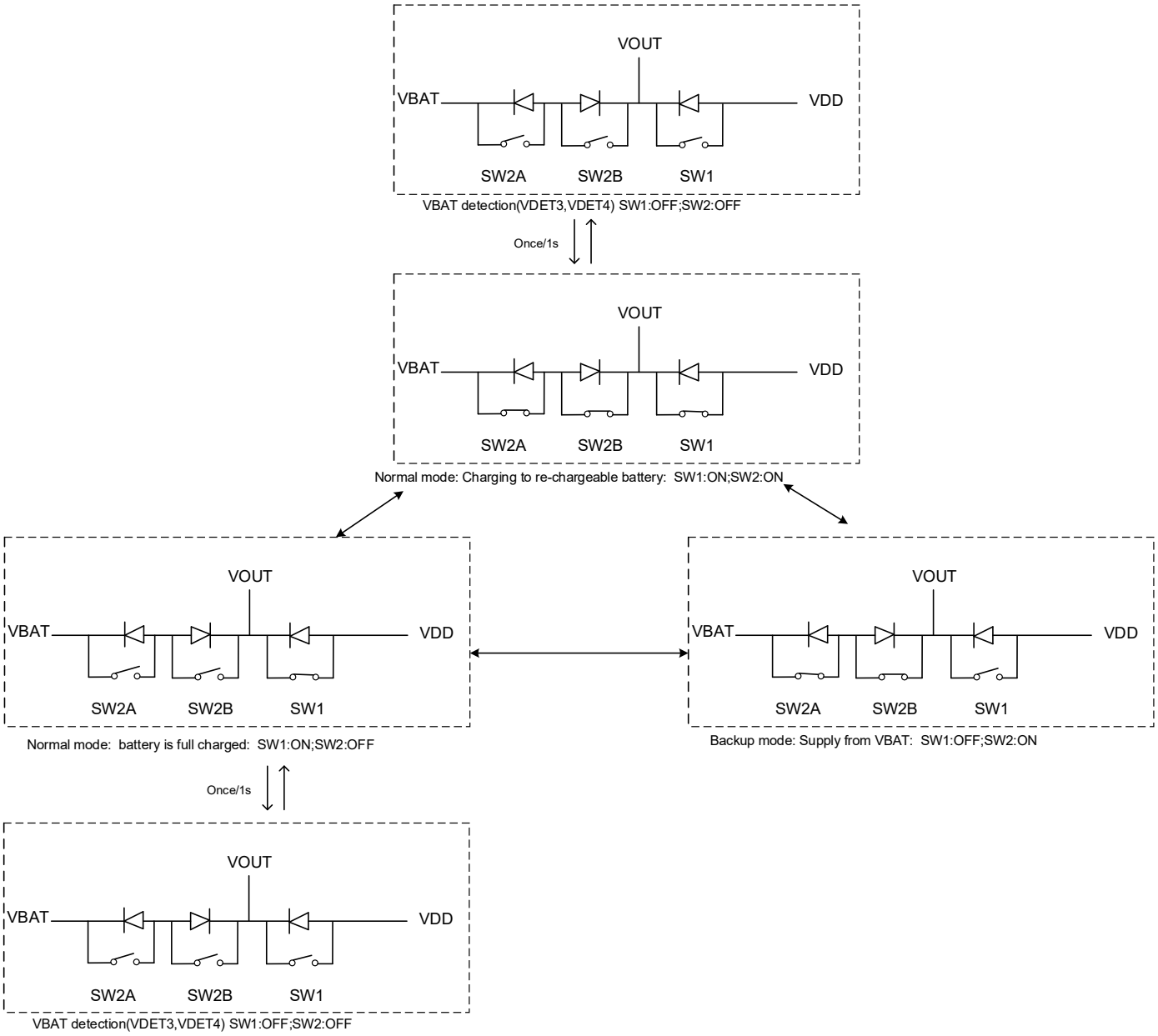


Figure 19 Re-chargeable battery SW1, SW2 control (INIEN = 1, CHGEN = 1)

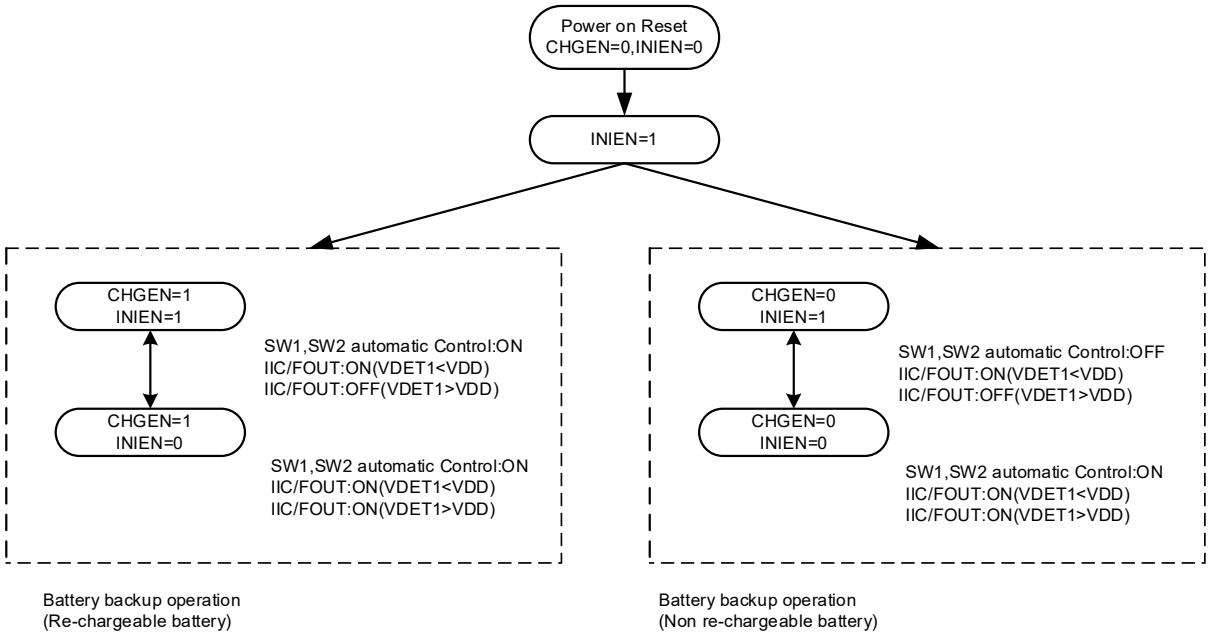


Figure 20 Battery backup (SW1, SW2 automatic control)

SMPTSEL1, SMPTSEL0 bit

VDD voltage detection: VDET1 (reset), VDET2 (voltage down):
Battery backup detection (VDET2) is done constantly and SW1 is opened periodically for VDD measurement. During SW1:ON, external voltage to VDD cannot be measured precisely because RTC internal voltage is leaked to VDD external voltage supply circuit even external circuit is down. So periodical SW1 = OFF makes disconnection between RTC internal voltage and external voltage supply, thus VDD external voltage is measured precisely. VDD external voltage drop moves to backup mode.

VBAT voltage detection: VDET3 (VBAT full charge), VDET4(VBAT over discharge)
In case of normal mode, VBAT voltage is precisely and periodically detected with condition (SW1 OFF, SW2 OFF). The detection period is determined by combination of SMPTSEL1, SMPTSEL0.

(In case of CHGEN = 0, There is no charge operation SW2 = OFF)

Voltage detection timing

Power supply mode	Normal mode (Backup battery is charging)	Normal mode (Backup battery is fully charged)	Normal mode (After return from backup VDET1>VDD>VDET2)	Backup mode
Reset detection VDD < VDET1	Constantly ON	Constantly ON	Constantly ON	Constantly OFF
Power switching detection VDD < VDET2	Constantly ON	Constantly ON	Constantly ON	Once/31.25 ms
Full charge detection VBAT > VDET3	Once/1.0 s	Once/1.0 s	Once/1.0 s	Constantly OFF
Low-VBAT detection VDD < VDET4	Once/1.0 s	Once/1.0 s	Once/1.0 s	Constantly OFF

Note:
In normal mode, when operating the RTC on VDD-supply, SW1 has to be opened (Off) to perform the VDD voltage detection for below mentioned times.

VDET3,VDET4 intermittent detection period

Power supply operation mode SMPTSEL1,0		VDD operation (Backup battery is charging)	VDD operation (Backup battery is fully charged)	VDD operation (After return from backup VDET1>VDD>VDET2)
SW1 Off time. *	00b (default)	2 ms	2 ms	2 ms
	01b	16 ms	16 ms	2 ms
	10b	128 ms	128 ms	2 ms
	11b	256 ms	256 ms	2 ms

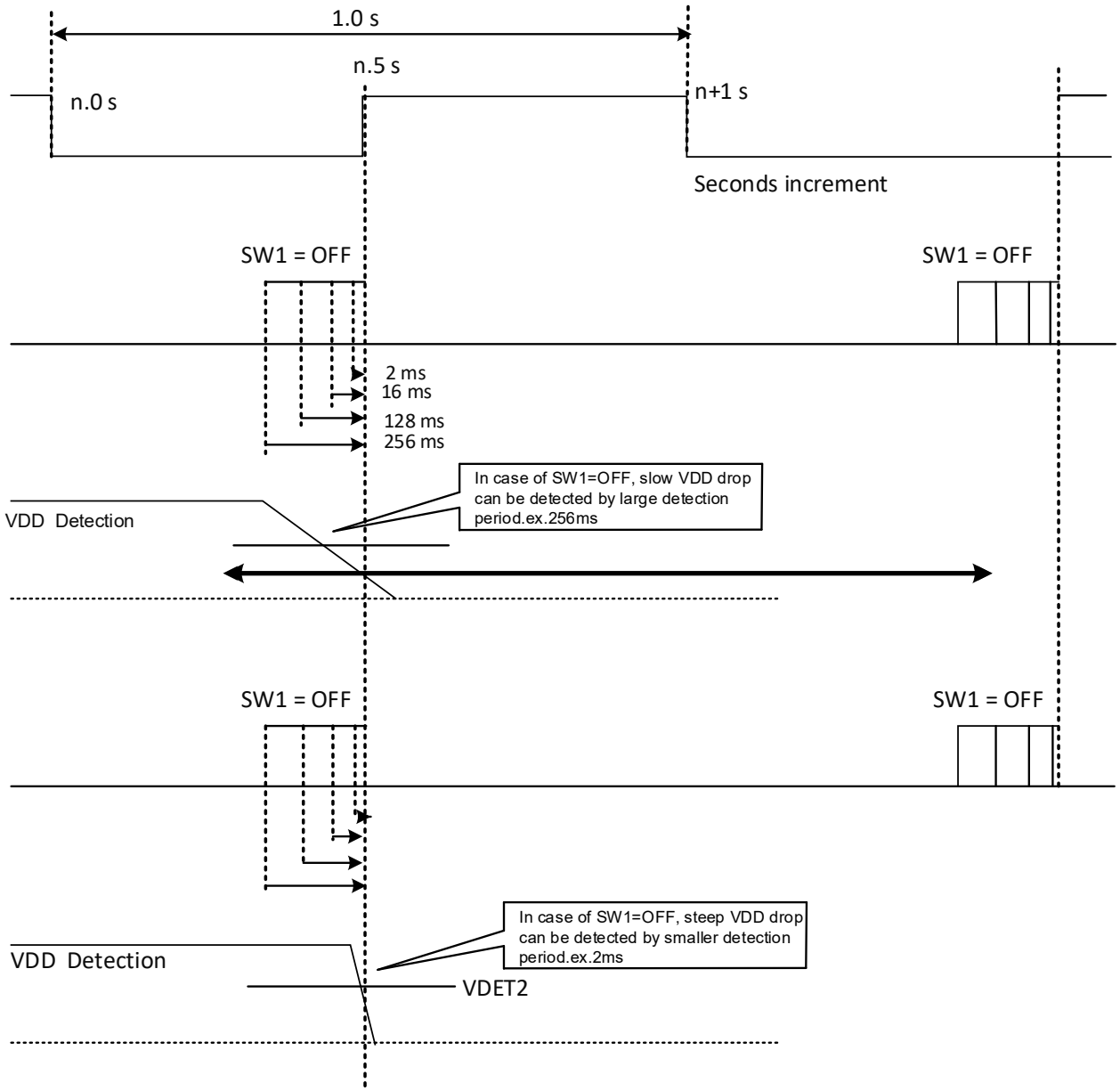


Figure 21 VDD detection (VDET2) timing

VDD voltage drop detection VDET2 is work always in Normal mode.
Shorter SW1:OFF times are suitable to detect fast external voltage drops on VDD. On the other hand, in order to detect a slower external voltage drop on VDD, a longer SW1:OFF detection time is needed. But longer SW1:OFF period increases the current consumption.
Users are requested to evaluate SW1:OFF period based on actual system configuration and characteristics. In backup mode VDD detection (VDET2) is activated once every 31.25 ms.
Note: Re-chargeable battery is charged through diode during1 the term of SW1 = OFF. Longer this term (ex. 256 ms) makes decreasing battery charging efficiency.

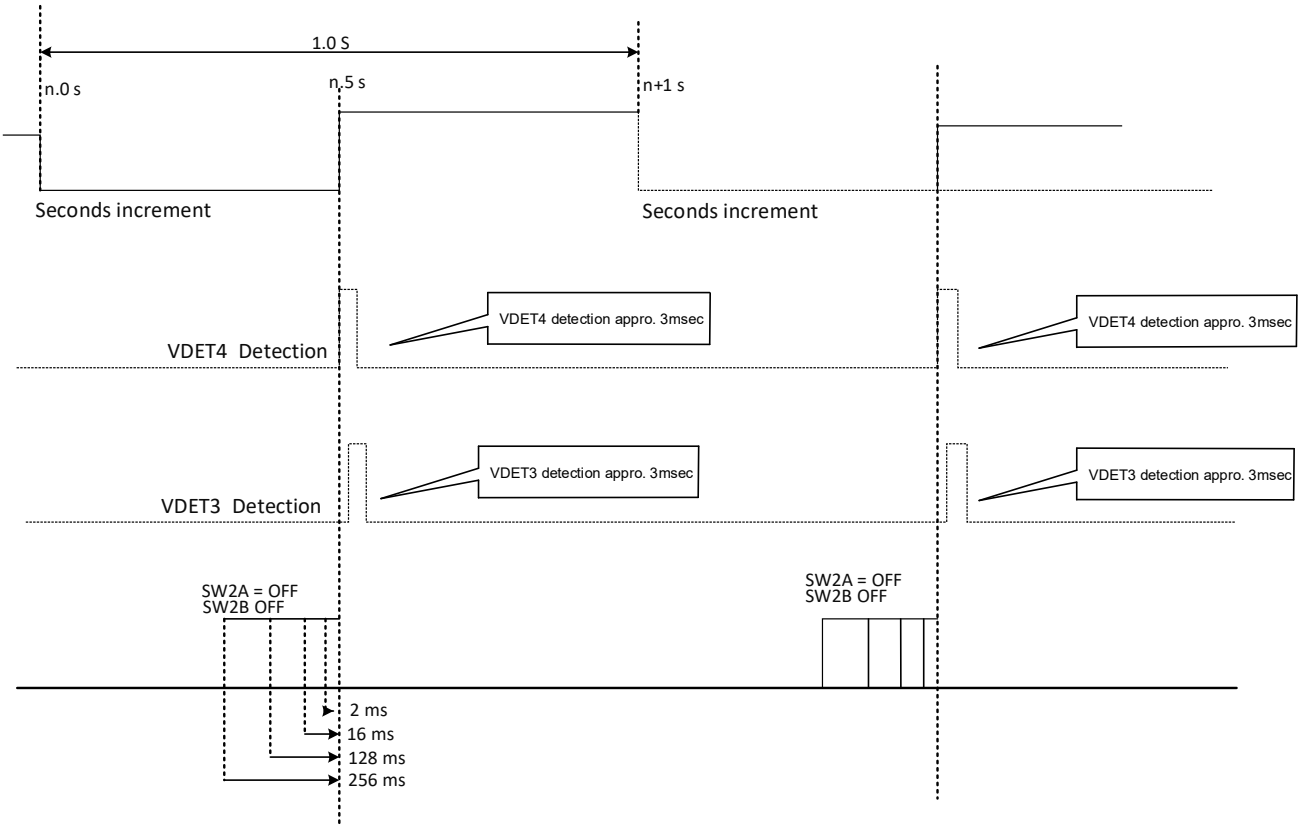


Figure 22 VDET3, VDET4 voltage detection timing) BFVSEL1, BFVSEL0 bit

Detection voltage setting

	Item	Symbol	Detect voltage Typ.	setting
V_{DET1}	Reset /Reset-release voltage	$+V_{DET11}$ / $-V_{DET11}$	2.8V / 2.75V	RSVSEL = 0 (default)
		$+V_{DET12}$ / $-V_{DET12}$	2.7V / 2.65V	RSVSEL = 1
V_{DET2}	Backup switchover/recover voltage	$+V_{DET2}$ / $-V_{DET2}$	1.35V / 1.30V	
V_{DET3}	Full charge detection voltage	$+V_{DET31}$ / $-V_{DET31}$	3.02V / 2.97V	BFVSEL = 00b default)
		$+V_{DET30}$ / $-V_{DET30}$	2.92V / 2.87V	BFVSEL = 01b
		$+V_{DET32}$ / $-V_{DET32}$	3.08V / 3.03V	BFVSEL = 10b
V_{DET4}	V_{BAT} low-voltage detection voltage	$-V_{DET4}$	2.4V	

BFVSEL1	BFVSEL0	Description
0	0	3.02 V (default)
0	1	3.08 V
1	0	2.92 V
1	1	OFF (Charging without limit)

VBFF bit

This bit indicates if the battery if fully charged (update Every 1sec)

VBFF	Data	Description
Read	0	Charging
	1	Full charge of VBAT detected (voltage level defined by BFVSEL-bit is reached)

VBLF bit

Low VBAT detection

VBLF	Data	Description
Write	0	Cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)
Read	0	-
	1	Low-VBAT has been detected (VDET4)

VBLFE bit

VBLFE	Data	Description
Write	0	CHGEN=0,VBLF detection not available
		CHGEN=1,VBLF detection available(during normal mode re-chargeable battery l)
	1	During VDD supply ,VBLF detection available

To use VBLF detection, it must be set up "INIEN=1" before the setting once at least, and VBLFE bit setting. During normal mode (VDD drive) VBAT low voltage (Non-rechargeable, rechargeable battery) can be detected. In case of backup mode VBLF function is not available, VBLF is detected after returning to normal mode.

STOP bit function

When STOP=1, in backup-mode, 31.25ms period of VDET2 detection stops.

As a result, power supply switching becomes insufficient, and there is the possibility that a leak current occurs. When STOP=1 and shift to backup-mode, clear the STOP bit to 0 after VDD-ON immediately.

Power supply control

By setting battery backup registers (INIEN, CHGEN), the RS5C8130Boperates like following either in re- chargeable battery or non-re-chargeable battery operation.

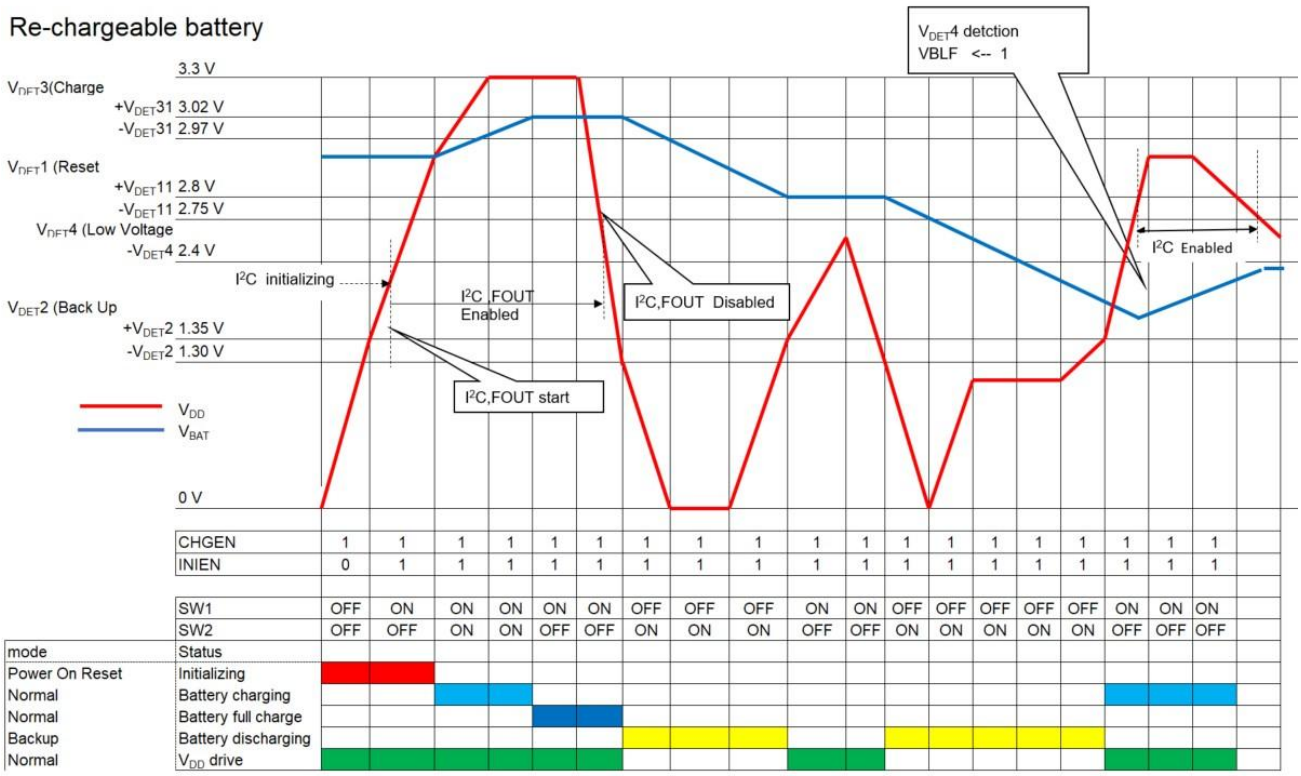


Figure 23 Re-chargeable battery operation

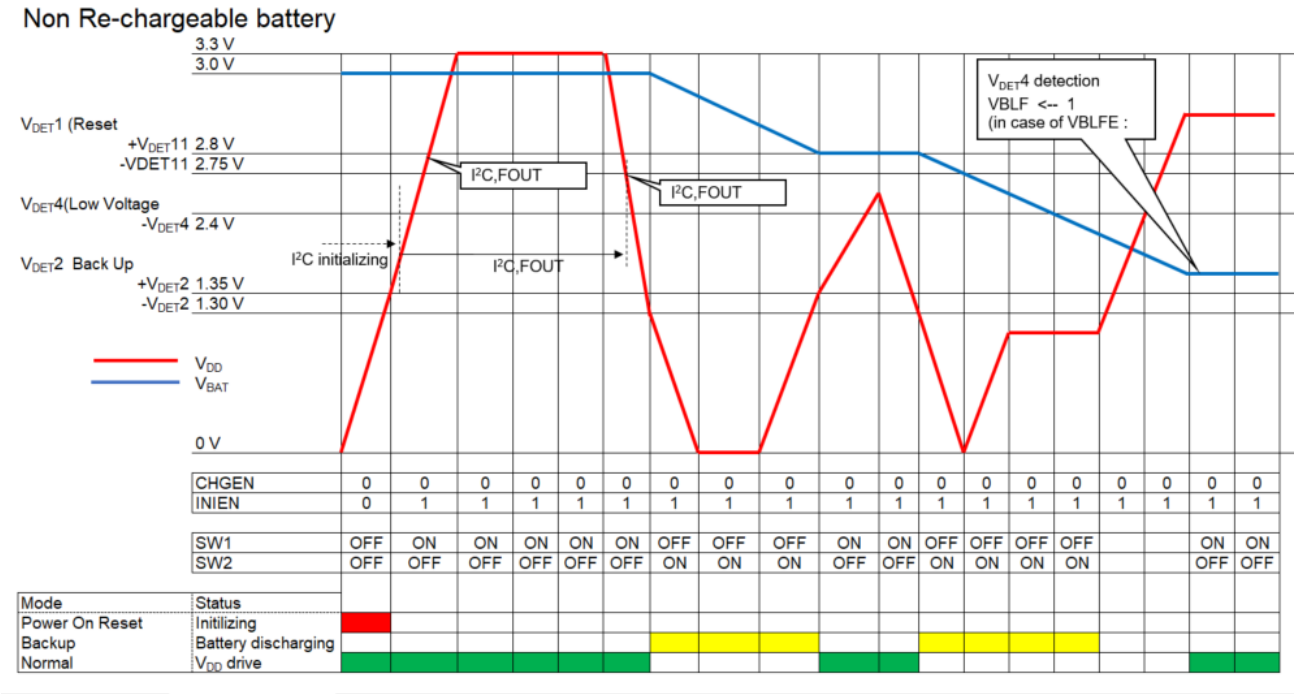
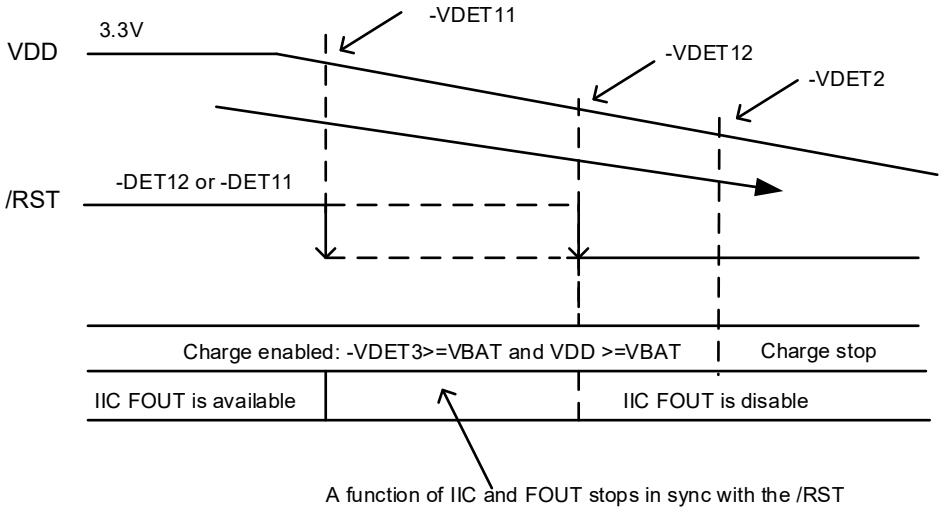


Figure 24 Non re-chargeable battery operation

Backup power supply (V_{BAT}) voltage and a charge state

1) In case of a voltage drop



2) In case of a voltage rise

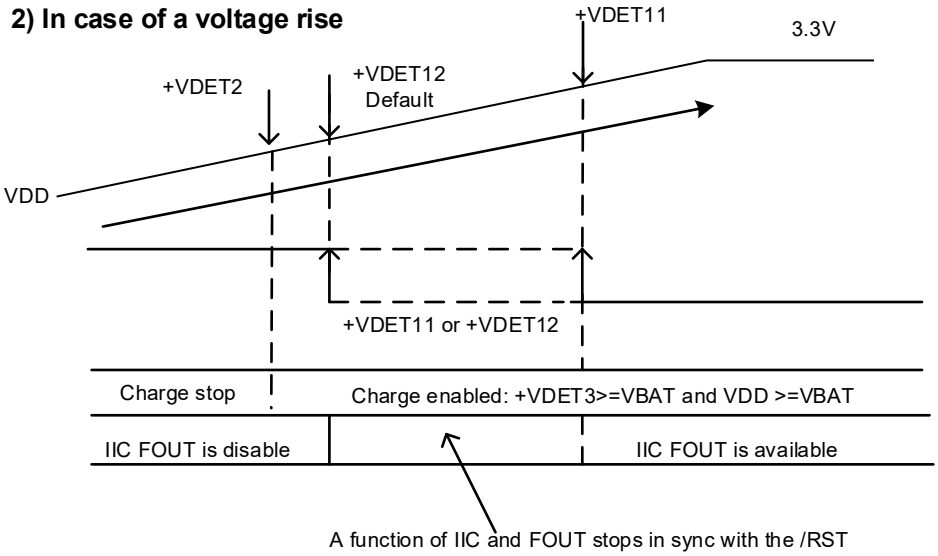
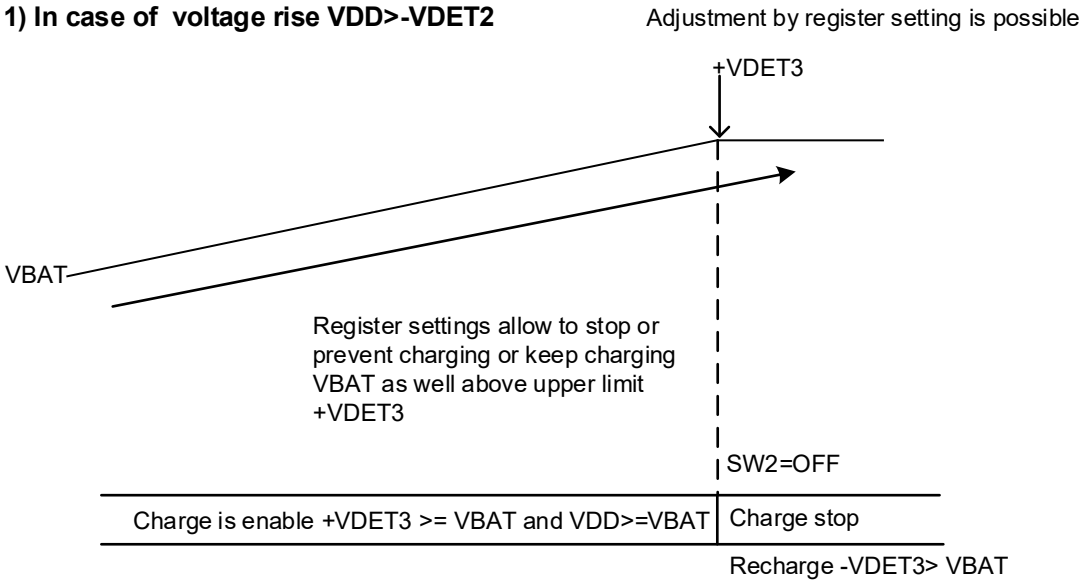


Figure 25 IIC, FOUT operation during voltage drop and rise

Backup power supply (VBAT) voltage and a charge state

1) In case of voltage rise VDD>-VDET2



2) In case of voltage drop VDD>+VDET2

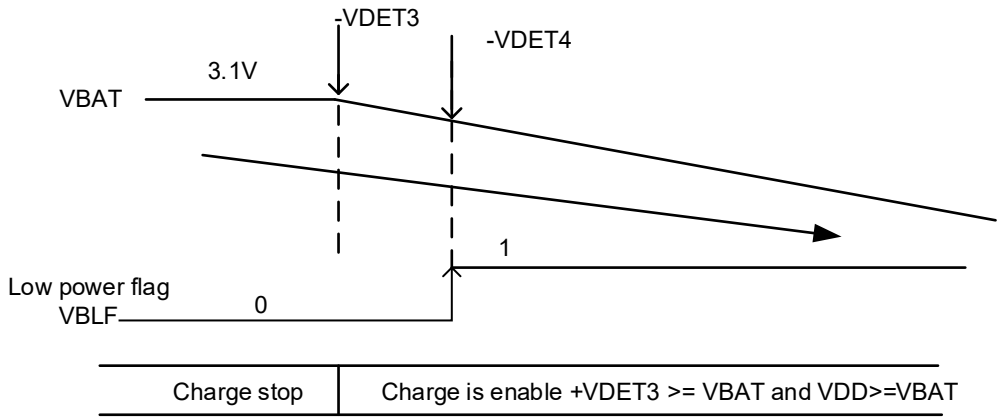


Figure 26 Re-chargeable battery operation during voltage rise and down

Reset output function

This RTC has a built-in Reset-Controller, which outputs a Reset-signal on the /RST-pin to control external HW like MCUs in case of a drop in supply voltage. When the VDD voltage drops below VDET1 (register selectable VDET11 or VDET12), a /RST-signal is output. Once VDD raises beyond VDET1 voltage again, the /RST-signal is released.
In case INIEN bit is set to "1", IIC and FOUT are stopped when VDD drops below VDET1.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	**0**	UF	TF	AF	**RSF**	VLF	VBFF
1F	Control Register1	SMP TSEL1	SMP TSEL0	CHG EN	INIEN	**0**	**RS VSEL**	BF VSEL1	BF VSEL0

RSVSEL-bit

Setting of VDET1 voltage level. In case VDD drops below this level, the /RST-signal is output and the I/F and FOUT output are stopped (depending on INIEN-bit setting).

RSVSEL	Data	Description
Write / Read	0	-VDET11 (2.75 V) (default)
	1	-VDET12 (2.70 V)

RSF-bit

This bit holds the result of detecting the reset voltage.

RSF	Data	Description
Write	0	The RSF is cleared to 0 and waiting for next low voltage detection.
	1	Invalid (writing a 1 will be ignored)
Read	0	-
	1	A voltage drops below -VDET1 was detected.

Digital offset function

With this function it is possible to increase or decrease the speed of the time counting and thus put a positive or negative offset to the clock precision. The adjustment range for this offset correction is $+192.3\times10^{-6}$ to -195.3×10^{-6} in steps of 3.05×10^{-6}.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1

DTE="1" enables the digital offset function.

When the digital offset function is enabled, the digital offset register digitally offsets the sub-second clocks according to the values set in the digital offset register. This correction of the second time register occurs every 10 seconds and the level of correction depends on the offset required. When outputting a 32.768 kHz signal on FOUT-pin , this function has no influence, since the oscillation frequency of the built-in crystal does not change by using this function. In case

of outputting a 1 Hz or 1024 Hz signal on FOUT, the offset correction will cause a certain jitter on the clock signal. Alarm function as well as the Wakeup Timer function (if source clock lower than 4096 Hz is selected) are affected by this function.

In order to disable the digital offset function, set to DTE = ”0”. In this case the L1 to L7 are ignored.

Below table shows the relationship of the L7~L1 bit and the digital offset value
When the L7 bit = “0”, the offset is positive (clock runs faster), when the L7 bit = “1”, the offset is negative (the clock runs slower).

Digital offset bits							Offset value
L7	L6	L5	L4	L3	L2	L1	(× 10^{-6})
0	1	1	1	1	1	1	+192.26
0	1	1	1	1	1	0	+189.21
:							:
0	0	0	0	0	1	0	+6.10
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0.00
1	1	1	1	1	1	1	–3.05
1	1	1	1	1	1	0	–6.10
:							:
1	0	0	0	0	0	1	–192.26
1	0	0	0	0	0	0	–195.31

How to calculate the offset value

1) When the offset value is positive:
L [7 ~ 1] =[Offset Value]/ 3.05 However, decimals are discarded.
Example calculation: When the offset value is +192 × 10^{-6}
L[7 ~ 1] = 192.26 / 3.05 = 63 (Dec)
= 0111111(bin) is set.

2) When the offset value is negative:
L[7 ~ 1] = 128 – [Offset Value] / 3.05
However, decimals are discarded.
Example calculation: When the offset value is –158 × 10^{-6}
L[7 ~ 1] = 128 - (158 / 3.05) = 76(Dec) = 1001100(bin) is set.

3) When calculate from accuracy of a clock
To adjust 30 seconds in 30 days:
Example calculation: 30sec. / 2592000s (30days) = 11.57 × 10^{-6}

Positive offset
L[7 ~ 1] = 11.57 / 3.05 = 4 (Dec) However, decimals are discarded.
= 0000100(bin) is set.

Negative offset
L[7 ~ 1] = 128 – (11.57 / 3.05) = 124 (Dec) However, decimals are discarded.
= 1111100(bin) is set.

Effect of the digital offset function to other functions

Because this function adjusts an internal sub-second clock, this function affects the a Wakeup timer interrupt function and FOUT function

1) FOUT function
1 Hz setting: Once in 10 seconds, the 1 Hz period fluctuates.
1024 Hz setting: Once in 10 seconds, the 1024 Hz period fluctuates.
There are cases where there is no fluctuation, depending on the offset correction value.
32.768 kHz: Not affected.

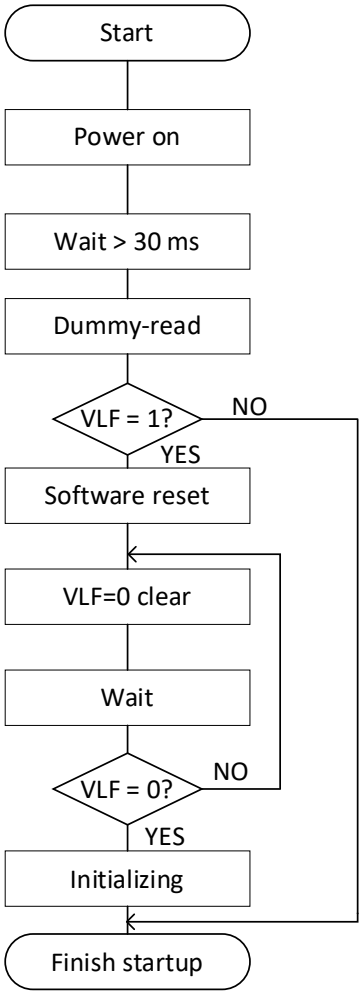
2) Wakeup timer interrupt function

64 Hz or 1 Hz source clock setting: Once in 10 seconds, the period fluctuates.
When the timer intervals are long, the fluctuations appear small.
4096 Hz source clock setting: Not affected.

Flow-chart

The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

Initializing example



At least 30 ms wait time is needed. So that it is stable RTC. 40 ms is not oscillation startup time

When the power supply conditions for which Power-On Reset is executed cannot be satisfied, then must be execute a Dummy-read.
Dummy read is one time read access to a free address Ignore ACK / NACK from RS4C8130CE in Dummy-read.

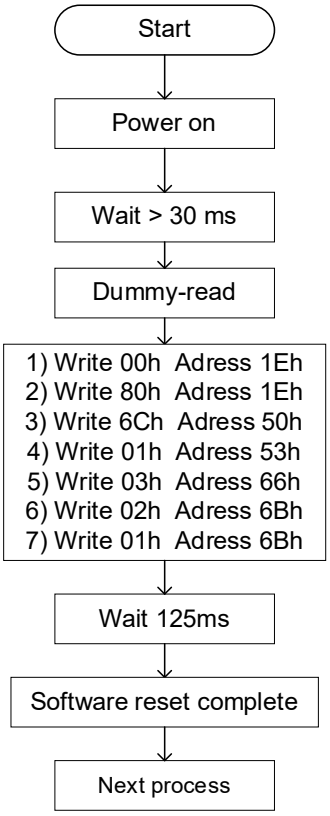
Judge RS4C8130CE returned from backup normally, or fail.

When the power conditions for which the power-on reset is executed are not satisfied, execute a software reset.

VLF cannot be cleared to 0 until internal oscillation starts. Set any waiting time

Set the maximum number of loops, for an trouble of crystal oscillation

Software Reset



In a dummy lead, ignore NACK/ACK from RTC

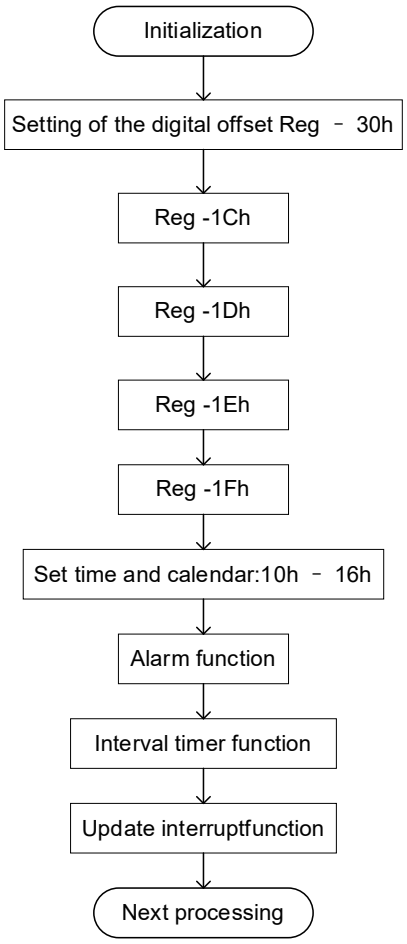
It has possibility leak current occurs from step 3) to step 7). because all power switch are turned to ON while this. After step 2), please complete the process immediately.

TEST bit is cleared automatically in step 7.

Both time and a calendar register are not initialized in any values by this Software Reset.
Both a calendar and Time before reset are maintained.

/RST signal outputs Low 95ms Max from step7.
Please care /RST active signal. And a VLF bit is set to
Please clear VLF to 0.

Example of Initialization routine



When the digital offset function is not being used, write 0 in the DTE bit

Clear TE bit to “0”.
Set FSEL1, 0 bit optionally

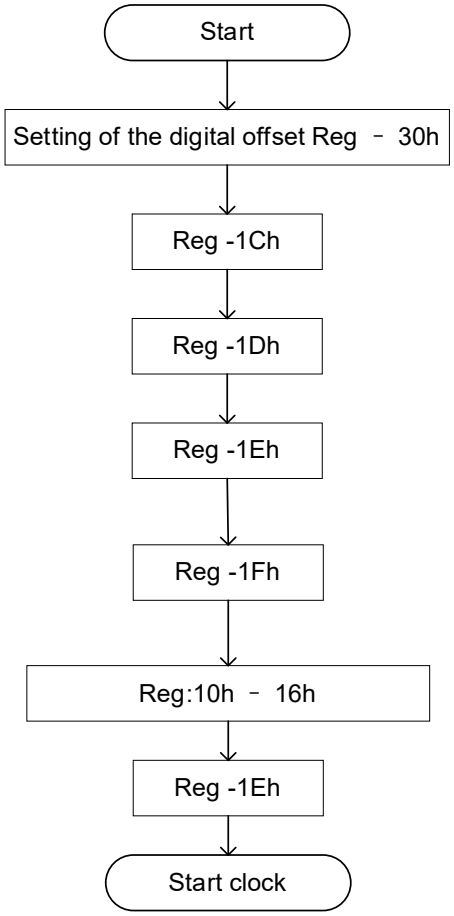
Clear VLF bit to “0”.
State of VLF=1 is held even if it 0 clear until oscillation start. When initialize it without waiting for an oscillation start, Clear VLF bit after an oscillation start.
Clear TEST bit to 0.
Clear AIE, TIE, UIE for inhibit interrupt output of suddenness
Set INIEN to 1.
When it is used in INIEN=0, please set it in INIEN=0 again after setting INIEN to 1 once. Also refer INIEN bit.

Set the present time.

Configure the Alarm interrupt function.
When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
Configure the interval timer function.
When the interval Timer function is not being used, the Timer Counter register can be used as a RAM register. In such cases,
stop the interval timer function by writing "0" to the TE and TIE bits.
Configure the Update interrupt function.

When initialization is finished, be sure to set STOP bit to “0”

Example of Initialization routine (only clock usage)



Setting value 04h

Setting value 00h
start of VLF=1 is held even if it0 clear until oscillation start.
When initialize it without waiting for an oscillation start,clear VLF bit after an oscillation.

Setting value 40h
Set STOP bit to 1 prevent timer update in time setting

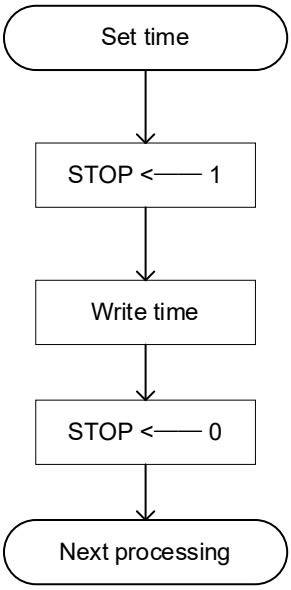
Value for using primary battery :setting value 10h
Value for using capacitors and secondary batteries that don’ t require charge control: setting value 33h

Set the present time.

Setting value 00h
Timer update starts by clearing the STOP bit to 0

When initialization is finished, be sure to set STOP bit to “0”

The setting of the clock and calendar



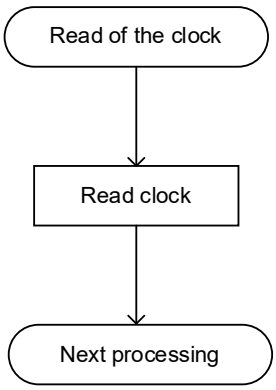
Set STOP bit to “1” to prevent timer update in time setting

Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset).
In case of initialization, please initialize all data.

Write 0 to STOP-bit for restart clock updating. Clock is started at the time.

It is able to set time even if not combined use of STOP bit.
Please note that [clock is started at the time of writing [second]] in case STOP bit is not used.
While STOP = 1, please be aware that the functions such as the voltage detection function stop.

The reading of the clock and calendar

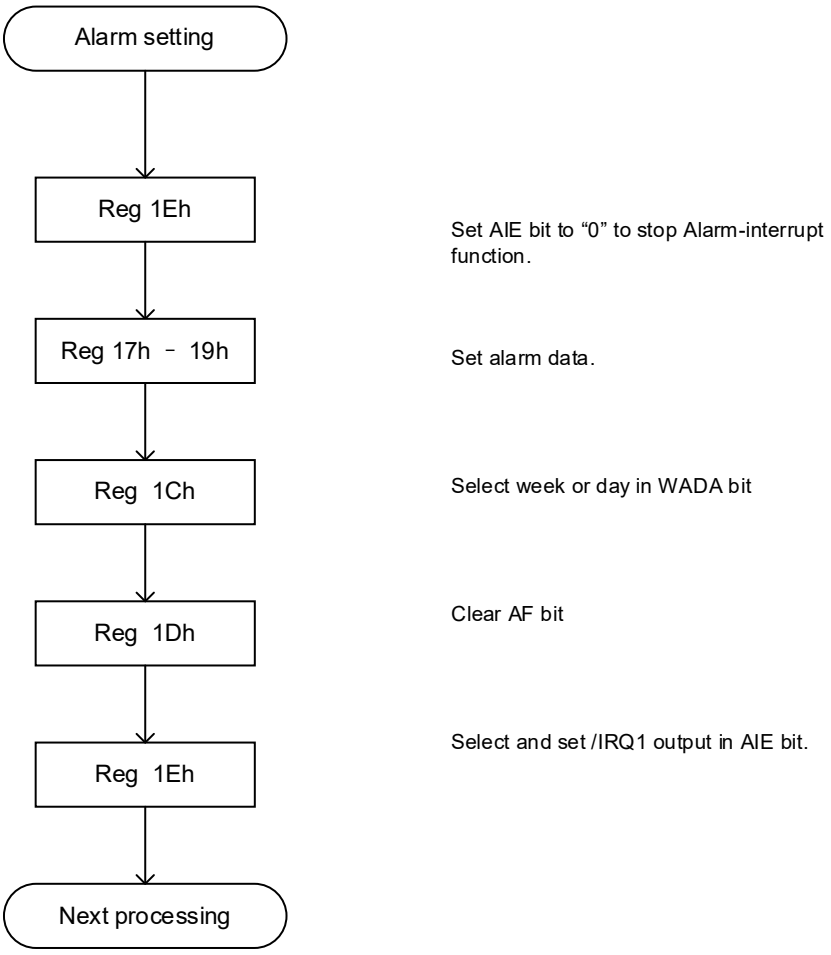


Pleas access within 0.95 seconds
The STOP bit holds complete "0".
(It causes the clock delay to set STOP bit to “1”)

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.

The access to a clock calendar recommends to have access to continuation by a auto increment function.

Setting example of the Alarm interrupt function



IIC-Bus Interface

The IIC-bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

Data transfers
Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.95 seconds.)

Starting and stopping IIC-Bus communications

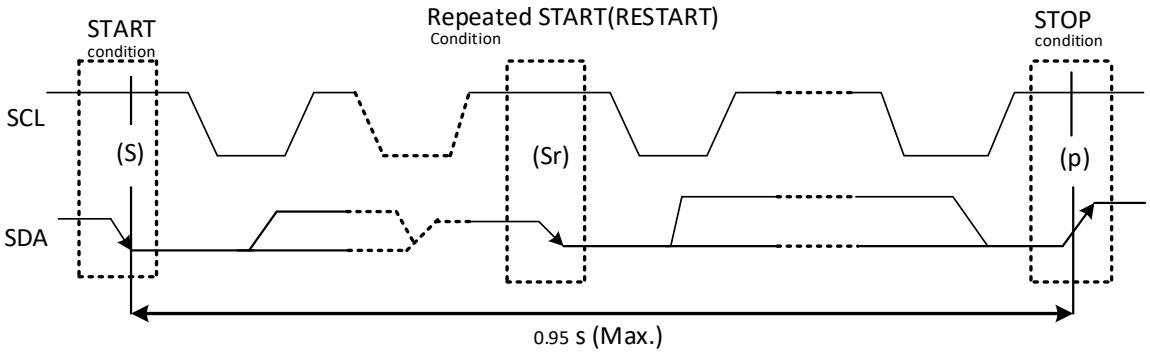


Figure 28 IIC-Bus start/stop timing

Slave address

Slave address							R/W bit
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	1	0	0	1	0	R/W

0 is Write mode
1 is Read mode

IIC-Bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RS5C8130Bis the slave.
Address specification write sequence

1) Address specification read sequence

Since the RS5C8130Bincludes an address auto increment function, once the initial address has been specified, the RS5C8130B increments (by one byte) the receive address each time data is transferred.

Address circulation of auto increment function.	**10h ->1Fh -> 10h**
	20h ->2Fh -> 20h
	30h ->3Fh -> 30h

(1) CPU transfers start condition [S].

(2) CPU transmits the RS5C8130B's slave address with the R/W bit set to write mode.

(3) Check for ACK signal from RS5C8130B.

(4) CPU transmits write address to RS5C8130B.

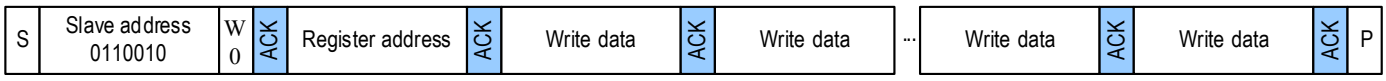
(5) Check for ACK signal from RS5C8130B.

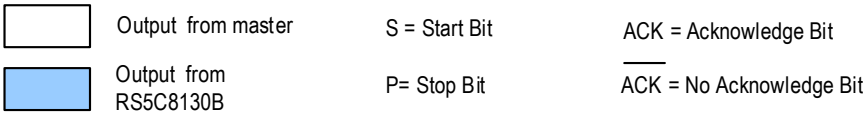
(6) CPU transfers write data to the address specified at (4) above.

(7) Check for ACK signal from RS5C8130B.

(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.

(9) CPU transfers stop condition [P].





2) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

(1) CPU transfers start condition [S].

(2) CPU transmits the RS5C8130B's slave address with the R/W bit set to write mode.

(3) Check for ACK signal from RS5C8130B.

(4) CPU transfers address for reading from RS5C8130B.

(5) Check for ACK signal from RS5C8130B.

(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).

(7) CPU transfers RS5C8130B's slave address with the R/W bit set to read mode.

(8) Check for ACK signal from RS5C8130B (from this point on, the CPU is the receiver and the RS5C8130B is the transmitter).

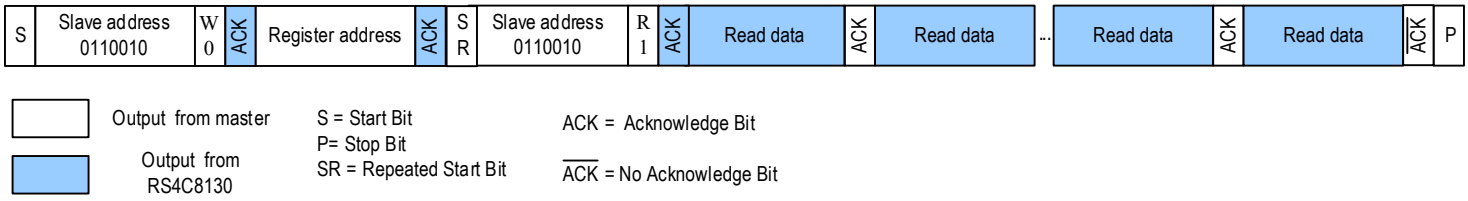
(9) Data from address specified at (4) above is output by the RS5C8130B.

(10) CPU transfers ACK signal to RS5C8130B.

(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented

(12) CPU transfers ACK signal for "1".

(13) CPU transfers stop condition [P].



Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].

(2) CPU transmits theRS5C8130B's slave address with the R/W bit set to read mode.

(3) Check for ACK signal from RS5C8130B(from this point on, the CPU is the receiver and the RS5C8130Bis the transmitter).

(4) Data is output from the RS5C8130B to the address following the end of the previously accessed address.

(5) CPU transfers ACK signal toRS5C8130B.

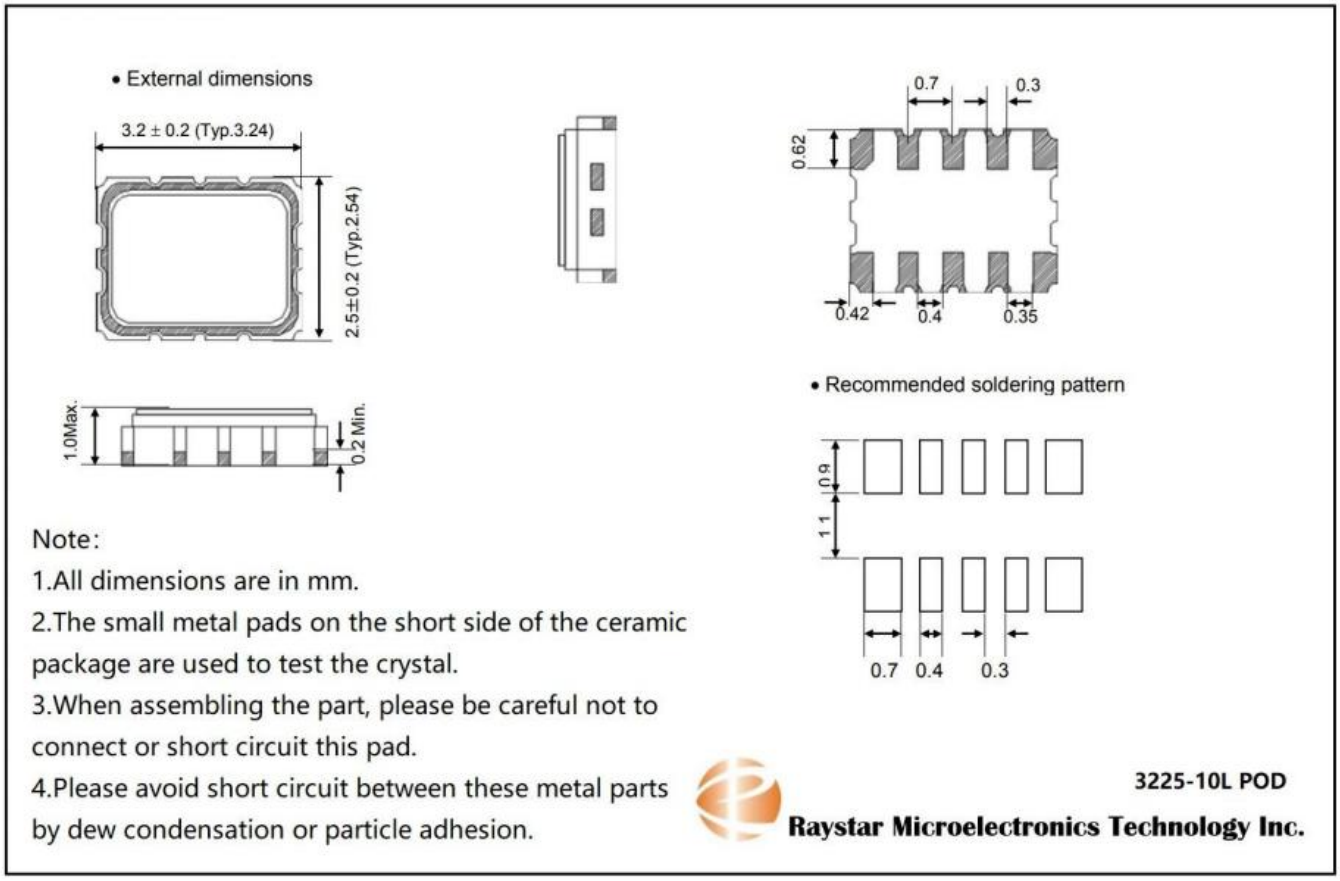
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RS5C8130B.

(7) CPU transfers ACK signal for "1".

(8) CPU transfers stop condition [P].

Package Information

3225 -10 pin



Revision History

Revision	Description	Date
V1.0	Initial Release	2025/7/17