Features

- 1:10 LVCMOS Output Clock Buffer
- 12kHz to 20MHz additive phase jitter: 25fs(Typical) RMS at 156.25MHz
- Operates DC to 200MHz
- Crystal Input: 8 to 50MHz
- Universal Input: LVPECL,LVDS,HCSL,SSTL, LVCMOS and LVTTL
- Output Skew: 30ps(Typical)
- Total Propagation Delay: 2ns(Typical)
- Synchronous and Glitch-Free Output Enable Is Available
- Spread-spectrum tolerant
- -40 to +85°C,
- 3.3V/2.5V/1.8V/1.5V Core Power Supply
- 3.3V/2.5V/1.8V/1.5V Output Power Supply
- VDDO can't be greater than VDD (VDDO≤ VDD)
- TQFN-32L 5.0 x 5.0mm package

Applications

- Wireless and Wired Infrastructure
- Networking and Data Communications
- Medical electronics
- Portable Test and Measurement

Description

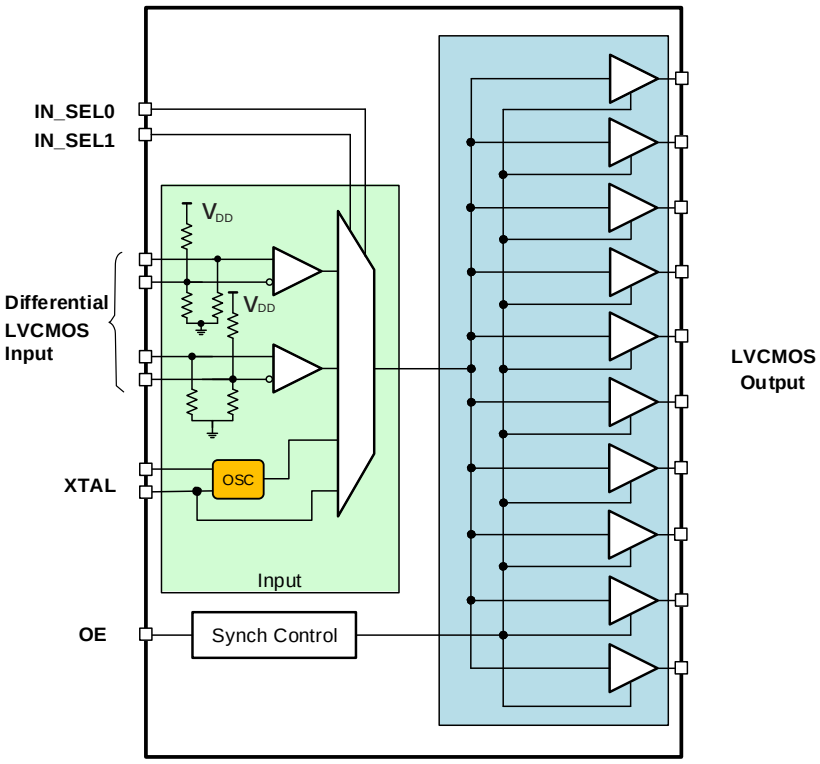
The RS2CB1310 device is a high-performance, low-jitter, low-power clock fanout buffer which can distribute to ten low-jitter LVCMOS clock outputs from one of three inputs, whose primary and secondary inputs can feature differential or single-ended signals and crystal input. Such a buffer is good for use in a variety of mobile and wired infrastructure, data communication, computing, low-power medical imaging, and portable test and measurement applications. When the input is an illegal level, the output is at a defined state. One can set the core to1.5V/1.8V/2.5V or 3.3V, and output to 1.5V/1.8V/2.5V or 3.3V. The overall additive jitter performance is 25fs RMS (typical).

Ordering Information

Part Number	Package	Description
RS2CB1310ZHE	TQFN-32L	5.0mm × 5.0 mm

Notes:
[1] E = Pb-free and Green

Block Diagram



Pin Configuration

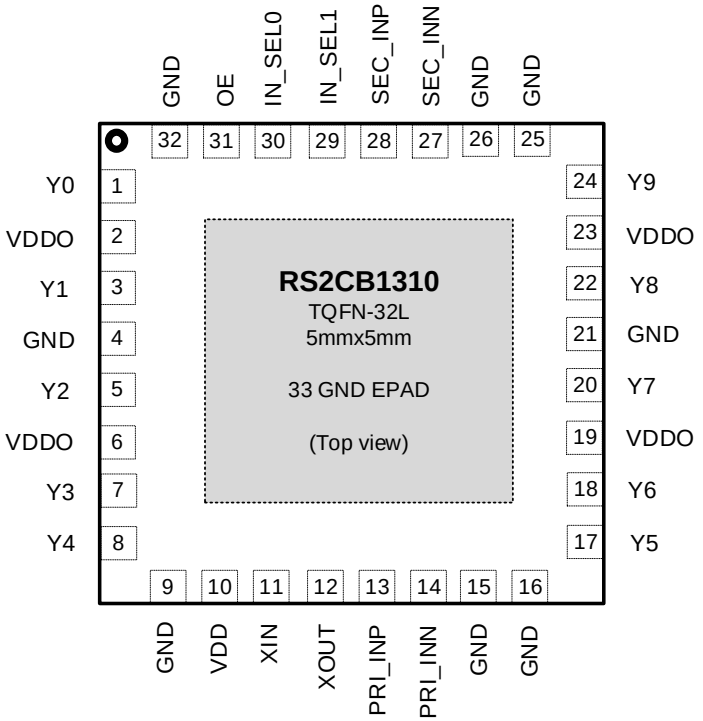


Figure 1. Pin Assignments for TQFN-32L Package

Pin Description

Table 1. Pin Descriptions

Pin Name	Number	Type	Description	Notes	
VDD	10	Power	Power Supply for operating Core and Clock Input.		
VDDO	2, 6,19, 23	Power	Power Supply for Clock Output.		
GND	4, 9, 15, 16, 21, 25, 26, 32	GND	Ground pin.		
IN_SEL0 IN_SEL1	30, 29	I, SE, PD	Clock Input Selection.	1	
OE	31	I, SE, PD	Output Enable. 1 = enable output, 0 = disable output.	1	
XIN	11	I, SE	Crystal input or XTAL bypass mode.		
XOUT	12	O, SE	Crystal Output. Leave XOUT floating if XIN is driven by a single-ended clock.		
PRI_INN	14	I, DIF	Primary complementary clock input. Leave PRI_INN floating if PRI_INP is driven by a single-ended clock.	2	
PRI_INP	13	I, DIF, SE	Primary true clock input or single-ended clock.	3	
SEC_INN	27	O, SE	Secondary complementary clock input. Leave SEC_INN floating if SEC_INP is driven by a single-ended clock.	2	
SEC_INP	28	O, SE	Secondary true clock input or single-ended clock.	3	
Y0	1	O, SE	LVCMOS Output 0.		
Y1	3	O, SE	LVCMOS Output 1.		
Y2	5	O, SE	LVCMOS Output 2.		
Y3	7	O, SE	LVCMOS Output 3.		
Y4	8	O, SE	LVCMOS Output 4.		
Y5	17	O, SE	LVCMOS Output 5.		
Y6	18	O, SE	LVCMOS Output 6.		
Y7	20	O, SE	LVCMOS Output 7.		
Y8	22	O, SE	LVCMOS Output 8.		
Y9	24	O, SE	LVCMOS Output 9.		
EPAD	33	GND	Connect EPAD to ground.		

1. CMOS control input with internal pull-down resistor(150 kΩ).
2. Clock input with internal biased to Vdd / 2 (pullup or pulldown of 150 kΩ).
3. Clock input with internal pull-down resistor(150 kΩ).

Table 2. Signal Types

Term	Description
I	Input
O	Output
PD	Pull-down
PU	Pull-up
SE	Single-ended
DIF	Differential
Power	Power
GND	Ground

Table 3. Input Selection

IN_SEL1	IN_SEL0	SELECTED INPUT	Notes
0	0	PRI_IN	
0	1	SEC_IN	
1	0	XTAL or overdrive	1
1	1	XTAL bypass	2

1. This mode is for XTAL input or overdrive of XTAL oscillator with LVCMOS input. For characteristics; see OUTPUT CHARACTERISTICS.
2.This mode is only XTAL bypass. For characteristics, see OUTPUT CHARACTERISTICS.

Table 4. INPUT/OUTPUT OPERATION

INPUT STATE	OUTPUT STATE
PRI_INx, SEC_INx open	Logic Low
PRI_INP, SEC_INP = High, PRI_INN, SEC_INN = Low	Logic High
PRI_INP, SEC_INP = Low, PRI_INN, SEC_INN = High	Logic Low

1. Device must have switching edge to obtain output states.

Table 5. OE Function

OE	Yx
0	High-impedance
1	Enabled

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CB1310 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN	MAX	Units	Notes
Core Supply Voltage	V_{DD}		-0.5	4.6	V	1,2
Output Supply Voltage	V_{DDO}		-0.5	4.6	V	1,2
Input Voltage	V_{IN}		-0.5	V_{DD} +0.5	V	
Output Voltage	V_{OUT}		-0.5	V_{DD} +0.5	V	
Input Current	I_{IN}		-20	20	mA	
Output Current	I_{OUT}		-50	50	mA	
Storage-temperature Temperature	T_{STG}		-65	125	°C	
Junction Temperature	T_J	Maximum operating junction temperature.		125	°C	
Input ESD Protection	ESD	Human Body Model.	2500		V	
		Charged-device Model	1000		V	

1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Core Supply Voltage	V_{DD}		2.375	2.5	2.625	V	
			3.135	3.3	3.465		
Output Supply Voltage	V_{DDO}		1.35	1.5	1.65	V	1
			1.6	1.8	2		
			2.375	2.5	2.625		
			3.135	3.3	3.465		
High-level output current, LVCMOS	I_{OH}				-24	mA	
Low-level output current, LVCMOS	I_{OL}				24	mA	
Operating Temperature	T_A		-40	25	85	°C	

1. V_{DDO} can't be greater than V_{DD} ($V_{DDO} \leq V_{DD}$).

Thermal Information

Table 8. Thermal Information

Package	Symbol	Conditions	TYP Value (°C/W)
TQFN (32) 5.0×5.0×0.5mm	θJa	Junction to Ambient	41.5
	θJctop	Junction to Case(top)	34.4
	θJcbot	Junction to Case(bottom)	6.3
	θJb	Junction to Board	14.4
	ψ_{JT}	Junction to Top Characterization Parameter	0.9
	ψ_{JB}	Junction to Board Characterization Parameter	14.4

Current Consumption

2.375V ≤ V_{DD} ≤ 3.45V, 1.35V ≤ V_{DDO} ≤ V_{DD}, -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at V_{DD} = V_{DDO} = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Table 9. Current Consumption

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Static device Current	I_{DD}	OE = 0V or V_{DD}; Ref. input (PRI/SEC) = 0 V or V_{DD}; I_O = 0mA; V_{DD} / V_{DDO} = 3.3V		14		mA	1
		OE = 0V or V_{DD}; Ref. input (PRI/SEC) = 0V or V_{DD}; I_O = 0mA; V_{DD} / V_{DDO} = 2.5V		8			
Device current with XTAL input	$I_{DD,XTAL}$			20		mA	1
Power dissipation capacitance per output	C_{PD}	V_{DDO}=3.465V @100MHz			8.8	pF	2
		V_{DDO}=2.625V @100MHz			7.7		
		V_{DDO}=2V @100MHz			7.3		
		V_{DDO}=1.65V @100MHz			6.9		

1. I_{DD} and $I_{DD,XTAL}$ is the current through V_{DD}; outputs enabled or in the high-impedance state; no load.
2. This is the formula for the power dissipation calculation (see the *Power Considerations* section)
   $I_{DD,Total} = I_{DD} + I_{DD,Cload} + I_{DD,dyn}$ [mA]
   $I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]
   $I_{DD,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA]
   n = Number of switching output pins

Input Characteristics

2.375V ≤ V_{DD} ≤ 3.45V, 1.35V ≤ V_{DDO} ≤ V_{DD}(V_{DDO} ≤ V_{DD}), -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at V_{DD} = V_{DDO} = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Table 10. Input Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
DC Characteristic (OE, IN_SEL0, IN_SEL1, PRI_IN, SEC_IN)							
Input High Current	I_{IH}	V_{DD}=3.465V, V_{IH}=3.465V			40	µA	
Input Low Current	I_{IL}	V_{DD}=3.465V, V_{IH}=0V			-40		
Input edge rate	ΔV/ΔT	20%--80%		2		V/ns	
Pullup or pulldown resistance	$R_{PU/PD}$			150		kΩ	
Input capacitance	C_{IN}			2		pF	
Single-Ended DC Characteristic (PRI_INP, SEC_INP)							
Input High Voltage	V_{IH}	V_{DD} = 3.3V ±5%	2		V_{DD}+0.3	V	1
		V_{DD} = 2.5V ±5%	1.6		V_{DD}+0.3		
Input Low Voltage	V_{IL}	V_{DD} = 3.3V ±5%	-0.3		1.3		
		V_{DD} = 2.5V ±5%	-0.3		0.9		
Single-Ended DC Characteristic (OE, IN_SEL0, IN_SEL1)							
Input High Voltage	V_{IH}		0.7 x V_{DD}			V	
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V	
Differential DC Characteristic (PRI_IN, SEC_IN)							
Differential input voltage swing	$V_{I,DIFF}$		0.15		1.3	V	2
Input common-mode voltage	V_{ICM}		0.5		V_{DD}-0.85		3
AC Characteristic (PRI_IN, SEC_IN							
Input Frequency	F_{IN}				200	MHz	
Input duty cycle	I_{DC}		40%		60%		

1. PRI/SEC_INN biased to VDD/2.
2. V_{IL} should not be less than –0.3V.
3. Input common-mode voltage is defined as V_{IH} (see Figure 19).

Crystal Characteristics

2.375V ≤ V_{DD} ≤ 3.45V, 1.35V ≤ V_{DDO} ≤ V_{DD}(V_{DDO} ≤ V_{DD}), -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at V_{DD} = V_{DDO} = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Table 11. Crystal Characteristics

Parameter	Test Conditions	MIN	TYP	MAX	Units	Notes
Equivalent series resistance (ESR)			50		Ω	
Maximum shunt capacitance			7		pF	
Drive level			100		µW	

Crystal Oscillator Characteristics

2.375V ≤ VDD ≤ 3.45V, 1.35V ≤ VDDO ≤ VDD(VDDO ≤ VDD), -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at VDD = VDDO = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Table 12. Crystal Oscillator Characteristics

Parameter	Test Conditions	MIN	TYP	MAX	Units	Notes
Mode of oscillation		Fundamental				
Frequency		8		50	MHz	
Frequency in overdrive mode				50		1
Frequency in bypass mode				50		2
On-chip load capacitance			12		pF	

1. Input signal swing (max) = 2V; input signal tr (max) = 10ns; tf (max) = 10ns; functional, but device may not meed ac parameters.
2. Input signal swing (max) = VDD; input signal tr (max) = 10ns; tf (max) = 10ns; functional, but device may not meed ac parameters.

Output Characteristics

2.375V ≤ VDD ≤ 3.45V, 1.35V ≤ VDDO ≤ VDD(VDDO ≤ VDD), -40°C ≤ TA ≤ 85°C. Typical values represent most likely parametric norms at VDD = VDDO = 3.3V, TA = 25°C, at the Recommended Operation Conditions at the time of product characterization and are not ensured. Test conditions: load 50Ω to VDDO/2

Table 13. Output Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Output Skew	$t_{SK(O)}$	Measured between outputs(Ym to Yn)		30	50	ps	
Part-to-Part Skew	$t_{SK(PP)}$				2	ns	1
Propagation Delay Clock IN to Clock OUT	t_{DELAY}	V_{DD} = 3.3 V ±5%, V_{DDO} = 1.35 V to V_{DD}	1.5	1.95	5.0	ns	
		V_{DD} = 2.5 V ±5%, V_{DDO} = 1.35 V to V_{DD}	1.8	2.4	6.0		
Output slew rate, rising and falling	$t_{SLEW-RATE}$	V_{DDO}=3.3V +/- 5%, 20% to 80%	5.6	7.3	9.0	V/ns	
		V_{DDO}=2.5V +/- 5%, 20% to 80%	3.9	4.8	5.4		
		V_{DDO}=1.8V +/- 200mV, 20% to 80%	1.6	2.1	2.5		
		V_{DDO}=1.5V +/- 150mV, 20% to 80%	0.9	1.2	1.4		
Output Frequency	F_{OUT}				200	MHz	
Output High Voltage	V_{OH}	V_{DDO} = 3.135V to 3.465V	0.8*V_{DDO}			V	
		V_{DDO} = 2.375V to 2.625V	0.8*V_{DDO}				
		V_{DDO} = 1.6V to 2V	0.7*V_{DDO}				
		V_{DDO} = 1.35V to 1.65V	0.7*V_{DDO}				
Output Low Voltage	V_{OL}	V_{DDO} = 3.135V to 3.465V			0.2*V_{DDO}	V	
		V_{DDO} = 2.375V to 2.625V			0.2*V_{DDO}		
		V_{DDO} = 1.6V to 2V			0.3*V_{DDO}		
		V_{DDO} = 1.35V to 1.65V			0.3*V_{DDO}		
Output Resistance	R_{CLKOUT}	V_{DDO} = 3.3V		15		ohm	
		V_{DDO} = 2.5V		20			
		V_{DDO} = 1.8V		25			
		V_{DDO} = 1.5V		30			

System-level additive jitter	tRJIT	Single-ended input, VDD = 3.3V VDDO = 3.3V		25		fs, RMS	2
		Single-ended input, VDD = 2.5V or 3.3V VDDO = 1.5V,1.8V,2.5V, FIN/OUT=125MHz		30			
		Differential input, VDD = 3.3V VDDO = 3.3V		30			
		Differential input, VDD = 2.5V or 3.3V VDDO = 1.5V,1.8V,2.5V, FIN/OUT=125MHz		30			
Noise floor	NF	10KHz offset		–145		dBc/Hz	3
		100KHz offset		–156			
		1MHz offset		–163			
		10MHz offset		–164			
		20MHz offset		–164			
		10KHz offset		–145			4
		100KHz offset		–155			
		1MHz offset		–160			
		10MHz offset		–161			
		2-MHz offset		–162			
Output duty cycle	ODC	FIN/OUT=125MHz, IDC = 50%	45%		55%		5
Output enable or disable time	tEN				2	Cycle	
MUX isolation	MUXISOLATION	125MHz	55			dB	6

1. Calculation for part-to-part skew is the difference between the fastest and the slowest tpd across multiple devices.
2. Integration range: 12KHz–20MHz; input source see the *System-Level Additive-Jitter Measurement* section.
3. Single-ended input, $f_{IN/OUT}$ = 125MHz, VDD = VDDO = 3.3V.
4. Differential input, $f_{IN/OUT}$ = 125MHz, VDD = VDDO = 3.3V.
5. Stable V_{IH}, V_{IL}, and V_{CM}
6. See Figure 18.

PHASE NOISE WITH XTAL SELECTED

VDD = VDDO = 2.5V or 3.3V, f_{XTAL} = 25MHz, TA = 25°C (unless otherwise noted). The selected XTAL specification refer to NOTE 1.

Table 14. PHASE NOISE

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
RMS phase jitter	Jrms	IB = 12kHz to 5MHz, VDD = VDDO = 3.3V		80		fs rms	1
		IB = 12kHz to 5MHz, VDD = VDDO = 2.5V		115			
Phase noise (see Figure 15)	PN	f_{offset} = 100Hz, VDD = VDDO = 3.3V		–92		dBc/Hz	
		f_{offset} = 1kHz, VDD = VDDO = 3.3V		–137			
		f_{offset} = 10kHz, VDD = VDDO = 3.3V		–163			
		f_{offset} = 100kHz, VDD = VDDO = 3.3V		–168			
		f_{offset} = 1MHz, VDD = VDDO = 3.3V		–168			
		f_{offset} = 5MHz, VDD = VDDO = 3.3V		–169			
		f_{offset} = 100Hz, VDD = VDDO = 2.5V		–91			
		f_{offset} = 1kHz, VDD = VDDO = 2.5V		–136			
		f_{offset} = 10kHz, VDD = VDDO = 2.5V		–159			
		f_{offset} = 100kHz, VDD = VDDO = 2.5V		–164			
		f_{offset} = 1MHz, VDD = VDDO = 2.5V		–165			
		f_{offset} = 5MHz, VDD = VDDO = 2.5V		–165			

1. Crystal specification: CL = 18pF; ESR = 35Ω (max); C0 = 7pF; drive level = 100µW (max).

TEST CONFIGURATIONS

Figure 2 through Figure 8 illustrate how to set up the device for a variety of test configurations.

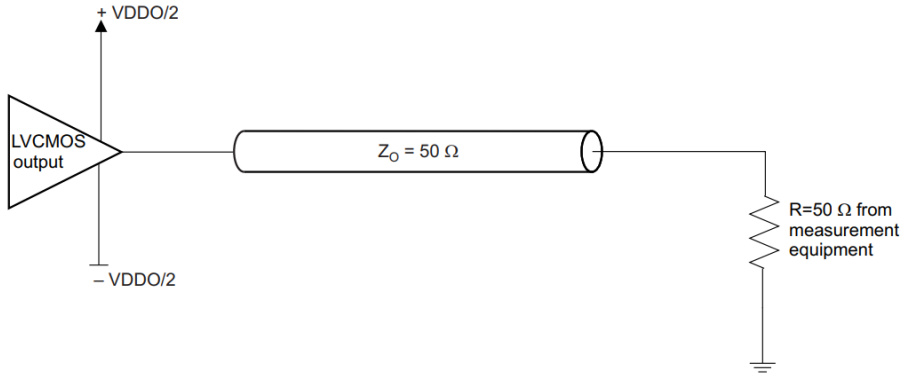


Figure 2. LVCMOS Output DC Configuration; Test Load Circuit

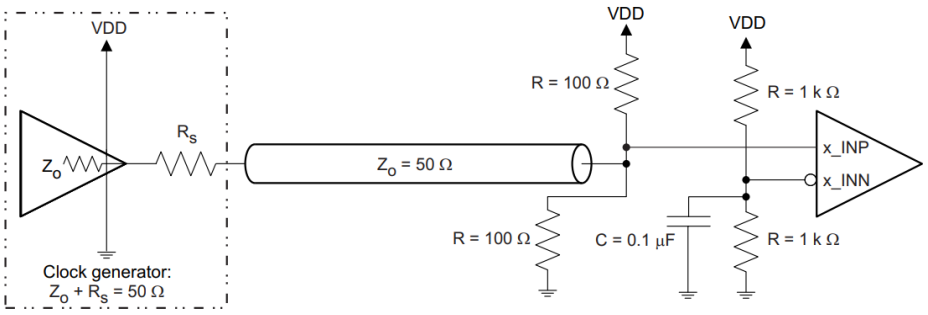


Figure 3. LVCMOS Input DC Configuration During Device Test

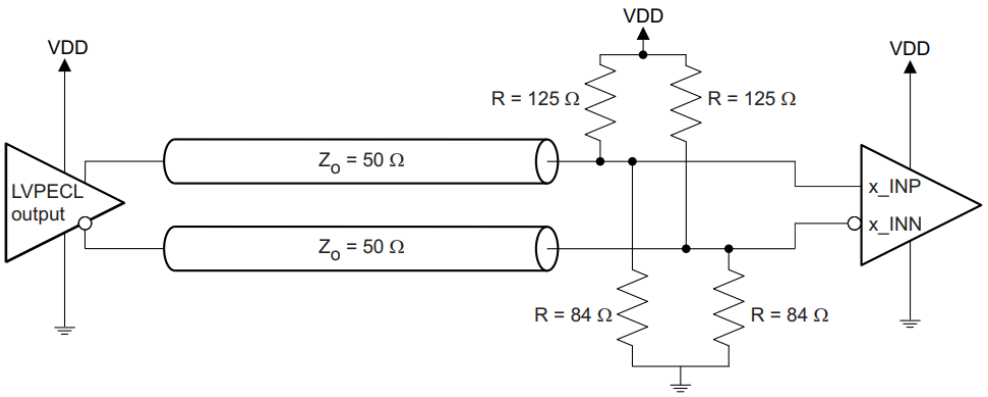


Figure 4. LVPECL Input Configuration During Device Test

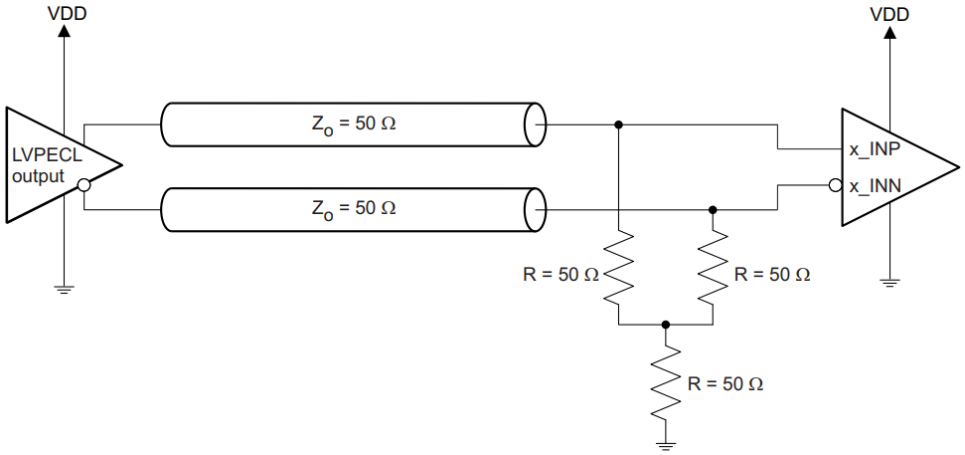


Figure 5. LVPECL Input Configuration During Device Test

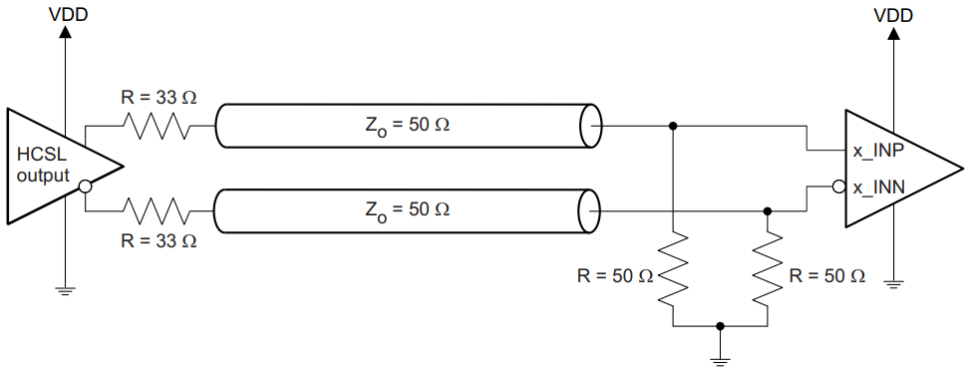


Figure 6. HCSL Input Configuration During Device Test

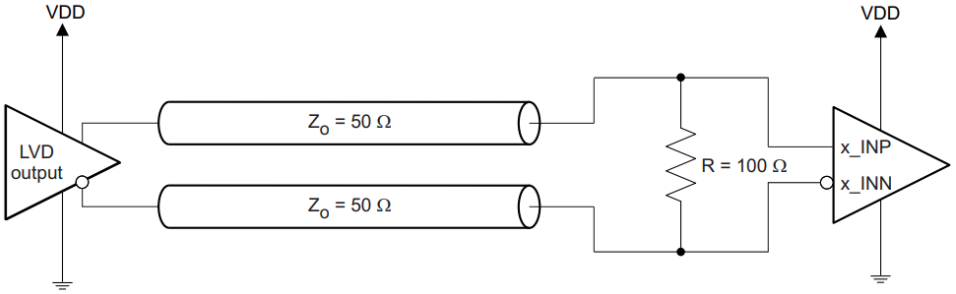


Figure 7. LVDS Input Configuration During Device Test

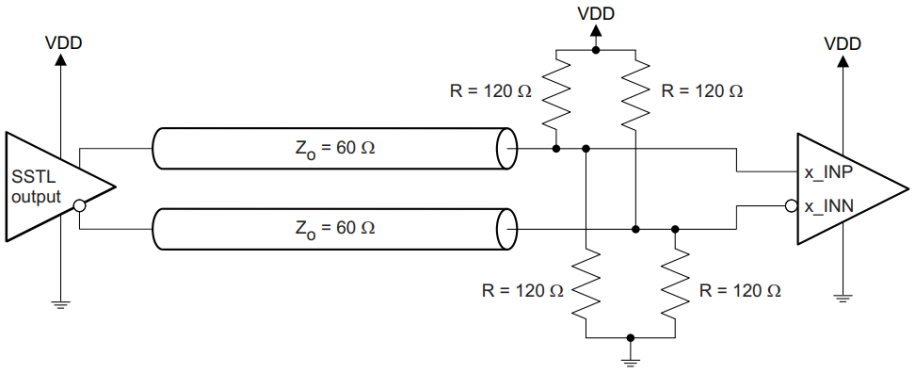


Figure 8. SSTL Input Configuration During Device Test

APPLICATION INFORMATION

Typical Application Load

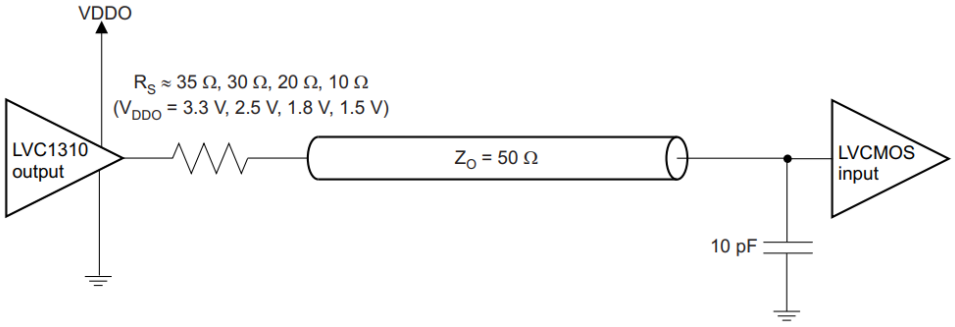


Figure 9. LVCMOS Output DC Configuration: Typical Application Load

Parameter Measurement Information

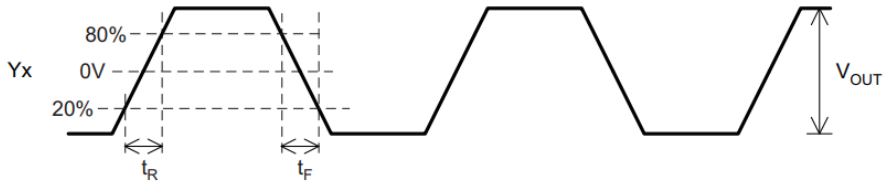


Figure 10. LVCMOS Output Voltage, and Rise and Fall Times

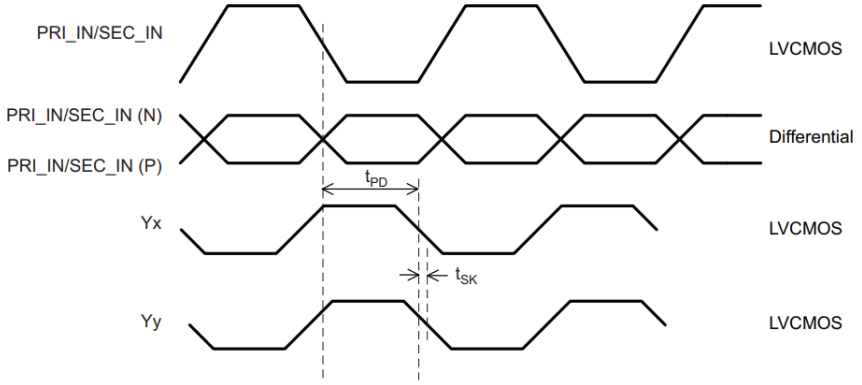


Figure 11. Differential and Single-Ended Output Skew and Propagation Delay

Crystal Oscillator Input

The crystal oscillator circuit is characterized with 18-pF parallel-resonant crystals. Choices of C1 and C2 were to minimize the ppm error. Optional resistor $R_{OPTIONAL}$ limits the drive level of the oscillator circuit.

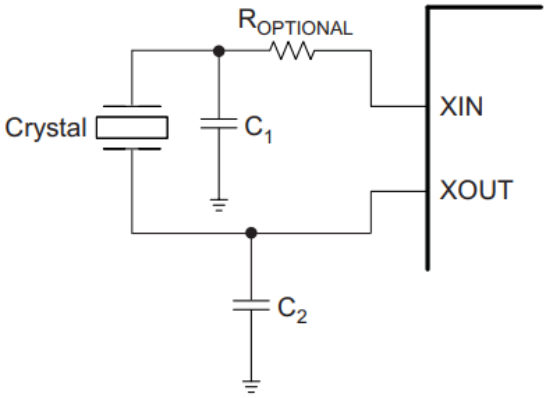


Figure 12. Crystal Reference Input

The input XIN can accept single-ended LVCMOS signals in two configurations. It is possible to overdrive the oscillator stage or to use a pure LVCMOS input (see Table 3). If overdriving the oscillator stage, it is necessary to ac-couple the input with a capacitor (see Figure 13). Otherwise, if selecting the bypass, there is no requirement for a coupling capacitor.

NOTE

1. If using the overdrive or bypass mode, the device is functional, but may not meet its ac parameters.

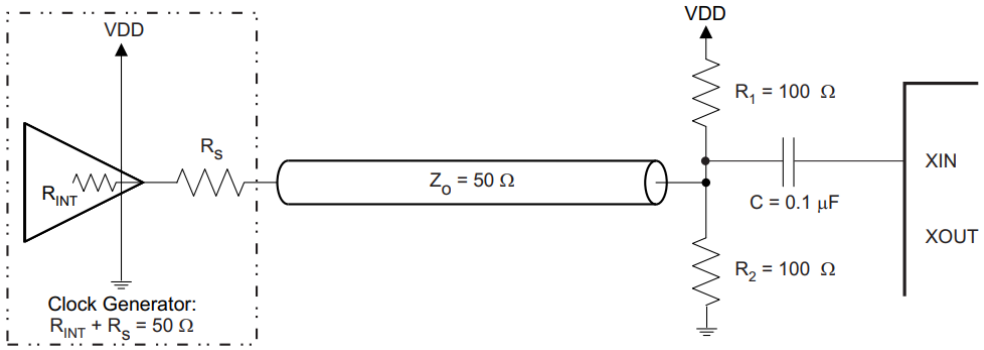


Figure 13. Single-Ended Crystal Input

Phase-Noise Performance

The RS2CB1310 provides ultralow phase-noise outputs (noise floor = –170dBc/Hz) if it has an attached crystal. Figure 14 shows the phase-noise plot of the RS2CB1310 with a 25-MHz crystal at V_{DD} = V_{DDO} = 3.3V and room temperature.

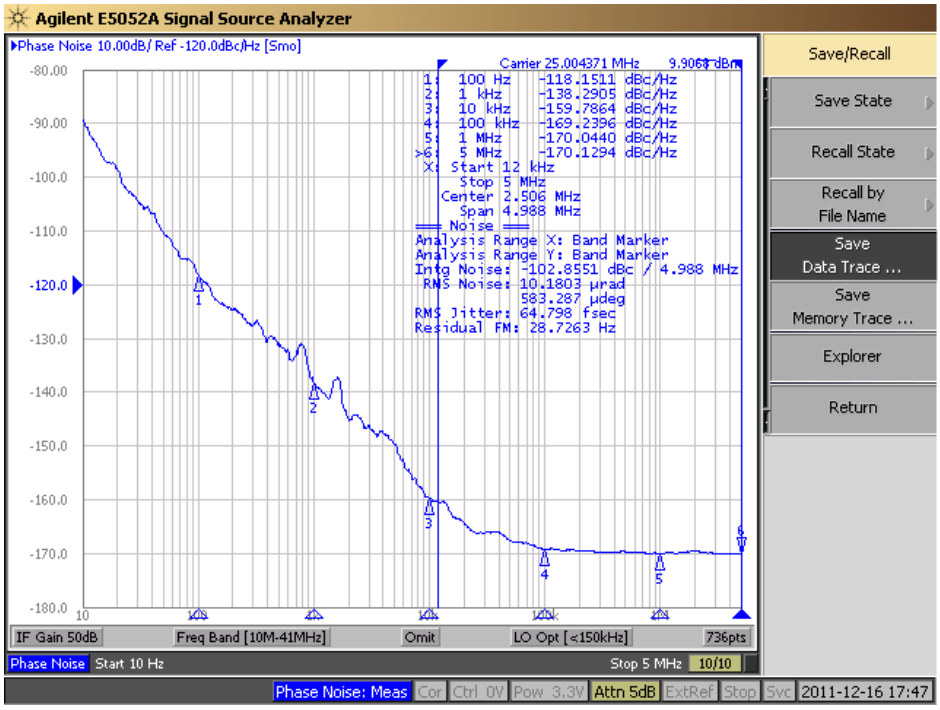


Figure 14. Phase-Noise Profile With 25-MHz Crystal at Nominal Conditions

System-Level Additive-Jitter Measurement

For high-performance devices, limitations of the equipment influence phase-noise measurements. The noise floor of the equipment often exceeds the noise floor of the device. The real noise floor of the device is probably lower (see Output Characteristics). Phase noise is influenced by the input source and the measurement equipment.

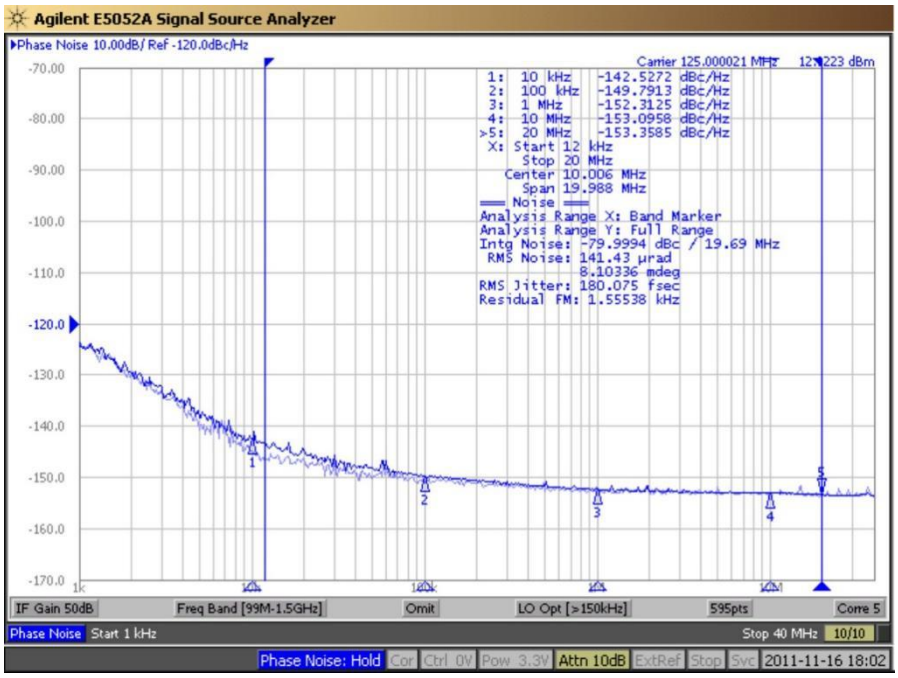


Figure 15. Input Phase Noise (179.4 fs, Light Blue) and Output Phase Noise (180 fs, Dark Blue)

Output Enable

Pulling OE to LOW (t_1), forces the outputs to the high-impedance state after the next falling edge of the input signal (t_2). The outputs remain in the high-impedance state as long as OE is LOW (see Figure 16).

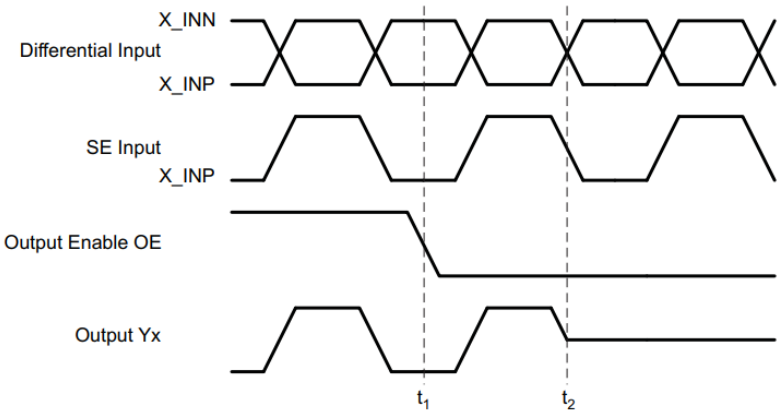


Figure 16. OE: Disable Outputs

If the outputs are in the high-impedance state, pulling OE to HIGH forces all outputs LOW asynchronously (t_3). Within two clock cycles (maximum), the outputs start switching again (t_4), after a falling edge of the input signal (see Figure 17).

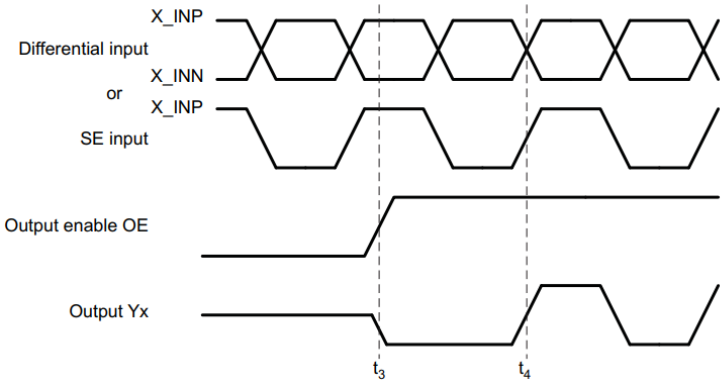


Figure 17. OE: Enable Outputs

If the outputs are in the high-impedance state and the input is static (no clock signal), OE works fully asynchronously. A transition of OE from LOW to HIGH forces the outputs to LOW. A transition from HIGH to LOW does not force to the high-impedance state again. Therefore, a state change requires a falling edge of the input signal (see Figure 16).

MUX Isolation

The definition of MUX isolation is the difference in output amplitude (dB) between an active and a static input signal.

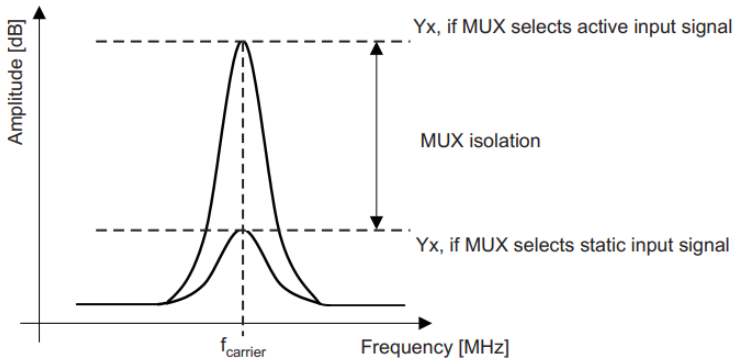
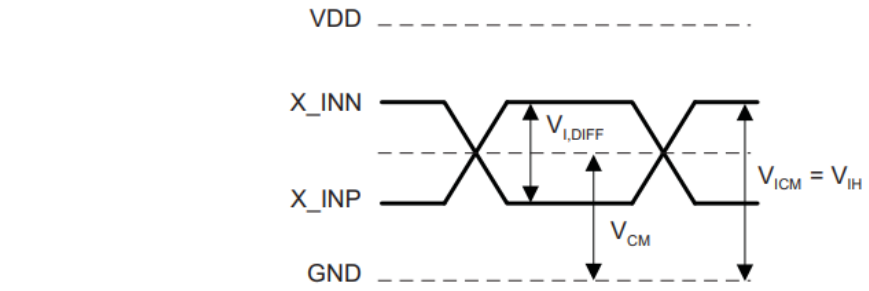


Figure 18. Output Spectrum of an Active and a Static Input Signal

Differential Input Level



NOTE: The calculation for VCM is: $V_{CM} = V_{DD} - V_{ICM} - V_{I,DIFF}/2$

Figure 19. Differential Input Level

Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states
- Power required to charge any output load

The output load can be capacitive-only or capacitive and resistive. Use the following formula to calculate the power consumption of the device:

$P_{Dev} = P_{stat} + P_{dyn} + P_{Cload}$ (see Figure 20 and Figure 21)

$P_{stat} = I_{DD} \times V_{DD}$

$P_{dyn} + P_{Cload} = (I_{DD,dyn} + I_{DD,Cload}) \times V_{DDO}$

where:

$I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA] (see Figure 22)

$I_{DD,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA]

Example for power consumption of the RS2CB1310: 10 outputs are switching, f = 100MHz, $V_{DD} = V_{DDO} = 3.3V$ and assuming $C_{load} = 2pF$ per output:

$P_{Dev} = 46.2mW + 117.5mW = 163.7mW$

$P_{stat} = 14\ mA \times 3.3V = 46.2mW$

$P_{dyn} + P_{Cload} = (29mA + 6.6\ mA) \times 3.3\ V = 117.5mW$

$I_{DD,dyn} = 8.8pF \times 3.3V \times 100MHz \times 10 = 29mA$

$I_{DD,Cload} = 2pF \times 3.3V \times 100MHz \times 10 = 6.6mA$

NOTE

1.For dimensioning the power supply, consider the total power consumption.The total power consumption is the sum of device power consumption and the power consumption of the load.

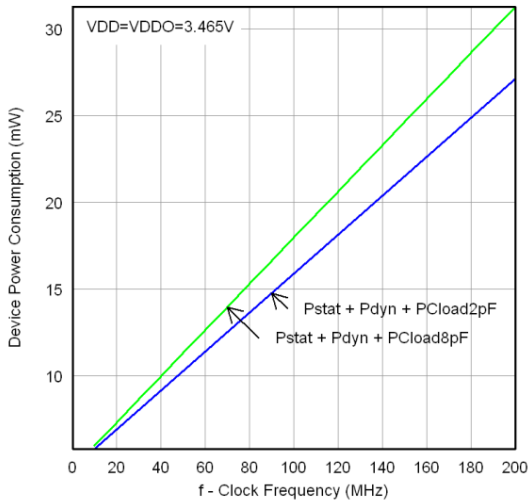


Figure 20. Device Power Consumption versus Clock Frequency (VDD = VDDO = 3.465 V; Load 2 pF, 8 pF; per Output)

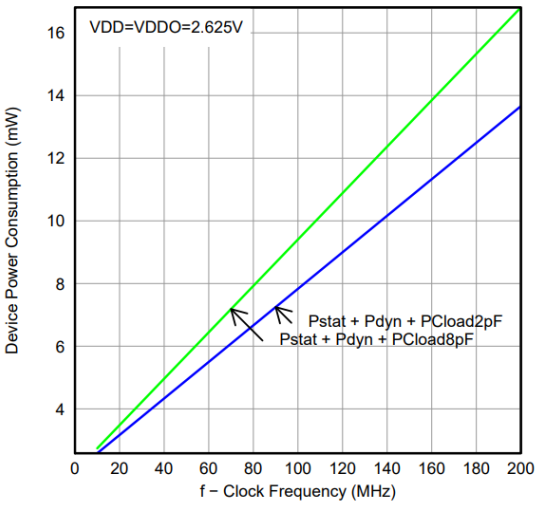


Figure 21. Device Power Consumption versus Clock Frequency (VDD = VDDO = 2.625 V; Load 2 pF, 8 pF; per Output)

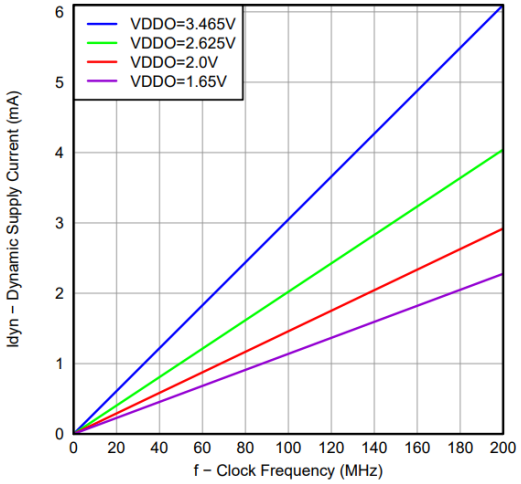


Figure 22. Dynamic Supply Current versus Clock Frequency (per Output)

Power Supply Filtering

It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is very critical to applications.

Use of filter capacitors eliminates the low-frequency noise from power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them very close to the power supply pins and lay out traces with short loops to minimize inductance. RSM recommends to adding as many high- frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package.

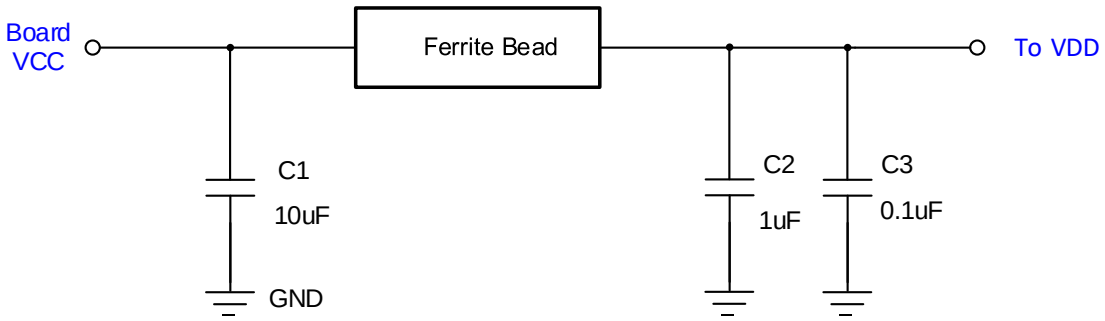
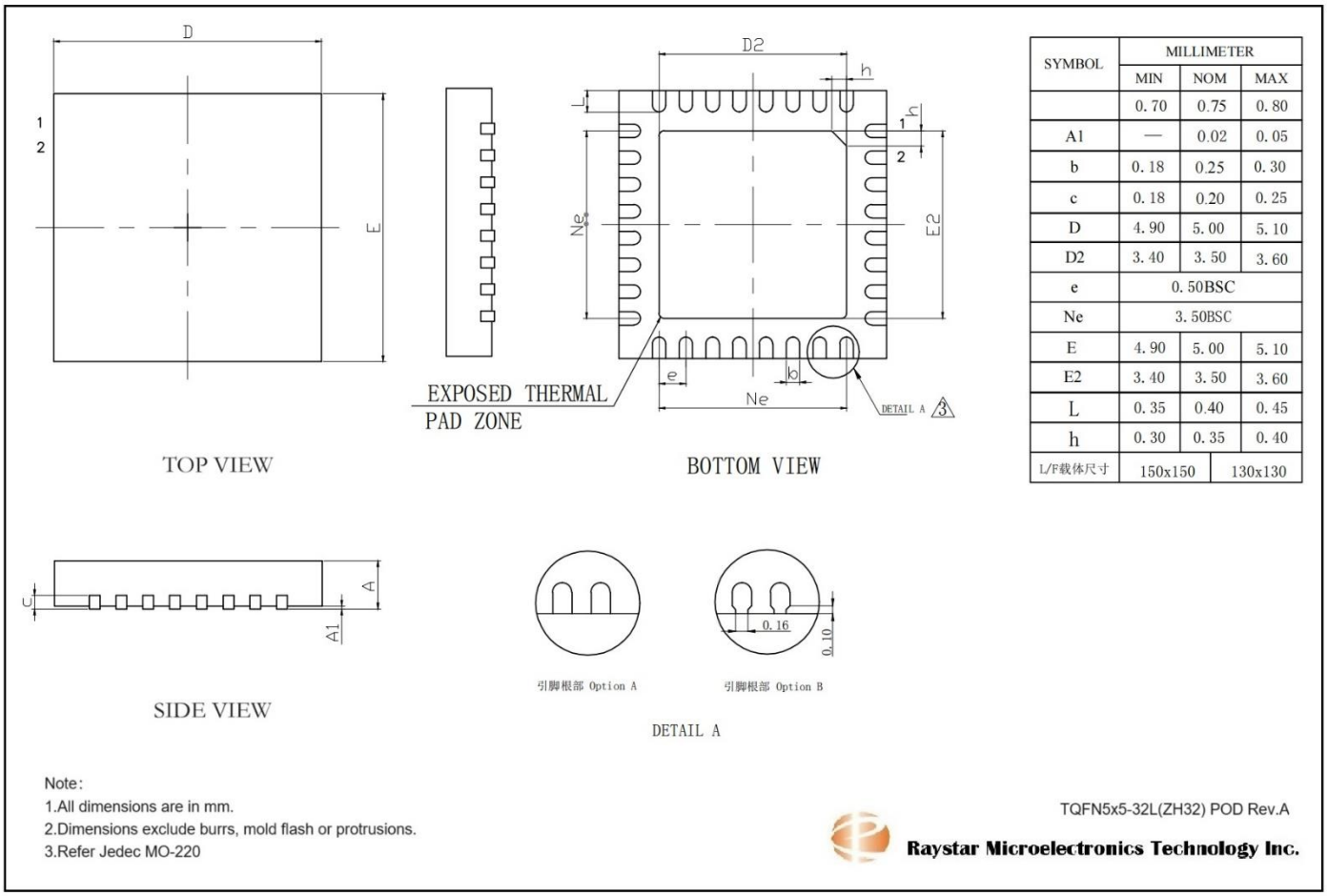


Figure 23. Power-Supply Decoupling

Package Information

TQFN-32L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	150x150		130x130

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TQFN5x5-32L(ZH32) POD Rev.A
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	1. Preliminary release	2024/06/21
1.0	1. Initial release	2025/7/8