RS7LS304

140Mb/s Bi-directional Level Translator for Push-Pull Applications

Features

- Qualified for Automotive Applications
- 1.65V to 3.6V on A Port and 1.65V to 3.6V on B Port
- VCCA may be greater than, equal to, or less than VCCB
- High-Speed with 140 Mb/s Guaranteed Date Rate
- 100 pF Capacitive Drive Capability
- Low Bit-to-Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Power-Up Sequencing
- Power-Off Protection
- ESD protection exceeds 4000V HBM
- Extended Temperature: -40°C to +85°C

Applications

- I2C/SMBus, MDIO, SPI Interface
- Low-Voltage ASIC Level Translation
- Tablet, PC
- Server, Telecommunication

Block Diagram

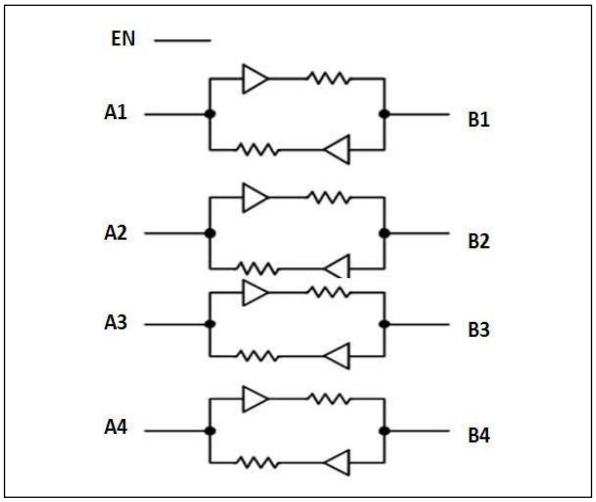


Figure 1 : Block Diagram

Description

The RS7LS304 is an automotive qualified 4-bit configurable dual-supply autosensing bidirectional level translator that does not require a direction control pin. The B and A ports are designed to track two different power supply rails, VCCB and VCCA respectively.

The RS7LS304 offers the feature that the values of the VCCB and VCCA supplies are independent. Design flexibility is maximized because VCCA can be set to a value either greater than or less than the VCCB supply.

The RS7LS304 has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. Another feature of the RS7LS304 is that each An and Bn channel can function as either an input or an output.

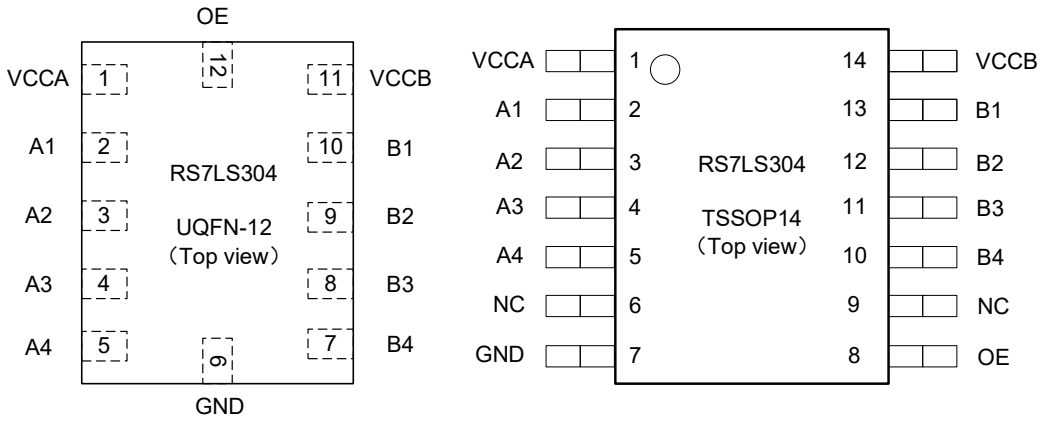
An Output Enable (EN) input is available to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current.

Ordering Information:

Part Number	Package	Description
RS7LS304ZME	UQFN-12	1.7mmx2.0 mm
RS7LS304LE	TSSOP-14	pitch 0.65mm

Notes:
[1] E = Pb-free and Green

Pin Configuration



Pin Name	UQFN-12	TSSOP-14	Description
VCCA	1	1	A-port supply voltage.1.65V ≤ VCCA ≤3.6 V
A1	2	2	Input/output A. Referenced to VCCA.
A2	3	3	Input/output A. Referenced to VCCA
A3	4	4	Input/output A. Referenced to VCCA
A4	5	5	Input/output A. Referenced to VCCA
GND	6	7	Ground.
OE	12	8	Output enables (active High). Pull OE low to place all outputs in 3-state mode.
B4	7	10	Input/output B. Referenced to VCCB
B3	8	11	Input/output B. Referenced to VCCB
B2	9	12	Input/output B. Referenced to VCCB
B1	10	13	Input/output B. Referenced to VCCB
VCCB	11	14	B-port supply voltage.1.65V ≤ VCCB ≤3.6V
NC	/	6,9	Not Connect

Maximum Ratings

Symbol	Parameter	Min	TYP	Max	Unit
Tstore	Storage Temperature	−65	-	+150	°C
VCCA	DC Supply Voltage port B	-0.3	-	4.0	V
VCCB	DC Supply Voltage port A	-0.3	-	4.0	V
VIOB	Vi(A) referenced DC Input / Output Voltage	-0.3	-	4.0	V
VIOB	Vi(B) referenced DC Input / Output Voltage	-0.3	-	4.0	V
VEN	Enable Control Pin DC Input Voltage	-0.3	-	4.0	V
Ishort	Short circuit duration (I/O to GND)			50	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	Min	TYP	Max	Unit
VCCA	VCCA Positive DC Supply Voltage	1.65	-	3.6	V
VCCB	VCCB Positive DC Supply Voltage	1.65	-	3.6	V
VEN	Enable Control Pin Voltage	GND	-	3.6	V
VIO	I/O Pin Voltage	GND	-	3.6	V
Δt /ΔV	Input transition rise or fall time	-	-	10	ns/V
TA	Operating Temperature Range	−40	-	+85	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤85°C, 1.65V≤V_{CCA}≤3.6V , 1.65V≤V_{CCB}≤3.6V

Symbol	Parameter	Test Conditions	V_{CCB} (V)	V_{CCA} (V)	-40°C to +85°C			Unit
					Min.	Typ.	Max.	
V_{IHB}	B port Input HIGH Voltage	—	1.65-3.6	1.65-3.6	2/3*VCCB	—	—	V
V_{ILB}	B port Input LOW Voltage	—	1.65-3.6	1.65-3.6	—	—	1/3*VCCB	V
V_{IHA}	A port Input HIGH Voltage	—	1.65-3.6	1.65-3.6	2/3*VCCA	—	—	V
V_{ILA}	A port Input LOW Voltage	—	1.65-3.6	1.65-3.6	—	—	1/3*VCCA	V
V_{IH}	Control Pin Input HIGH Voltage	—	1.65-3.6	1.65-3.6	2/3*VCCA	—	—	V
V_{IL}	Control Pin Input LOW Voltage	—	1.65-3.6	1.65-3.6	—	—	1/3*VCCA	V
V_{OHB}	B port Output HIGH Voltage	B port source current = 20μA	1.65-3.6	1.65-3.6	0.9*VCCB	—	—	V
V_{OLB}	B port Output LOW Voltage	B port sink current = 20μA	1.65-3.6	1.65-3.6	—	—	0.2	V
V_{OHA}	A port Output HIGH Voltage	A port source current= 20μA	1.65-3.6	1.65-3.6	0.9*VCCA	—	—	V
V_{OLA}	A port Output LOW Voltage	A port sink current = 20μA	1.65-3.6	1.65-3.6	—	—	0.2	V
I_{QVB}	VCCB Supply Current	EN = VCCA, I_O = 0A, (I/O_B= 0V or VCCB, I/O_A= float) or (I/O_B = float, I/O_A = 0V or V_{CCA})	1.65-3.6	1.65-3.6	—	0.1	6	μA
I_{QVA}	VCCA Supply Current		1.65-3.6	1.65-3.6	—	0.2	30	μA
I_{TS-B}	B port Tristate Output Mode Supply Current	EN=0V (I/O_B = 0V or VCCB, I/O_A = float) or (I/O_B = float, I/O_A = 0V or V_{CCA})	1.65-3.6	1.65-3.6	—	0.1	6	μA
I_{TS-A}	A port Tristate Output Mode Supply Current		1.65-3.6	1.65-3.6	—	0.2	30	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	EN= 0V	1.65-3.6	1.65-3.6	—	—	±6	μA
I_I	Control Pin Input Current	—	1.65-3.6	1.65-3.6	—	—	±1	μA
I_{OFF}	Power Off Leakage Current	I/O_B = 0 to 3.6V, I/O_A = 0 to 3.6V	0	0	—	—	15	μA
			1.65-3.6	0	—	—	30	
			0	1.65-3.6	—	—	15	

AC Electrical characteristics

Symbol	Parameter	Test Conditions	V_{CCB} (V)	V_{CCA} (V)	-40°C to +85°C			Unit
					Min.	Typ.	Max.	
t_{RB}	B port Rise Time	C_{IOB} = 15 pF	1.65-3.6	1.65-3.6	—	1	4	ns
t_{FB}	B port Fall Time	C_{IOB} = 15 pF	1.65-3.6	1.65-3.6	—	0.8	3	ns
t_{RA}	A port Rise Time	C_{IOA} = 15 pF	1.65-3.6	1.65-3.6	—	1	4	ns
t_{FA}	A port Fall Time	C_{IOA} = 15 pF	1.65-3.6	1.65-3.6	—	0.8	3	ns
t_{PD_AB}	Propagation Delay (Driving B port)	C_{IOB} = 15 pF	1.65-3.6	1.65-3.6	—	3	10	ns
		C_{IOB} = 30 pF	1.65-3.6	1.65-3.6	—	5	15	
		C_{IOB} = 50 pF	1.65-3.6	1.65-3.6	—	8	18	
		C_{IOB} = 100 pF	1.65-3.6	1.65-3.6	—	12	20	
t_{PD_BA}	Propagation Delay (Driving A port)	C_{IOA} = 15 pF	1.65-3.6	1.65-3.6	—	3	10	ns
		C_{IOA} = 30 pF	1.65-3.6	1.65-3.6	—	5	15	
		C_{IOA} = 50 pF	1.65-3.6	1.65-3.6	—	8	18	
		C_{IOA} = 100 pF	1.65-3.6	1.65-3.6	—	12	20	
t_{SK}	Channel-to-Channel Skew	C_{IOB} = 15pF, C_{IOA} = 15pF	1.65-3.6	1.65-3.6	—	-	0.15	ns
t_{PZHB}	B port Output Enable Time	C_{IOB} = 15pF, I/O_A = V_{CCA}	1.65-3.6	1.65-3.6	—	120	250	ns
t_{PZLB}		C_{IOB} = 15pF, I/O_A = 0V	1.65-3.6	1.65-3.6	—	80	200	
t_{PZHA}	A port Output Enable Time	C_{IOA} = 15pF, I/O_B = V_{CCB}	1.65-3.6	1.65-3.6	—	120	250	ns
t_{PZLA}		C_{IOA} = 15 pF, I/O_B = 0 V	1.65-3.6	1.65-3.6	—	50	200	
t_{PHZB}	B port Output Disable Time	C_{IOB} = 15pF, I/O_A = V_{CCA}	1.65-3.6	1.65-3.6	—	200	400	ns
t_{PLZB}		C_{IOB} = 15pF, I/O_A = 0V	1.65-3.6	1.65-3.6	—	60	175	
t_{PHZA}	A port Output Disable Time	C_{IOB} = 15pF, I/O_A = V_{CCA}	1.65-3.6	1.65-3.6	—	180	400	ns
t_{PLZA}		C_{IOB} = 15pF, I/O_A = 0V	1.65-3.6	1.65-3.6	—	50	175	
M_{IDR}	Maximum Data Rate	C_{IO} = 15pF	1.65-3.6	1.65-3.6	140	—	—	Mbps
		C_{IO} = 30pF	1.65-3.6	1.65-3.6	120	—	—	
		C_{IO} = 50pF	1.65-3.6	1.65-3.6	100	—	—	Mbps
		C_{IO} = 100pF	1.65-3.6	1.65-3.6	60	—	—	

Test Circuits

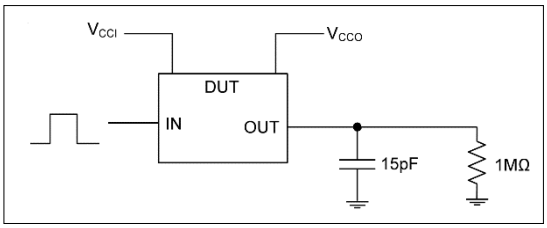
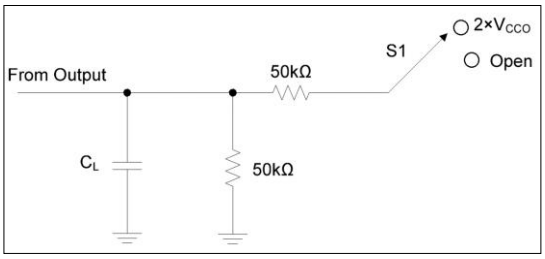


Figure 2 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement



TEST	S1
tPZL / tPLZ	2 × VCCO
tPHZ / Tpzh	Open

Figure 3 Load Circuit for Enable-Time and Disable-Time Measurement

Notes:

1. CL includes probe and jig capacitance.
2. ten is the same as tPZL and tPZH. tdis is the same as tPLZ and tPHZ.
3. VCCI is the supply voltage associated with the input.
4. VCCO is the supply voltage associated with the input.

Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤10 MHz
- Z_O = 50 Ω
- dv/dt ≥1 V/ns

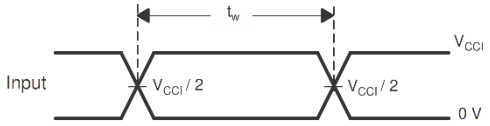


Figure 4 Pulse Duration

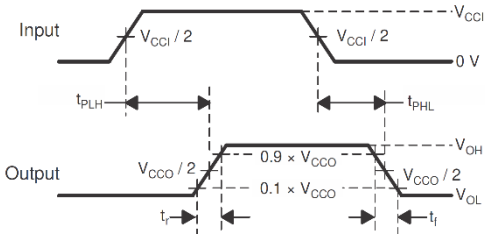
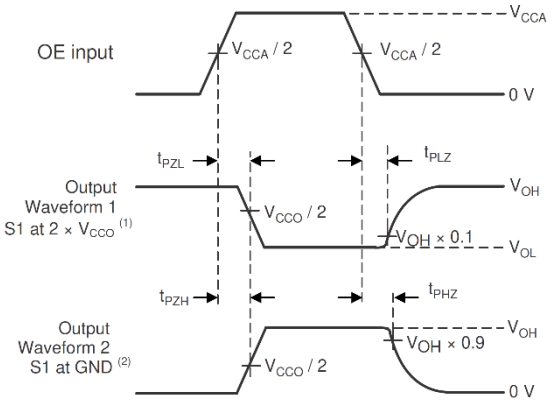


Figure 5 Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.

B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 6 Enable and Disable Times

Functional Description

The RS7LS304 is a 4-bit configurable dual-supply autosensing bidirectional level translator that does not require a direction control pin. The B and A ports are designed to track two different power supply rails, VCCB and VCCA respectively.

The RS7LS304 offers the feature that the values of the VCCB and V_{CCA} supplies are independent. Design flexibility is maximized because VCCA can be set to a value either greater than or less than the VCCB supply.

The RS7LS304 has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. Another feature of the RS7LS304 is that each An and Bn channel can function as either an input or an output.

An Output Enable (EN) input is available to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current.

Application Information

Level Translator Architecture

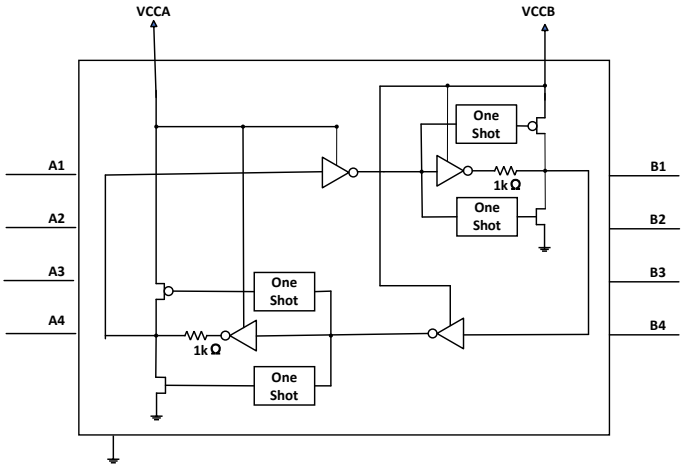


Figure 7: Architecture

The RS7LS304 auto-sense translator provides bi-directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, V_{CCA} and V_{CCB}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the I/O V_{CCA} to the I/O V_{CCB} ports, input signals referenced to the V_{CCA} supply are translated to output signals with a logic level matched to VCCB. In a similar manner, the I/O V_{CCB} to I/O V_{CCA} translation shifts input signals with a logic level compatible to V_{CCB} to an output signal matched to V_{CCA}. The RS7LS304 translator consists of bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. One-shot circuits are used to detect the rising or falling input signals. In addition, the one-shots decrease the rise and fall times of the output signal for high-to-low and low-to- high transitions.

Input Driver Requirements

Auto-sense translators such as the RS7LS304 have a wide bandwidth, but a relatively small DC output current rating. The high bandwidth of the bi-directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. The I/O ports have a modest DC current output specification so that the output driver can be over driven when data is sent in the opposite direction. For proper operation, the input driver to the auto-sense translator should be capable of driving 3mA of peak output current. The bi-directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

Enable Input (EN)

The RS7LS304 translator has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CCB} and I/O V_{CCA} pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_{CCA} supply and has Over-Voltage Tolerant (OVT) protection.

Uni-Directional versus Bi-Directional Translation

The RS7LS304 translator can function as a non-inverting uni-directional translator. One advantage of using the translator as a uni-directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

The values of the V_{CCA} and V_{CCB} supplies can be set to anywhere in range 1.65-3.6V and 1.65-3.6V. Design flexibility is maximized because V_{CCA} may be either greater than or less than the V_{CCB} supply. In contrast, the majority of the competitive auto sense translators has a restriction that the value of the V_{CCA} supply must be equal to less than (V_{CCB} - 0.4) V. The sequencing of the power supplies will not damage the device during power-up operation. In addition, the I/O V_{CCB} and I/O V_{CCA} pins are in the high impedance state if either supply voltage is equal to 0V. For optimal performance, 0.01 to 0.1μF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

The RS7LS304 translators have a power down feature that provides design flexibility. The output ports are disabled when either power supply is off (V_{CCA} or V_{CCB} = 0V). This feature causes all of the I/O pins to be in the power saving high impedance state.

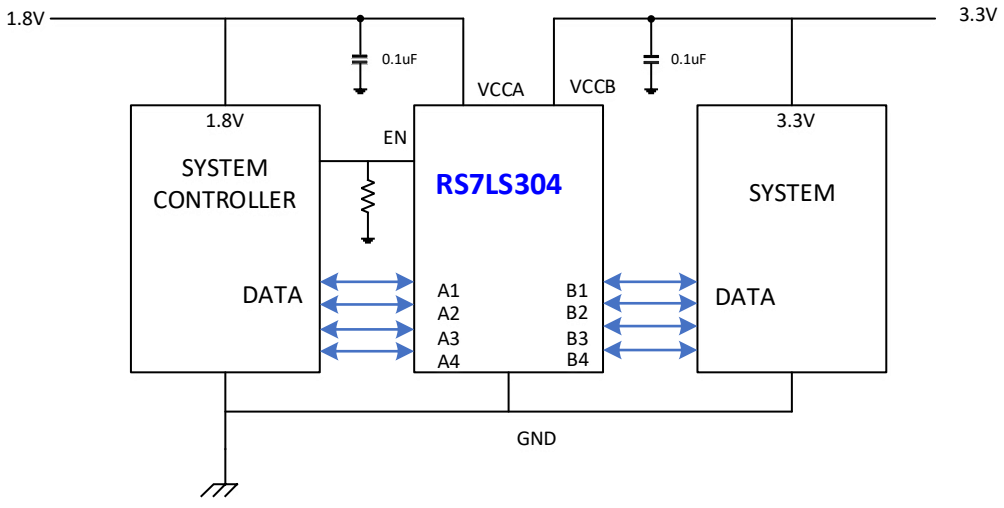
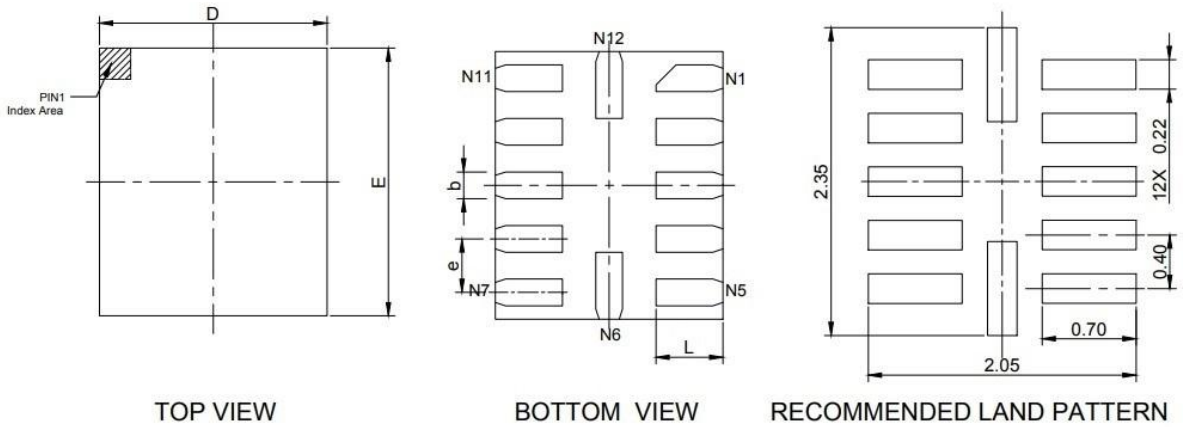


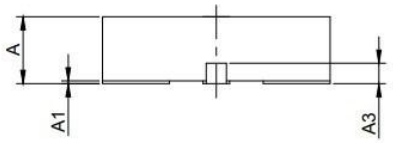
Figure 8. Typical Application

Package Information

UQFN 1.7x2.0-12L



TOP VIEW BOTTOM VIEW RECOMMENDED LAND PATTERN



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
D	1.65	1.75
E	1.95	2.05
b	0.15	0.25
e	0.40 TYP	
L	0.45	0.55

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-287A
4. Recommended land pattern is for reference only.

UQFN1.7X2.0-12L (ZM12) POD Rev.0
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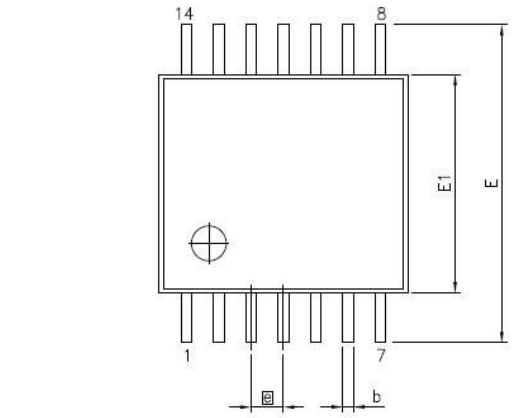
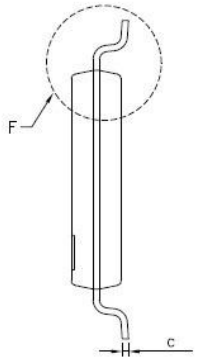
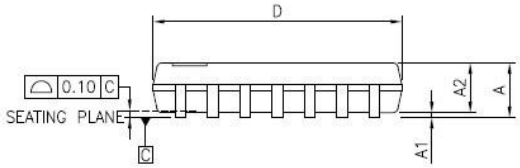
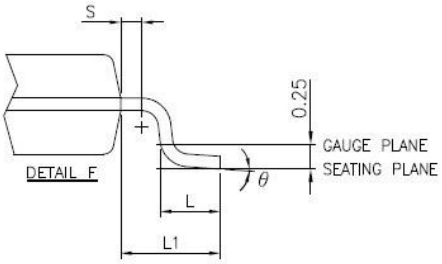
TSSOP-14L





SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MO-153F

4. Recommended land pattern is for reference only.

TSSOP14 POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	DATE
1.0	Initial Release	2022/11
1.1	Add document number	2024/10/31
1.2	Update application diagram	2025/7/7