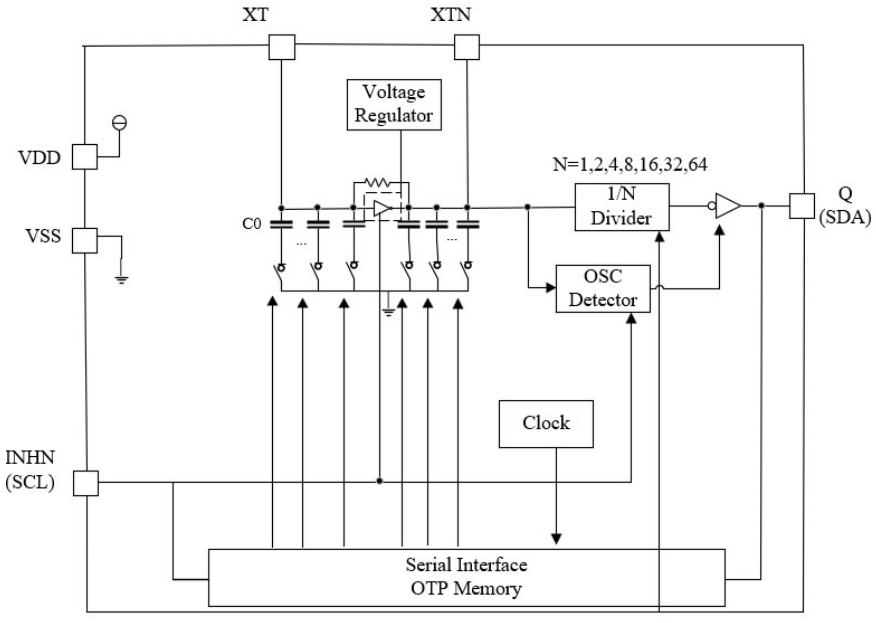
Function Description

The XO7101 series are crystal oscillator module CMOS ICS with f0 adjustment function. It supports 16MHZ to 100MHZ fundamental-frequency and +125C operation. The oscillator circuit stage has a voltage regulator drive, which reduces current consumption and frequency deviation due to fluctuations in the supply voltage. Even with an f0 adjustment function built in, the miniature chip size enables it to be implemented in a 1612 or 2016 size package

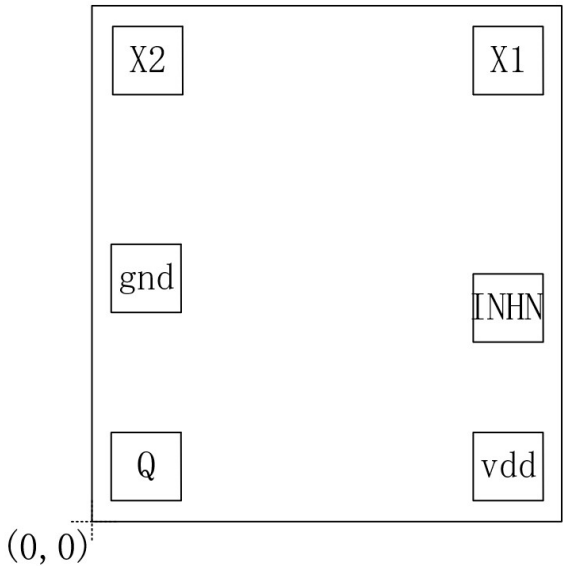
Feature

- Operating supply voltage, 1.6V to 3.63V
- Recommended oscillation frequency (Fundamental-frequency): 16MHZ to 100MHZ
- Output frequency: 0.25MHZ to 100MHZ
- Operating temperature: -40 to +125°C
- Chip size: X=0.605mm.Y=0.66mn
- Output level: CMOS
- Embedded memory: Nonvolatile memory (OTP: One Time Programmable)
- f0 adjustment function
  - Adjustment method: OTP Memory writing
  - Oscillator load capacitance (CL): 5pF
  - Frequency adjustment range: ±30ppm(min)
  - Frequency adjustment resolution: 1. 5ppm/bit(max)
- Frequency division function:
- -Setting method: OTP Memory writing
- -Selectable divider's ratio:1/2,1/4,1/8,1/16,1/32,1/64
- a Phase noise characteristics(typ.)
- f_{OSC}=40 MHZ, VDD=3.3V: -87dBc/Hz@10HZ, -140 dBc/Hz @1KHZ, -157 dBc/Hz @100KHZ
- Output 3-state function
- Low standby current(oscillator stopped, power saving pull-up resistor)
- Oscillation detection circuit built-in

Block Diagram



Pad Configuration



Pad Coordinate File					
Pad Name	X Coordinate	Y Coordinate	Pad Name	X Coordinate	Y Coordinate
XT	480.69	535.37	Q(SDA)	63.375	63.36
XTN	63.41	535.37	VDD	480.695	63.36
GND	271.955	299.365	INHN (SCL)	480.695	249.17
Die Size: 605μm*660μm (Including scribe line , Scribe Line Width 60um) **Die Thickness:** 130μm±15μm(-3) , 100um±15um(-4)					
Pad Size: 80um*80um					

Pad Definition

Name	I/O	Function
XT	I	Crystal element connection pins Connect crystal between XT and XTN pins
XTN	O	
VDD	-	Supply voltage
Q(SDA)	O (I/O)	oscillator output f_{osc}, $f_{osc}/2$, $f_{osc}/4$, $f_{osc}/8$, $f_{osc}/16$, $f_{osc}/32$, $f_{osc}/64$ frequency output. In program mode, SDA pin is the serial interface data input/output
VSS	-	Ground
INHN (SCL)	I (I)	Output state control input(Inhibit)pin. Oscillator is stopped in standby mode when LOW Pull-up resistor built-in In program mode, SCL pin is the serial interface Clock input

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Supply voltage range	VDD	Voltage between VDD and VSS	-0.3 to +4.5	V	*1
Program input voltage range	VPP	Voltage between INHN and VSS	-0.3 to +6.75	V	*1.*5
Input voltage range l	V_{INl}	INHN pin	-0.3 to VDD+0.3	V	*1，*2，*5
Input voltage range 2	V_{IN2}	XT pin	-0.3 to +2.5	V	*1.*2
Output voltage range 1	V_{OUTl}	Q pin	-0.3 to VDD+0.3	V	*1，*2，*5
Output voltage range 2	V_{OUT2}	XTN pin	-0.3 to +2.5	V	*1.*2
Output current	I_{OUT}	Q pin	±20	mA	*3
Junction temperature	T_j		150	°C	*3
Storage temperature range	T_{STG}	Chip form wafer form	-55to+150	°C	*4

Note:
1. Absolute maximum ratings are the values that must never be exceeded, even for a moment. This product may suffer breakdown if anyone of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.
2. VDD is the VDD value of recommended operating conditions.
3. Do not exceed the absolute maximum ratings. If they are exceeded, device characteristics and reliability will be degraded.
4. When stored alone in nitrogen or vacuum atmosphere.
5. Refer to “RECOMMENDED OPERATING CONDITIONS(OTP MEMORY PROGRAMMING) ”for OTP memory programming.

Recommended Operating Condition

(V_{SS}=0V，Ta=－40℃~+125℃)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Oscillator frequency	f_{OSC}	VDD=1.6 to 3.63V	16		100	MHz	*1
Output frequency	f_{OUT}	VPP=1.6 to 3.63V	0.25		100	MHz	
Operating supply voltage	V_{DD}	Voltage between V_{DD} and V_{SS}	1.6		3.63	V	*2
Input voltage l	V_{IN1}	INHN Pin	V_{SS}		V_{DD}	V	
Input voltage 2	V_{IN2}	XT pin	V_{SS}		2.0	V	
Operating temperature	Ta		-40		+125	°C	
Output load capacitance	C_L	Q pin			15	pF	
OTP Memory data retention		Ta=-40 to 125°c	10			year	

Note:
1. The oscillation frequency is a yardstick value and the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
2. For stable operation of this product, mount a ceramic chip capacitor of 0.01uF or larger between VDD and VSS in close proximity to IC(within 3mm) .Wiring pattern between IC and capacitor should be as thick as possible.

DC Characteristics

Current consumption (f_{OSC}=40MHz)

V_{DD}=1.6 to 3.63V, V_{SS}=0V, Ta=-40 to+125°C unless otherwise noted

Symbol	Parameter	Conditions		MIN	TYP	MAX	Unit
I_{DD}*1	Current consumption Fundamental (DSL Code=0H)	Measurement circuit 1 INHN =OPEN， no load， f_{OSC}=40MHz， f_{OUT}=40MHz	V_{DD}=1.8V		1.00	1.70	mA
			V_{DD} =2.5V		1.30	2.00	
			V_{DD} =3.3V		1.70	2.40	
	Current consumption Divide -by-2 (DSL Code=1H)	Measurement circuit 1， INHN=OPEN， no load， f_{OSC}=40MHz， f_{OUT}=20MHz	V_{DD} =1.8V		0.75	1.35	mA
			V_{DD} =2.5V		0.95	1.55	
			V_{DD} =3.3V		1.15	1.75	
	Current consumption Divide -by-4 (DSL Code=2H)	Measurement circuit 1， INHN=OPEN， no load， f_{OSC}=40MHz, f_{OUT}=10MHz	V_{DD} =1.8V		0.60	1.15	mA
			V_{DD} =2.5V		0.75	1.30	
			V_{DD} =3.3V		0.90	1.45	
	Current consumption Divide -by-8 (DSL Code=3H	Measurement circuit 1， INHN=OPEN， no load， f_{OSC}=40MHz， f_{OUT}=5MHz	V_{DD} =1.8V		0.55	1.05	mA
			V_{DD} =2.5V		0.65	1.15	
			V_{DD} =3.3V		0.75	1.25	
	Current consumption Divide -by-16 (DSL Code-4H)	Measurement circuit 1， INHN=OPEN， no load， f_{OSC}=40MHz， f_{OUT}=2.5MHz	V_{DD} =1.8V		0.50	1.00	mA
			V_{DD} =2.5V		0.60	1.10	
			V_{DD} =3.3V		0.70	1.20	
	Current consumption Divide -by-32 (DSL Code=5H)	Measurement circuit 1， INHN=OPEN， no load， f_{OSC}=40MHz， f_{OUT}=1.25MHz	V_{DD} =1.8V		0.45	0.90	mA
			V_{DD} =2.5V		0.55	1.00	
			V_{DD} =3.3V		0.65	1.10	
	Current consumption Divide -by-64 (DSL Code=6H)	Measurement circuit 1， INHN=OPEN， no load， f_{OSC}=40MHz， f_{OUT}=0.625MHz	V_{DD} =1.8V		0.45	0.90	mA
			V_{DD} =2.5V		0.50	0.95	
			V_{DD} =3.3V		0.60	1.05	

Note:
1. The consumption current $I_{DD}(C_{LOUT})$with a load capacitance (C_{LOUT})connected to the Q pin is given by following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency

$I_{DD}(C_{LOUT})$[mA] = I_{DD}[mA] + C_{LOUT}[pF] * V_{DD}[V] * f_{OUT}[MHz] * 10^{-3}

Current consumption

(fOSC=96MHz)

V_{DD}=1.6 to 3.63V, V_{SS}=0V, Ta=-40 to+125°C unless otherwise noted

Symbol	Parameter	Conditions		MIN	TYP	MAX	Unit
IDD*1	Current consumption Fundamental (DSL Code=0H)	Measurement circuit 1 INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=96MHz	V_{DD}=1.8V		2.00	2.70	mA
			V_{DD} =2.5V		2.65	3.35	
			V_{DD} =3.3V		3.50	4.20	
	Current consumption Divide -by-2 (DSL Code=1H)	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=48MHz	V_{DD} =1.8V		1.30	1.90	mA
			V_{DD} =2.5V		1.70	2.30	
			V_{DD} =3.3V		2.20	2.80	
	Current consumption Divide -by-4 (DSL Code=2H)	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=24MHz	V_{DD} =1.8V		1.00	1.55	mA
			V_{DD} =2.5V		1.25	1.80	
			V_{DD} =3.3V		1.55	2.10	
	Current consumption Divide -by-8 (DSL Code=3H	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=12MHz	V_{DD} =1.8V		0.80	1.30	mA
			V_{DD} =2.5V		1.00	1.50	
			V_{DD} =3.3V		1.20	1.70	
	Current consumption Divide -by-16 (DSL Code-4H)	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=6MHz	V_{DD} =1.8V		0.75	1.25	mA
			V_{DD} =2.5V		0.90	1.40	
			V_{DD} =3.3V		1.05	1.55	
	Current consumption Divide -by-32 (DSL Code=5H)	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=3MHz	V_{DD} =1.8V		0.70	1.15	mA
			V_{DD} =2.5V		0.80	1.25	
			V_{DD} =3.3V		0.95	1.40	
	Current consumption Divide -by-64 (DSL Code=6H)	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=96MHz, f_{OUT}=1.5MHz	V_{DD} =1.8V		0.70	1.15	mA
			V_{DD} =2.5V		0.80	1.25	
			V_{DD} =3.3V		0.90	1.35	

Note:

1. The consumption current $I_{DD}(C_{LOUT})$with a load capacitance (C_{LOUT})connected to the Q pin is given by following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency

$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA] + C_{LOUT}[pF] * V_{DD}[V] * f_{OUT}[MHz] * 10^{-3}$

Other DC characteristics

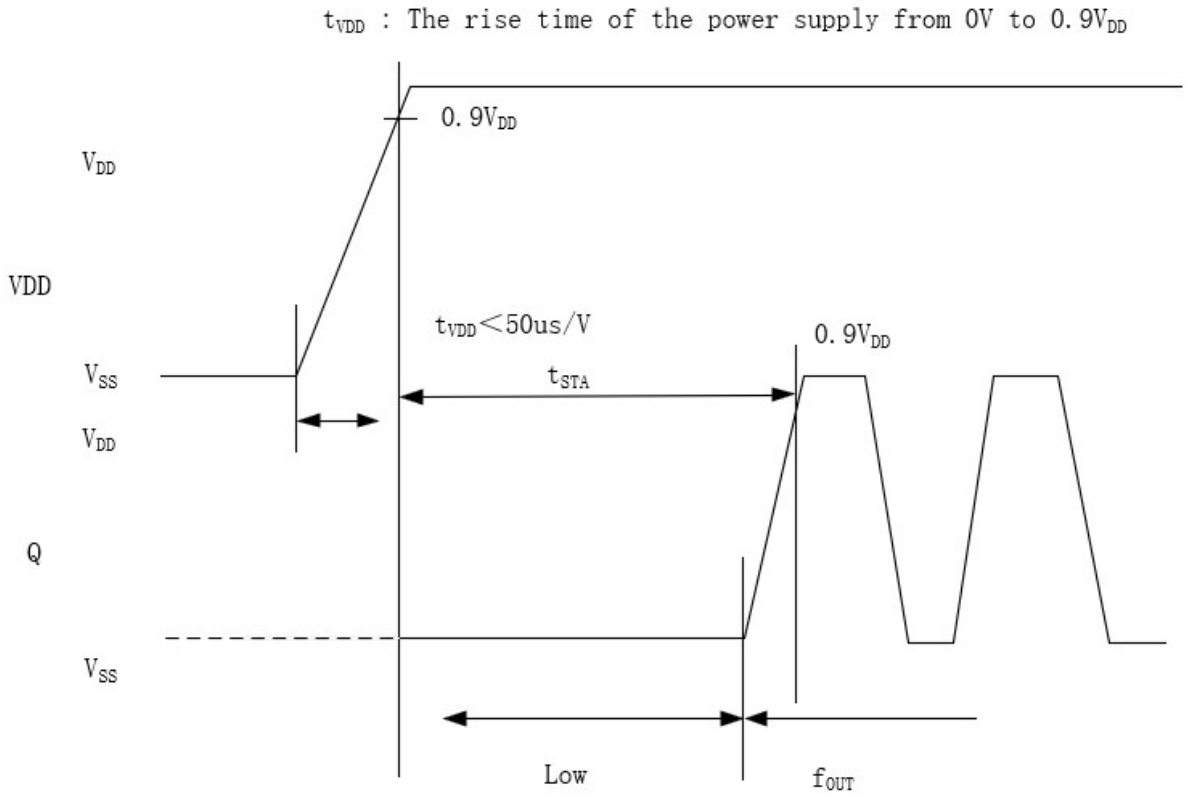
V_{DD}=1.6 to 3.63V, V_{SS}=0V, Ta=-40 to+125°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
HIGH-level output voltage	V_{OH}	Q pin，Measurement circuit 2, I_{OH}=-4mA		V_{DD}-0.4		V_{DD}	V
		Q pin，Measurement circuit 2, I_{OH}=-1mA		0.9V_{DD}		V_{DD}	V
LOW-level output voltage	V_{OL}	Q pin，Measurement circuit 3，I_{OL}=4mA		0		0.4	V
		Q pin，Measurement circuit 3，I_{OL}=1mA		0		0.1V_{DD}	V
HIGH-level input voltage	V_{IH}	INHN pin， Measurement circuit 4		0.7V_{DD}			V
LOW-level input voltage	V_{IL}	INHN pin， Measurement circuit 4				0.3V_{DD}	V
Output leakage current	I_Z	Q pin，INHN =V_{SS} Measurement circuit 5	Q=V_{DD}			10	μA
			Q=V_{SS}	-10			
Standby current	I_{ST}	Measurement circuit 1， INHN=V_{SS}				10	μA
pull-up resistance	R_{PU1}	INHN pin， Measurement circuit 4		1	2	3	MΩ
	R_{PU2}	INHN pin， Measurement circuit 4		200	250	300	kΩ
Oscillator feedback resistance	R_f	Measurement circuit 6		50	100	200	kΩ

Oscillator Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillation start voltage	V_{STR}	V_{DD} slowly increasing， Measurement circuit 7			1.5	V
Frequency adjustment range	Δf/f	F0 Code：00H(=60H) Center，Ta=25℃ F0 Code range=01H to FFH	±30			ppm
Frequency adjustment resolution	Δf_{RES}	F0 Code：00H(=60H) Center,Ta=25℃ Frequency fluctuation by 1 code unit in the Frequency adjustment range			1.5	ppm
Oscillator minimum load capacitance	C_{LMIN}	C_L minimum setting， Ta=25℃ F0 Code=01H， CLS Code=0H		3.25		pF
Oscillator maximum load capacitance	C_{LMAX}	C_L maximum setting， Ta=25℃ F0 Code=FFH， CLS Code=3H		9.83		pF
Oscillator start time	t_{STA}	Ta=25℃， VDD applied(rising edge：0-90%ofVpD) ， V_{OH} and V_{OL} ratings nominal， Measurement circuit 7			2	ms

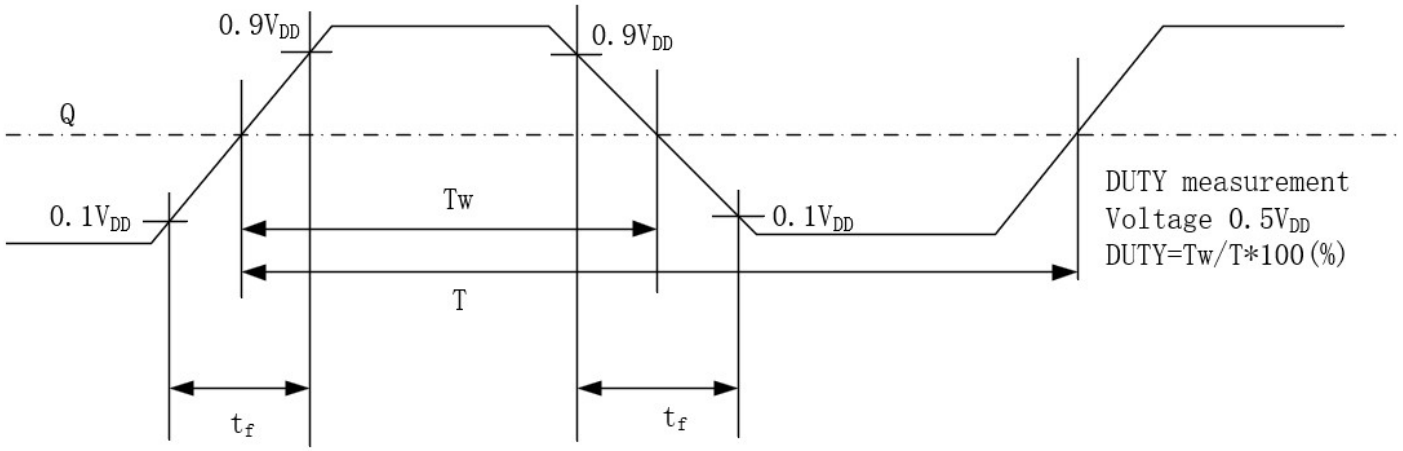
Timing Diagrams



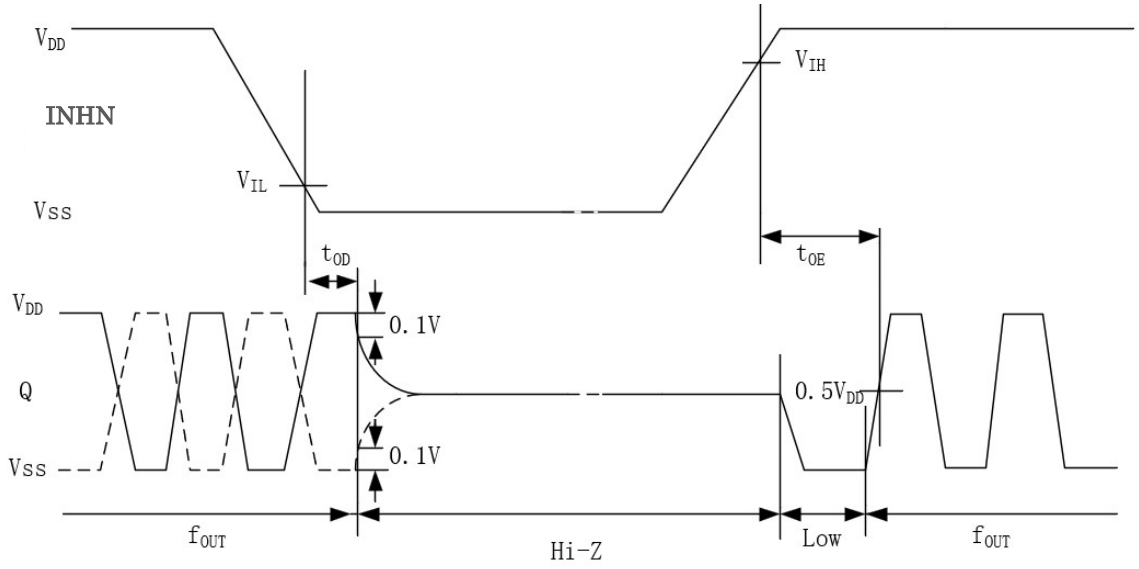
Clock Output Characteristics

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Rise time	Tr	Q pin, Measurement circuit 1, C_{LOUT}=15pF, 0.1VDD→0.9VDD	VDD=1.6 to 2.25V		1.8	5.0	ns
			VDD=2.25 to 2.97V		1.2	3.0	ns
			VDD=2.97 to 3.63V		0.9	2.5	ns
Fall time	Tf	Q pin, Measurement circuit 1, C_{LOUT}=15pF, 0.1VDD→0.9VDD	VDD=1.6 to 2.25V		1.8	5.0	ns
			VDD=2.25 to 2.97V		1.2	3.0	ns
			VDD=2.97 to 3.63V		0.9	2.5	ns
Output duty cycle	DUTY	Q pin, Measurement circuit 1, Ta=25°C, C_{LOUT} r≤15pF		45	50	55	%
Output enable delay time	t_{OE}	Q pin, Measurement circuit 7, design value, Ta=25°C, CLOUT≤15pF, INHN=Low→High				2	ms
Output disable delay time	t_{OD}	Q pin, Measurement circuit 7, design value, Ta=25°C, Cl our≤15pF, INHN=High→Low				200	ns

Output switching waveform



Output disable and enable time



When INHN goes HIGH to LOW, the Q output becomes high impedance.

When INHN goes LOW to HIGH, the Q output goes low once and then becomes normal output operation after having detected oscillation signals.

Recommended operating conditions(OTP memory programming)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating supply voltage	V_{DD}[1]		3.0		3.63	V
OTP memory programming supply voltage	V_{PP}	SCL(INHN) pin	6.25	6.5	6.75	V
Operating temperature	T.		0		+50	℃

Note

1.For stable operation of this product, mount a ceramic chip capacitor of 0.01u For larger between VDD and VSS

Electrical characteristics(OTP memory programming)

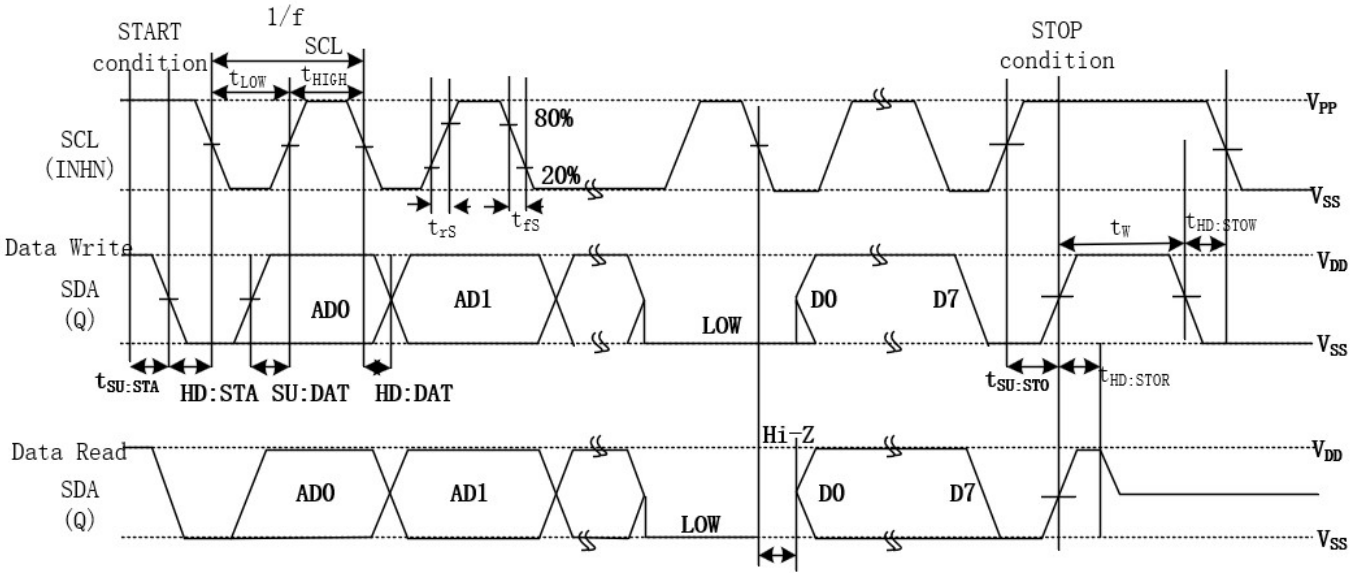
DC characteristics (2-wire type serial interface)

V_{PP}=6.25 to 6.75V, V_{DD}=3.0 to 3.63V, Vss=0V, Ta= 0 to+50°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL(INHN) pin HIGH-level input voltage	V_{IHC}	SCL(INHN) pin	V_{DD}+1.7V			V
SCL(INHN) pin LOW-level input voltage	V_{ILC}	SCL(INHN) pin			0.3V_{DD}	V
SDA(Q) pin HIGH-level input voltage	V_{IHD}	SDA(Q) pin	0.7V_{DD}			V
SDA(Q) pin LOW-level input voltage	V_{ILD}	SDA(Q) pin			0.3V_{DD}	V
SDA(Q) pin HIGH-level output y oltage	V_{OHD}	SDA(Q) pin， I_{OHD}=-0.1mA	V_{DD}-0.4V		V_{DD}	V
SDA(Q) pin LOW-level output voltage	V_{OLD}	SDA(Q) pin， I_{OLD}=0.1mA	0		0.4	V

AC characteristics (2-wire type serial interface)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL clock frequency	f_{SCL}	After program start condition	25		500	kHz
Start condition setup time	$t_{SU:STA}$		0.3			μs
Start condition hold time	$t_{HD:STA}$		0.3			μs
Data setup time	$t_{SU:DAT}$		0.3			μs
Data hold time	$t_{HD:DAT}$		0.3			μs
Stop condition setup time	$t_{SU:STO}$		0.3			μs
Stop condition hold time	$t_{SU:STOW}$	Write the data to OTP memory	0.3			μs
	$t_{HD:STOR}$	Read the data to OTP memory Access the registers	0.2			μs
OTP memory write time	t_W		150	200	250	μs
SCL LOW-period	t_{LOW}					μs
SCL HIGH-period	t_{HIGH}					μs
SCL rise time	rs	20%→80%			0.2	μs
SCL fall time	Lis	80%→20%			0.2	μs
Read data delay time	RD	CL our=15pF			0.5	μs



Function Description

INHN function

The INHN pin switches the IC between normal operating/standby mode and serial interface mode, depending on the input voltage.
When INHN is left open-circuit or tied to HIGH level, the IC is in normal operating mode. When INHN is tied to LOW level, the IC enters standby mode. The Q output becomes high-impedance and the oscillator circuit stop When the INHN pin voltage is between V_{IHC} and V_{PP}(4.7V[min] ~ 6.75[max]), the device enters serial interface mode.

INHN pin	Q pin	Oscillator	Mode
High or Open	f_{OUT}	Operating	Normal operating mode
LOW	Hi-Z	Stopped	Standby mode
VIHC ≤ V_{PP}(SCL)	SDA	Operating	Serial interface mode

Power Saving Pull-up Resistor

The INHN Pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level(HIGH or LOW)
When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), and the internal circuit of INHN becomes HIGH level.
Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation election Function and Power ON Reset Function

The 7101 series have an oscillation detection circuit.
The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit Starts up. This function avoids the abnormal oscillation during initial power up and when started again using INHN.
When oscillation is detected. the serial interface internal circuits are initialized and the data written to OTP memory is read out.

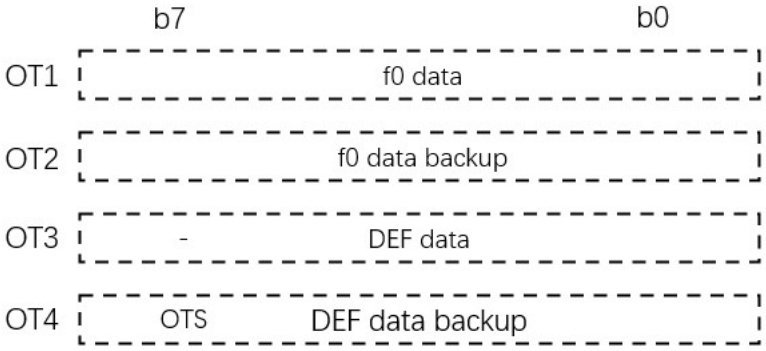
OTP Memory Function and Register Function

OTP Memory, Register Map

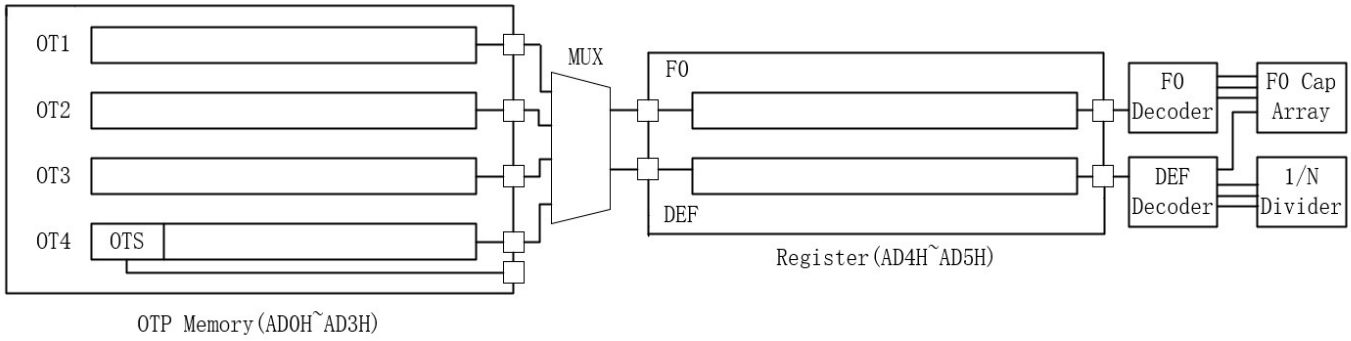
The 7101 series has a 4-bit address used to access the OTP memory or register
Users can use addresses OH to 5H and FH. Addresses 6H to EH are used for = device testing. Access in addresses 6H to EH is prohibited to prevent unstable operation.
During normal operation, f0 adjustment data and internal settings data in OTP memory are loaded after oscillation detection. You use settings data by writing to the OTP memory.
Backup memory is used when you want to change data written in memory to other data. Data in backup memory side is enabled by writing"1"to the OTS bit of address 3H(OT4), You can check the f0 adjustment and various settings using the register before data is written to the OTP memory.

Address	Memory	Function	Symbol	R/W	Initial value
00H	OTP	f0 adjustment memory	OT1	R/W	00H
01H		f0 adjustment memory backup	OT2	R/W	00H
02H		Internal setting memory	OT3	R/W	00H
03H		Internal setting memory backup	OT4	R/W	00H
04H	Register	f0 adjustment register	F0	W	Don't care
05H		internal setting register	DEF	R/W	00H
06H-0EH	Unusable (for IC testing)				
0FH	Register	OTP Memory Test	PTM	W	00H

OTP Memory(Address:00H-03H)



When the OTS bit is 0,OT1 and OT3 data is output.When the OTS bit is 1, the backup data is selected and OT2 and OT4 data is output.



F0 Adjustment Register F0 (Address:04H)

The F0 register is directly linked to the capacitor array connected to the XT and XTN terminals of the oscillator. It supports 255 gradations of adjustment, from 01H(minimum oscillator load capacitance code) to FFH(maximum oscillator load capacitance code).The F0 register is set to F0[7:0]= 60H when the F0 setting .This setting is in the OTP memory initial value 00H, is intended to be in the CL=5pF.Refer to the following table for code setting(design values).

z	Function		Capacitance(pF)	
	"ON"	"OFF"	XT	XN
b0	1	0	0.04	0.04
b1	1	0	0.08	0.08
b2	1	0	0.16	0.16
b3	1	0	0.32	0.32
b4	1	0	0.64	0.64
b5	1	0	1.28	1.28
b6	1	0	2.56	2.56
b7	1	0	5.12	5.12

Dec.	Hex.	Code								Capacitance array		C_L(pF)
		b7	b6	b5	b4	b3	b2	bl	b0	XT(pF)	XTN(pF)	
0	00	0	1	1	0	0	0	0	0	3.84	3.84	5.15
1	01	0	0	0	0	0	0	0	1	0.04	0.04	3.25
2	02	0	0	0	0	0	0	1	0	0.08	0.08	3.27
3	03	0	0	0	0	0	0	1	1	0.12	0.12	3.29
4	04	0	0	0	0	0	1	0	0	0.16	0.16	3.31
…												
88	58	0	1	0	1	1	0	0	0	3.52	3.52	4.99
89	59	0	1	0	1	1	0	0	1	3.56	3.56	5.01
90	5A	0	1	0	1	1	0	1	0	3.60	3.60	5.03
91	5B	0	1	0	1	1	0	1	1	3.64	3.64	5.05
92	5C	0	1	0	1	1	1	0	0	3.68	3.68	5.07
93	5D	0	1	0	1	1	1	0	1	3.72	3.72	5.09
94	5E	0	1	0	1	1	1	1	0	3.76	3.76	5.11
95	5F	0	1	0	1	1	1	1	1	3.80	3.80	5.13
96	60	0	1	1	0	0	0	0	0	3.84	3.84	5.15
97	61	0	1	1	0	0	0	0	1	3.88	3.88	5.17
…												
252	FC	1	1	1	1	1	1	0	0	10.08	10.08	8.27
253	FD	1	1	1	1	1	1	0	1	10.12	10.12	8.29
254	FE	1	1	1	1	1	1	1	0	10.16	10.16	8.31
255	FF	1	1	1	1	1	1	1	1	10.20	10.20	8.33

Internal settings of Register DEF (05H)

	b7	b5	b4	b3	b2	b0
DEF	unusable		CLS		DSL	

The DEF register is an internal settings register. It can switch the internal state, such as switching the frequency division factor. If you change the DEF register, in order to confirm that the state has changed writes to f0 adjustment register without exiting the serial interface mode. Along with the f0 adjustment register set value, it outputs the oscillation frequency of the modified internal state. Bits 5-7 are for device testing. When writing, write data 0 to this register.

Divider select bits DSL[2: 0]

The DSL bits switch the frequency division conditions. The DSL[2:0] =07H setting is for device testing. Its use is prohibited to prevent unstable operation

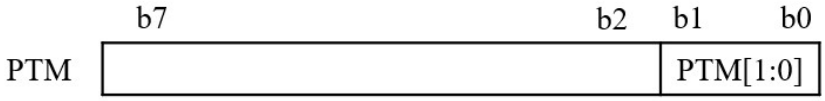
Output frequency	DSL[2:0]
f0 output	00H
f0/2 output	01H
f0/4 output	02H
f0/8 output	03H
f0/16 output	04H
f0/32 output	05H
f0/64 output	06H
Unusable	07H

C_L offset adjustment bits CLS[1:0]

The CLS bits switch the oscillator load capacitance offset adjustment value (design values).When the code 00H of f0 adjustment register has been set , CLS will be invalid.

C_L set value	CLS[1:0]
C_L	00H
C_L + 0.5pF	01H
C_L + 1.0pF	02H
C_L + 1.5pF	03H

OTP Memory Test Register PTM(Address:0FH)



The PTM bits switch the read condition to confirm strength of writing in OTP memory.Margin-1 Read Mode provides a read condition to confirm state of strength of writing in OTP memory. The OTP memory test Register is set to the Margin-1 Read Mode when the PTM[1:0]=3H setting. After writing the 3H in PTM, lead the Memory without exiting the serial interface mode.If you can correctly read the codes that you wrote in OTP memory, the strength of writing in OTP memory is guaranteed.

PTM[1:0]	Mode
0H	User Mode(Normal Mode)
3H	Margin-1 Read Mode

The factory setting of the IC

Function	State
Use memory	Main memory(Initial)Selectable memory：Main memory or Backup memory
f0 adjustment capacitor array	Ct=5.15pF(Initial)Selectable CL capacitance value range：3.25pF~9.83pF
frequency division conditions	Fundamental(Initial)Selectable division setting：Fundamental， fosc/2， fosc/4， fosc/8， fosc/16， fosc/32， fosc/64

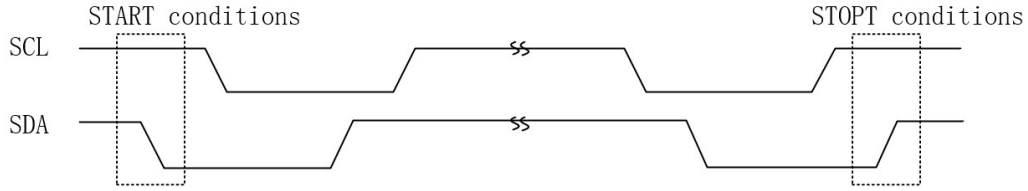
2-wire Serial Interface

Serial Interface Start Condition

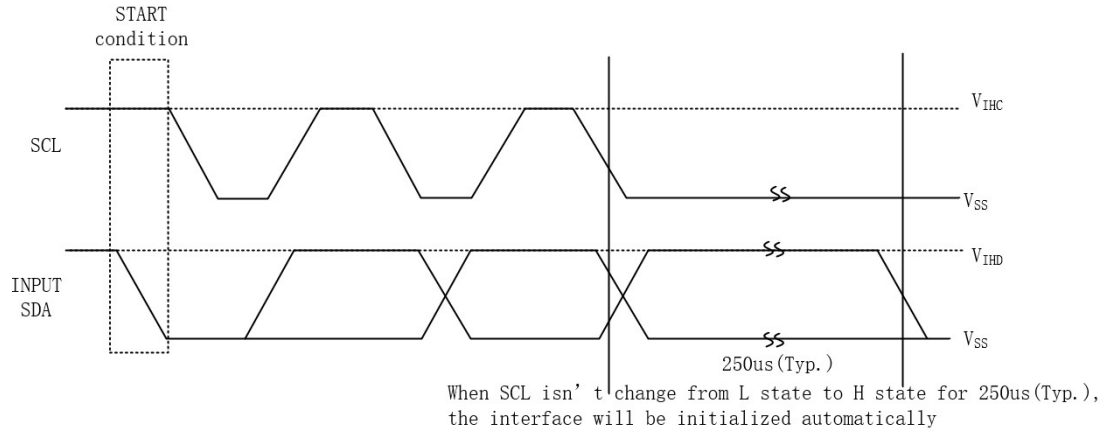
Oscillation detection is required to initialize the serial interface internal circuits .Start the serial interface when the oscillation startup time(t_{STA})has elapsed after power is applied. INHN pin control(INHN=LOW), start the serial interface when the enable delay time (t_{OE}) has elapsed after setting INHN open circuit or HIGH level. This start condition also applies when restarting after the serial interface is stopped.

Programming Start/Stop Conditions

Data is sent and received using a 2-wire serial interface comprising SCL(INHN clock line) and SDA(Q data line).Hold SCL and SDA both HIGH level when the serial interface is not transferring data. Device access starts when SDA goes from HIGH to LOW with SCL held HIGH(START condition), and then data can be transferred. Conversely, device access ends when SDA goes from LOW to HIGH with SCL held HIGH (STOP condition). These conditions can be accepted during data transfer, so data transfer should always start with the START condition and end with the STOP condition.



When a voltage V_{IHC} is applied to SCL, the output from the Q pin is disabled, and the device is in communication state. If the SCL clock is LOW level for 250 us(Typ) or longer during communications state the interface is initialized and communication ends



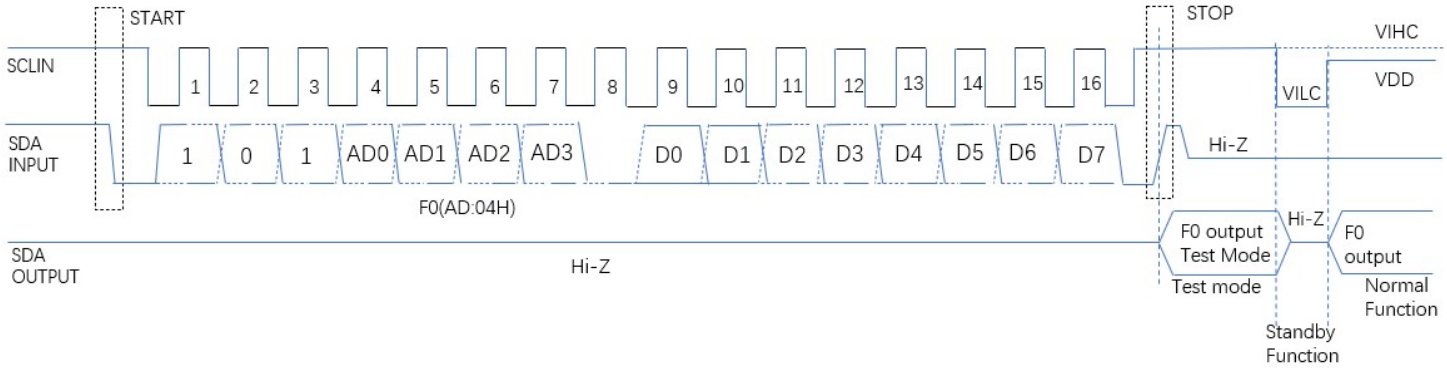
Register and OTP Memory Data Transfer Format

The register and OTP memory data transfer formats are described below. Data is always transferred with ISB first.

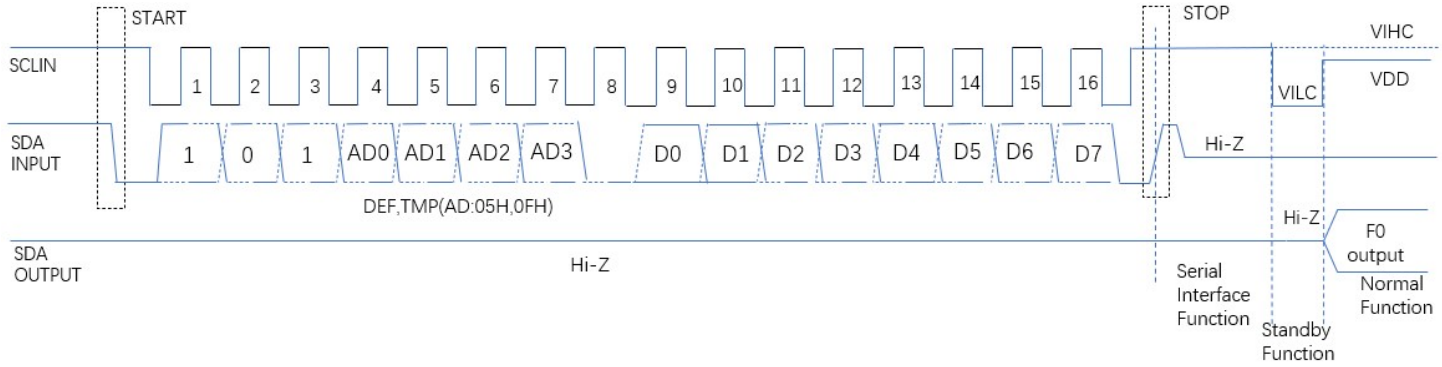
Data write Format

The transmitting device sends the START condition and 8-bit data comprising the write operation code (101), address, followed by a Low-level 8th bit. Followed by 8-bit data, 16-bit transfers in total, and then send the STOP condition.
When writing data to the register, data is written into the register in sync with the 16th on SCL. When writing to OTP memory, specify the OTP memory address and send the data and STOP condition. After sensing the STOP condition, maintain the write state (SCL=V_{PP}, SDA=V_{IHD})during the OTP memory write time(tw). Once the OTP memory write time has elapsed, set SDA to LOW level(V_{ILD}).To end serial communication and return to normal operation, set SCL to LOW level(V_{ILC})after the STOP.
condition, and set SDA open circuit(Hi-Z).

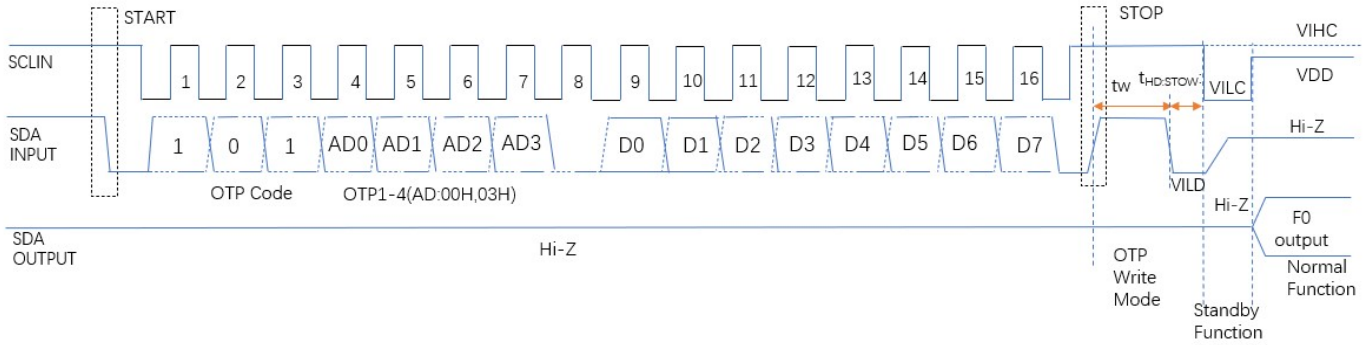
Register write timing （Address: 04H）



Register write timing （Address: 05H or 0FH）

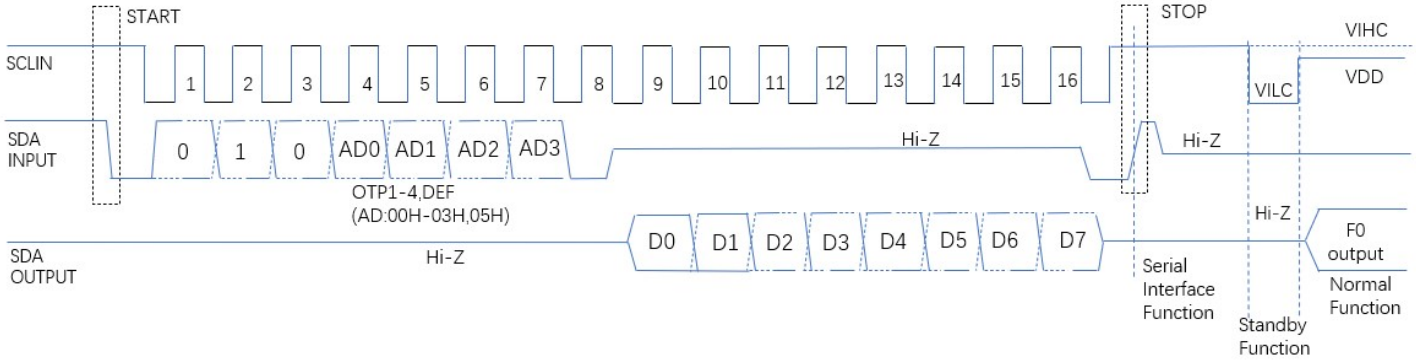


OTP memory write timing



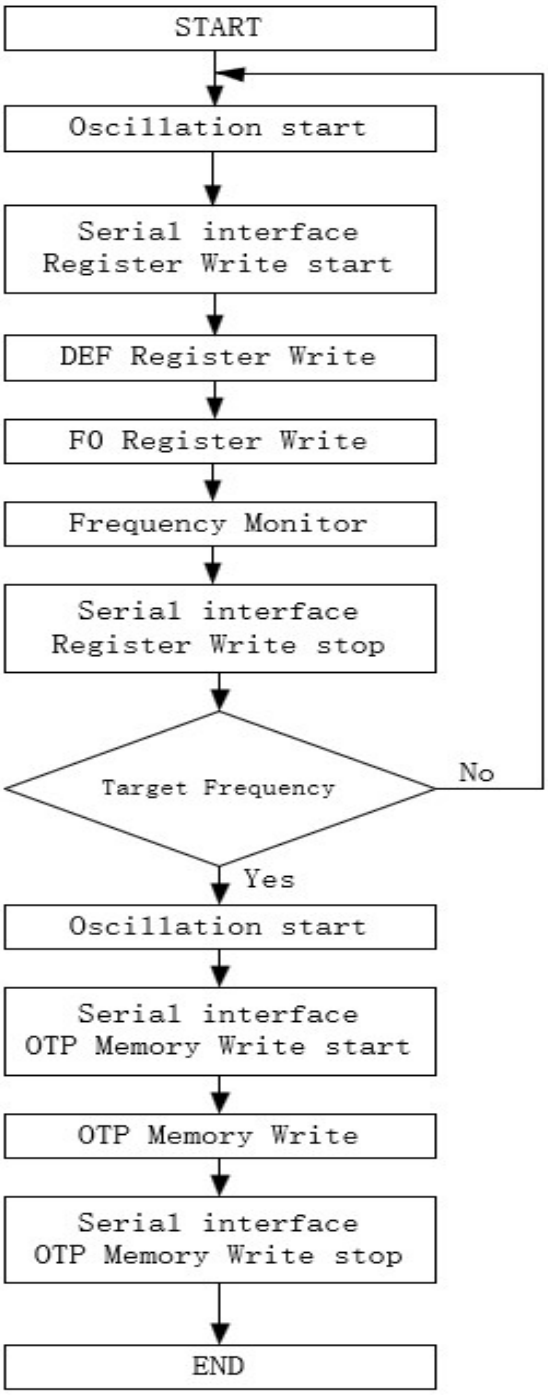
Data Read Format

When reading from OTP memory, the transmitter sends the START condition and 7-bit data comprising the read operation code (010) and address, followed by a Low-level 8th bit SDA goes open circuit (Hi-Z) on the SCL falling edge after 8 bits have been sent, and then data is output from SDA in sync with the, SCL falling edge.



f0 Adjustment Flow Chart

The following adjustment flow is an example. The flow will vary depending on the required frequency precision manufacturing process and adjustment environment.



When adjusting the frequency using the register, start the interface when the oscillation startup time(t_{STA}) or enable delay time (t_{OE})has elapsed after applying the START condition

.

After the interface starts, write data to the register. After writing to the DEF register (after sending the STOP condition), you can continue and write to the FO register by sending the START condition.

After writing to the F0 register(after sending the STOP(condition), monitor the frequency on the Q output.

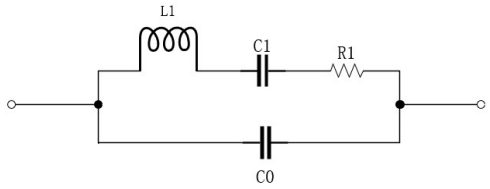
After the serial interface stops, check whether the target frequency is achieved, and readjust as necessary.

When writing to OTP memory, start the interface when the oscillation startup time(t_{STA}) has elapsed after sending the START condition.
After the interface starts, write the adjustment code obtained b:
the register write.
After writing to OTP memory (after sending the STOP condition), monitor the frequency on the Q output or read the OTP memory to check the written data, as necessary

Reference Data

The following characteristics are measured using the crystal below.
Note that the characteristics will vary with the crystal used.
Crystal used for measurement

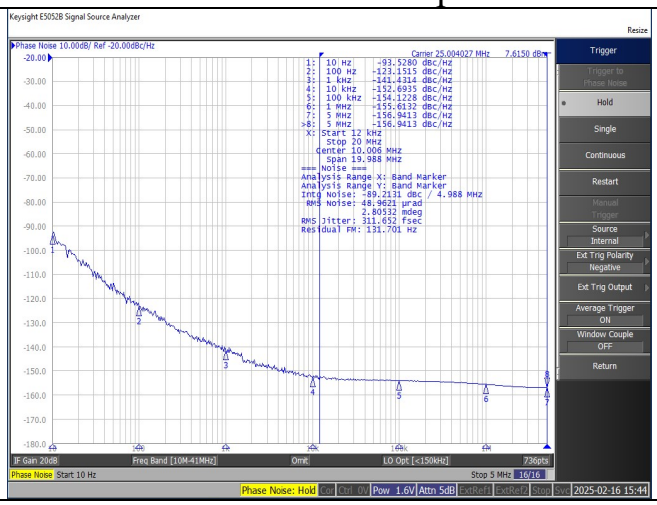
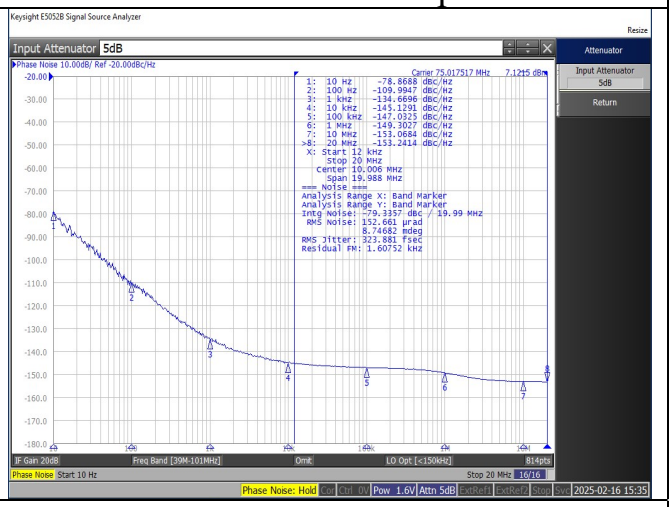
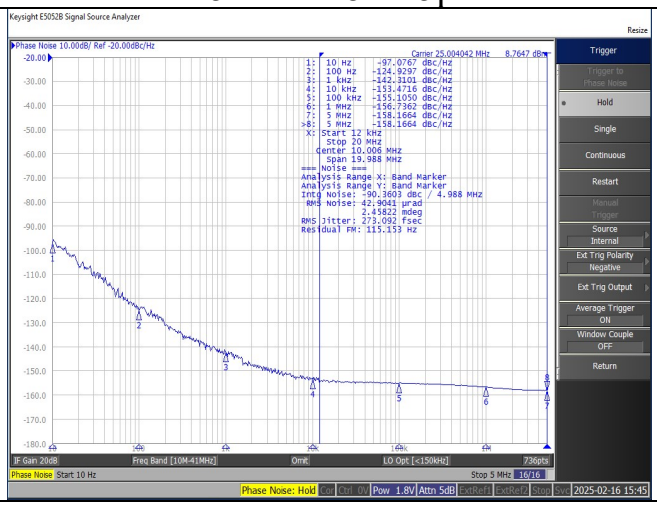
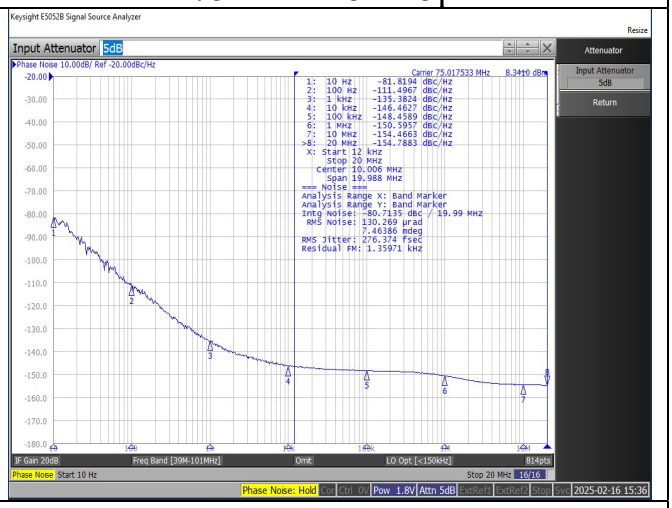
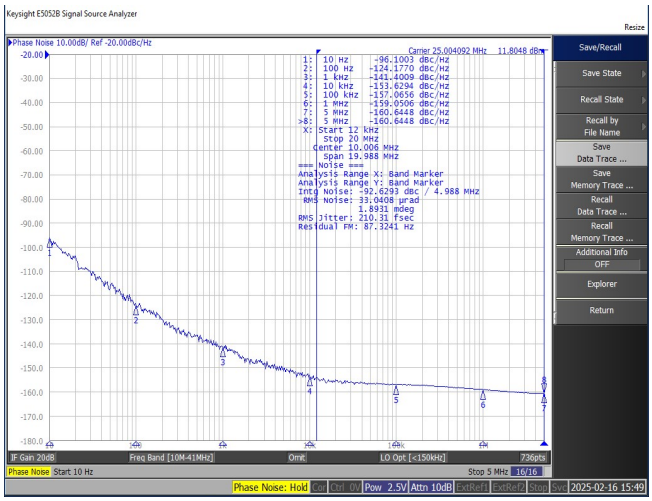
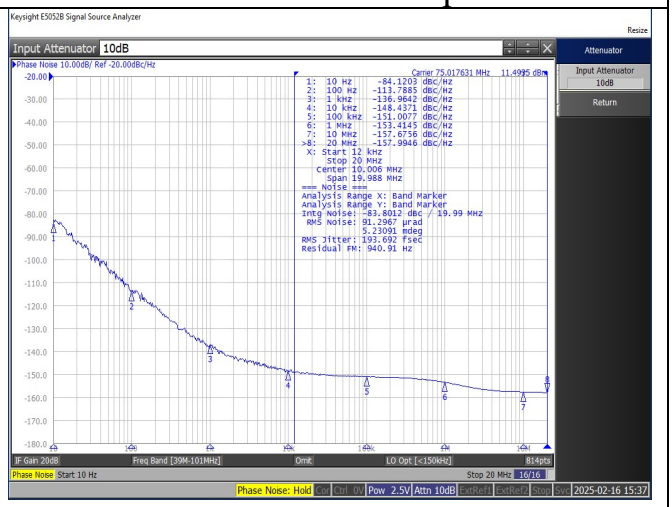
Parameter	40MHz	80MHz	100MHz
C0(pF)	1.5	2.4	2.1
R1(Ω)	27.5	6.3	8.1

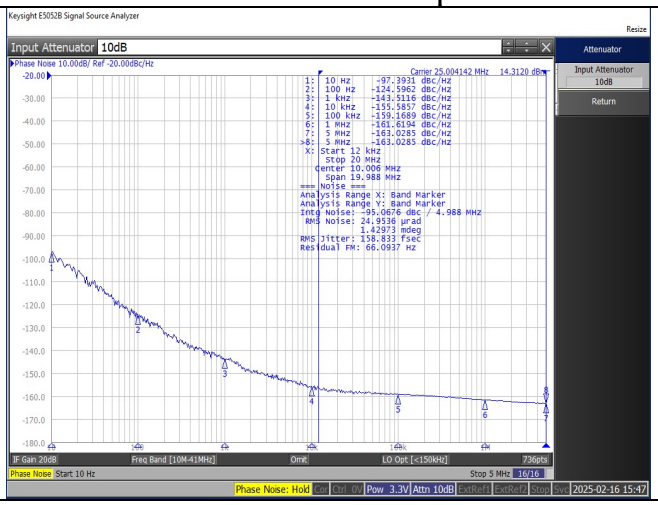
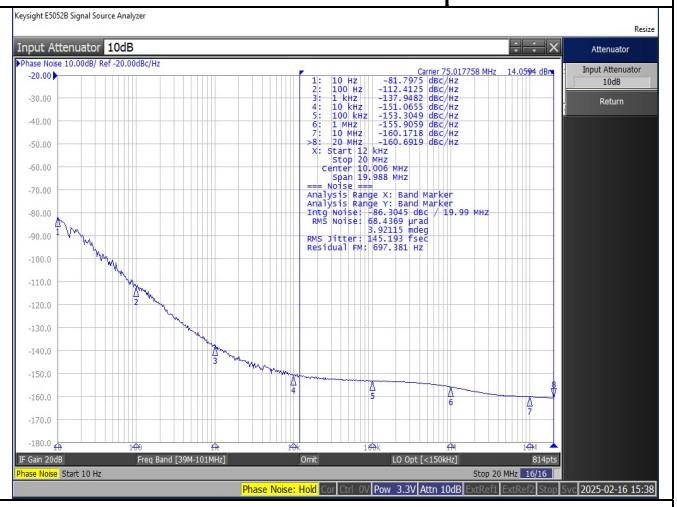
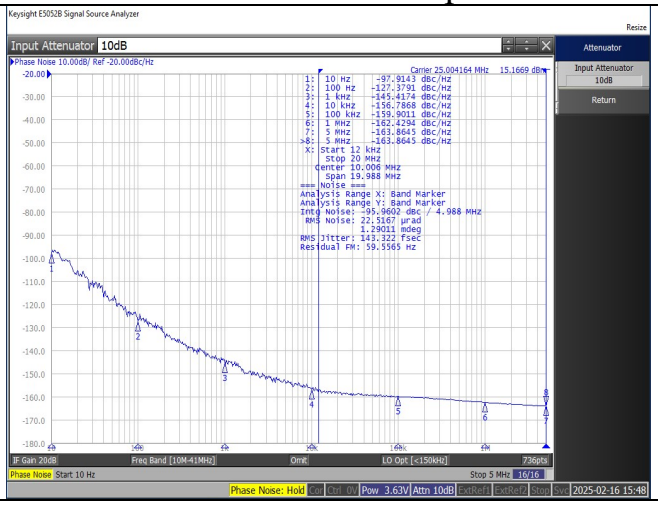
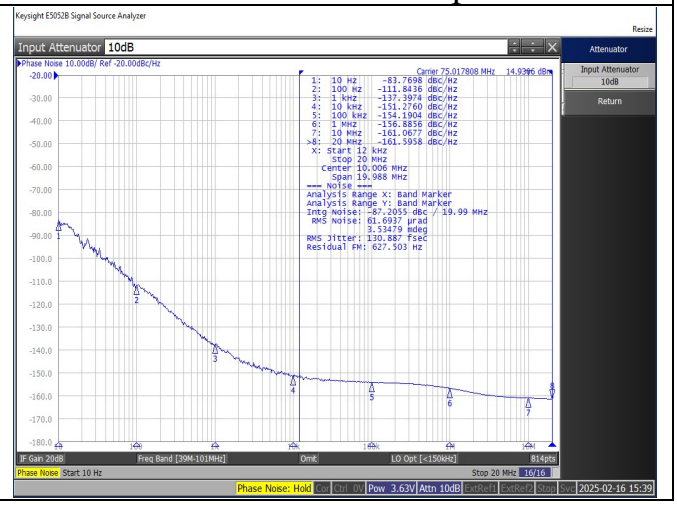


Crystal parameters

Phase Noise

Ta=25 ℃

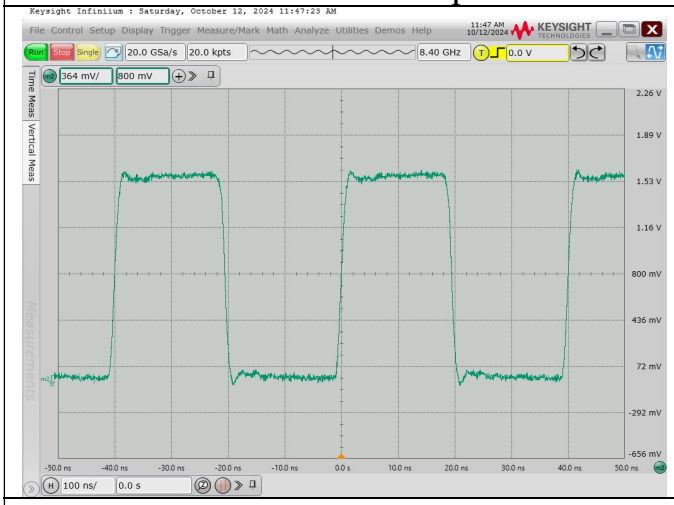
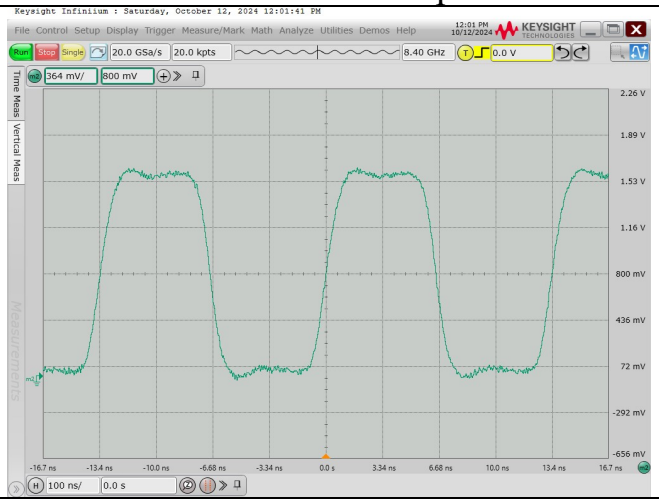
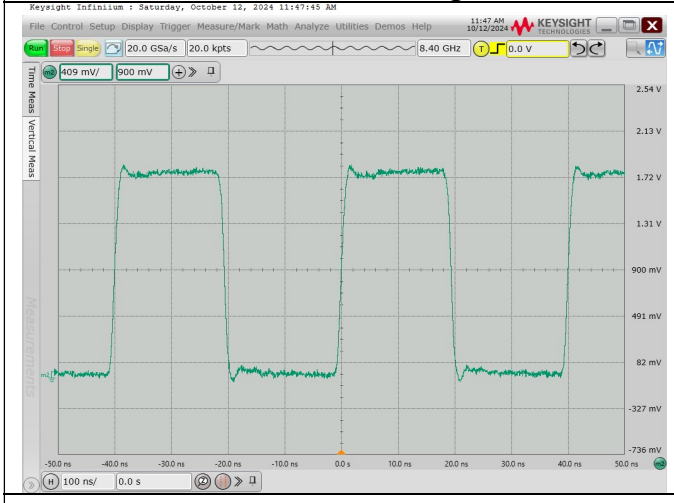
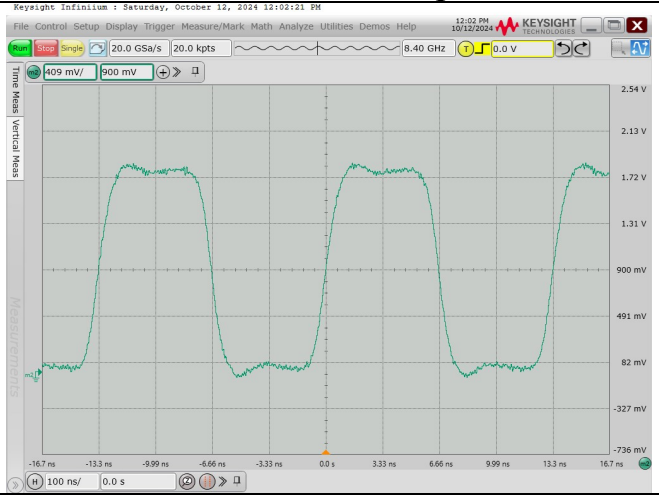
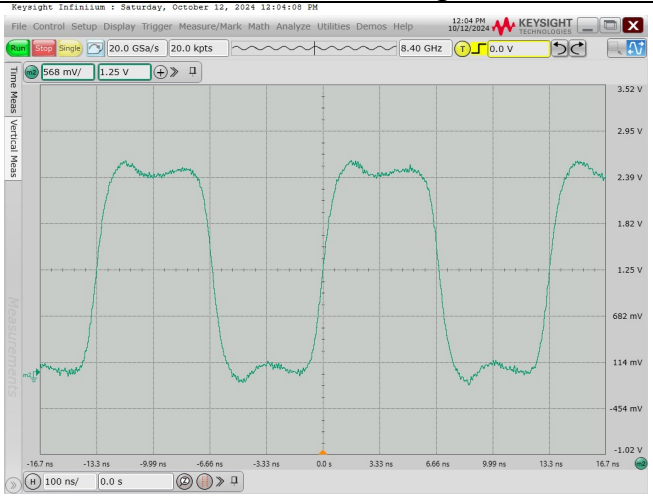
25MHz/1.6V/15pf	75MHz/1.6V/15pf
	
25MHz/1.8V/15pf	75MHz/1.8V/15pf
	
25MHz/2.5V/15pf	75MHz/2.5V /15pf
	

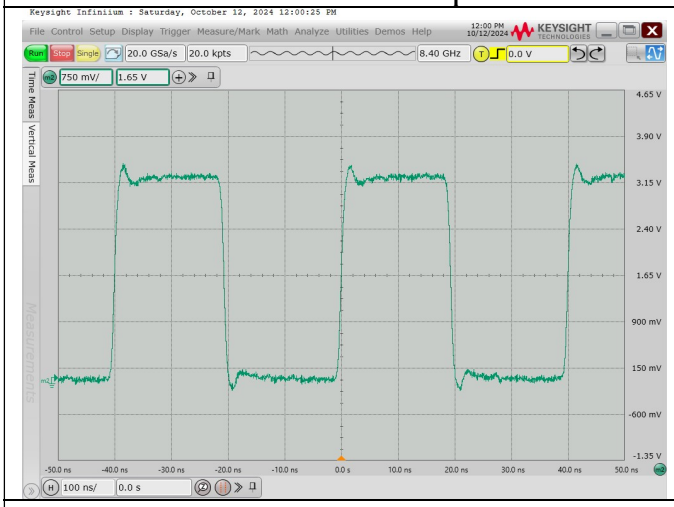
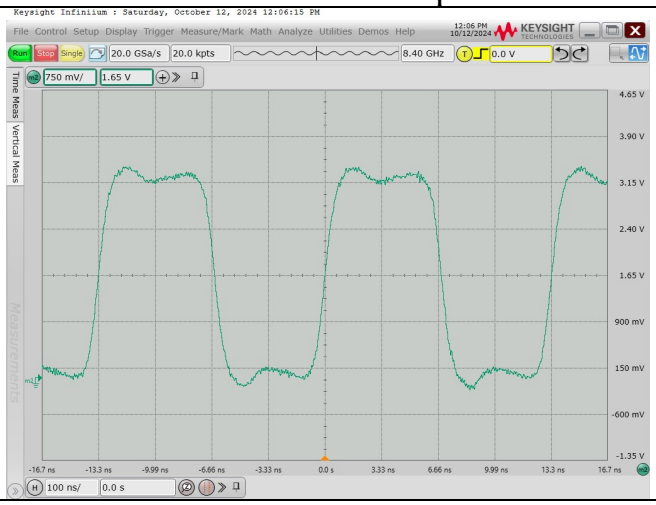
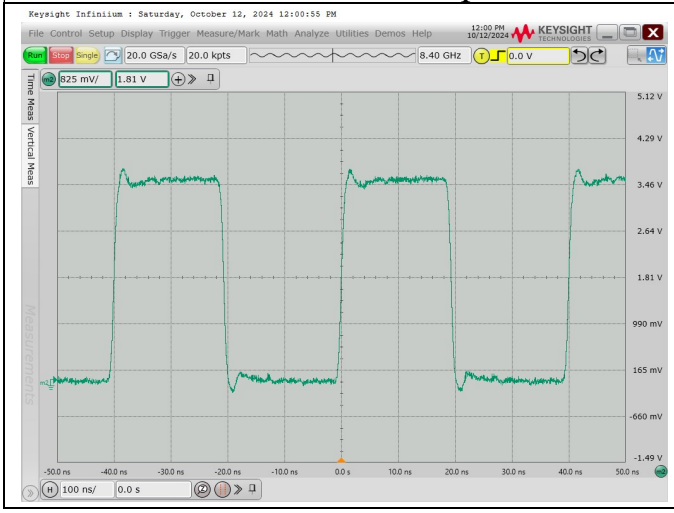
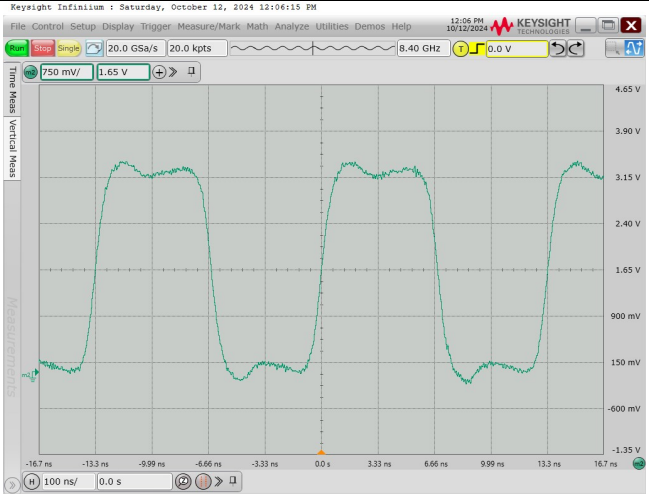
25MHz/3.3V/15pf	75MHz/3.3V/15pf
	
25MHz/3.63V/15pf	**75MHz/3.63V/15pf**
	

Note
Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

Output Waveform

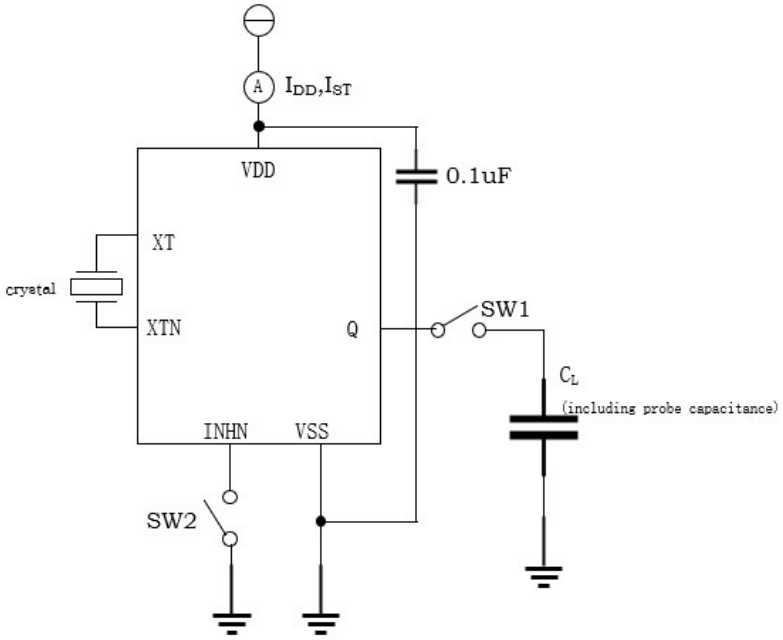
Ta=25 ℃

25MHz/1.6V/15pf	75MHz/1.6V/15pf
	
25MHz/1.8V/15pf	75MHz/1.8V/15pf
	
25MHz/2.5V/15pf	75MHz/2.5V /15pf
	

25MHz/3.3V/15pf	75MHz/3.3V/15pf
	
25MHz/3.63V/15pf	**75MHz/3.63V/15pf**
	

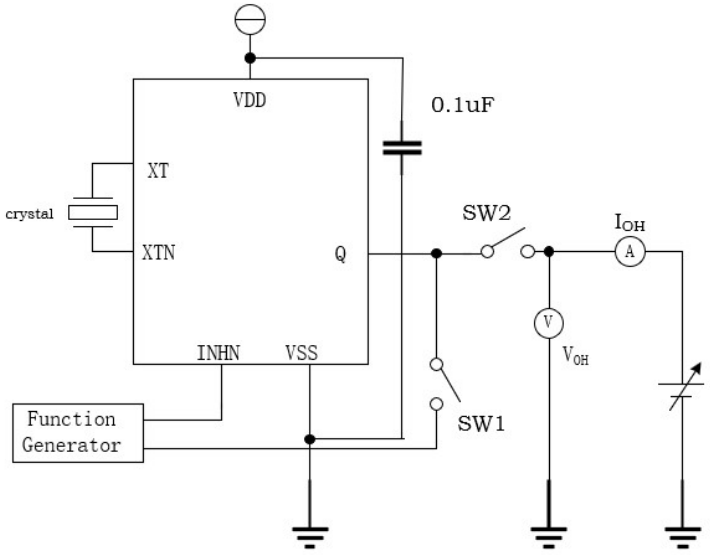
Measurement Circuit

Measurement Circuit 1 : I_{DD}, I_{ST}, DUTY ,tr, tf



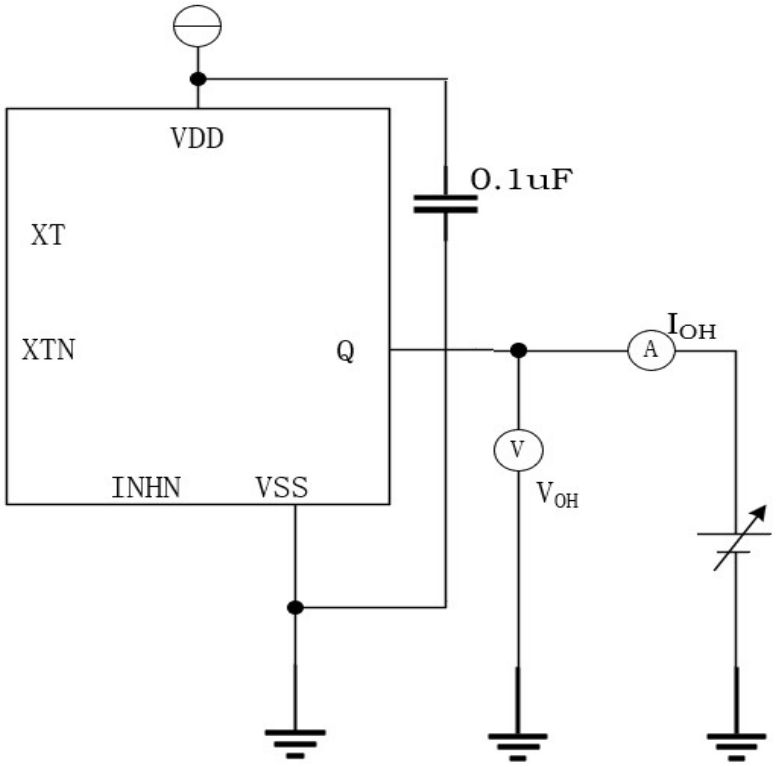
Measurement item	SW1	SW2
IDD	OFF	OFF
IST	ON or OFF	ON
DUTY,tr,tf	ON	OFF

Measurement Circuit 2, V_{OH}

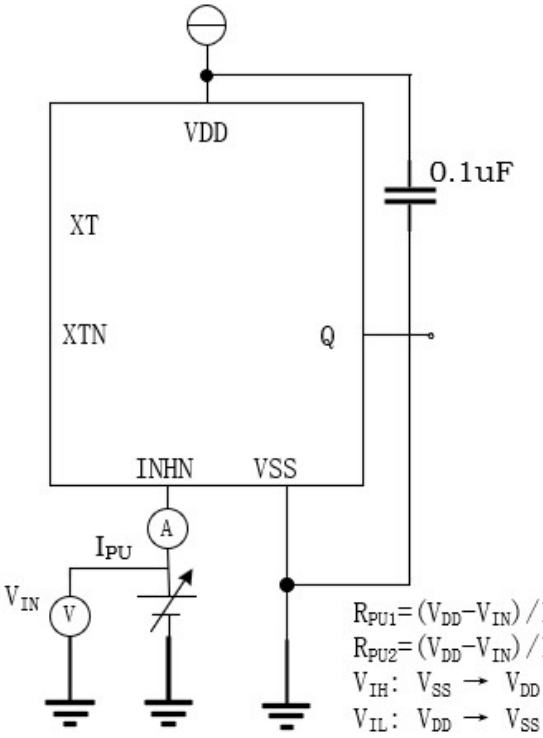


Step1: [SW1=ON, SW2=OFF] SIFMode AD=4H Write Data=07H
Step2: [SW1=OFF, SW2=ON] VOH Measure

Measurement Circuit 3 V_{OL}

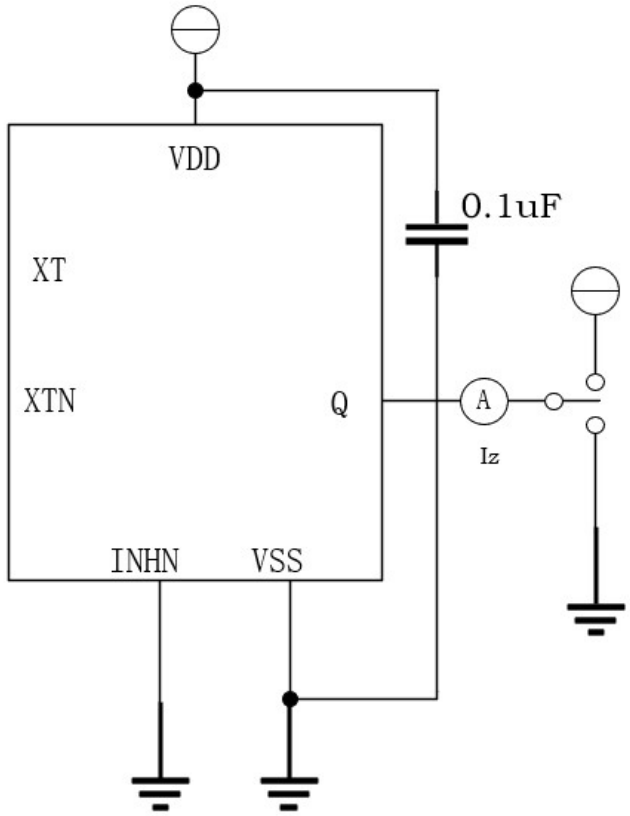


Measurement circuit 4 Rpu1, Rpu2, V_{IH},V_{IL}

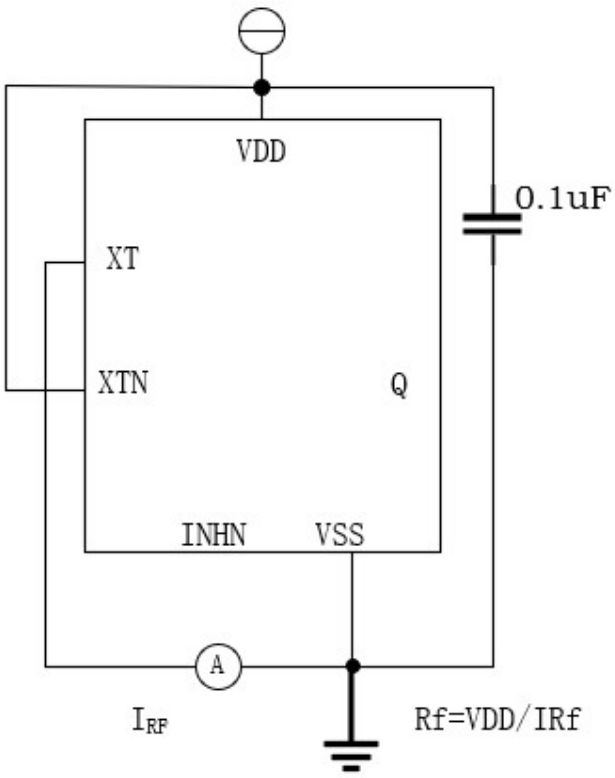


$R_{PU1}=(V_{DD}-V_{IN})/I_{PU}$, $V_{IN}=V_{SS}$
$R_{PU2}=(V_{DD}-V_{IN})/I_{PU}$, $V_{IN}=0.7V_{DD}$
V_{IH}: V_{SS} → V_{DD} , voltage that changes enable output state
V_{IL}: V_{DD} → V_{SS} , voltage that changes disable output state

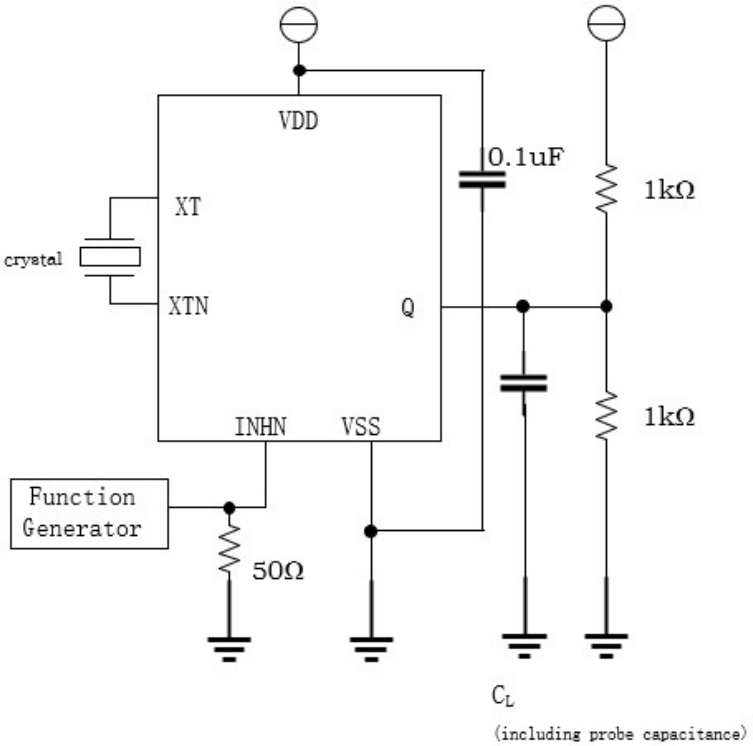
Measurement Circuit 5 I_Z



Measurement Circuit 6 Rr



Measurement Circuit 7 V_{STR},V_{STO},t_{STA},t_{OE},t_{OD}



Revision	Description	DATE
V1.0	Initial release	2025/5/14