Features

- Provides year, month, day, weekday, hours, minutes, and seconds based on a internal 32.768 kHz quartz crystal
- Optional 12/24 hour format.
- Low power consumption: 500nA typical value (VBAT=3.0V, Ta=25℃).
- Operating voltage: 1.8~5.3V.
- Operating temperature: -40℃~+85℃.
- Standard IIC bus interface, maximum speed 400KHz
- 12-byte SRAM
- Alarm function
- Countdown timer
- Programmable square-wave output
- Automatic power-fail detect and switch circuitry
- Write protection function
- Built-in power supply voltage regulation, internal timing voltage can be as low as 1.5V.

Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

Description

RS4C2078 is a real-time clock chip with a standard IIC interface, which can be used by the CPU to read and write data from 32 bytes of registers on the chip (including time registers, alarm registers, control registers, and general SRAM registers)

RS4C2078 built-in single timing/alarm interrupt output, alarm interrupt time can be set up to 100 years.

RS4C2078 built-in crystal oscillator, users can not worry about the component matching error caused by external crystal oscillator, resonant capacitor and other problems of oscillation reliability.

RS4C2078 built-in clock accuracy digital adjustment function, can correct the deviation of the clock in a wide range (-189ppm~+189ppm, resolution of 3.05ppm), and through the external temperature sensor can be set to adapt to the temperature change adjustment value, to achieve high precision timing function in a wide temperature range.

The RS4C2078 has a backup battery input pin VBAT. When the chip detects that the main power VCC drops below the backup battery voltage, the chip automatically switches to the backup battery connected to the VBAT.

Ordering Information

Part Number	Package	Description
RS4C2078SE	SOP8(208mil)	5.3mm x 8.1mm

Note:
E= Green Package

Typical Application Circuit

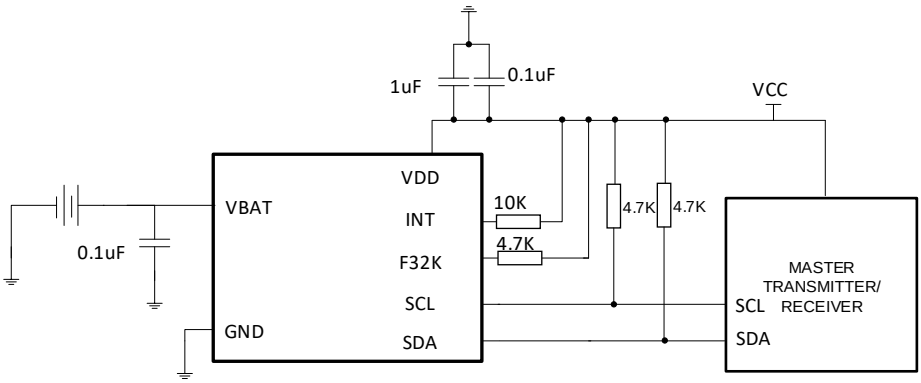


Figure1 Typical application circuit

Pin Configuration

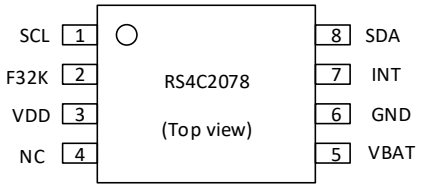


Figure2 Pin configuration

Pin Description

Pin Number	Pin Name	Description
1	SCL	Serial Clock.CMOS input.
2	F32K	32KHZ frequency output pin (open-drain)
3	VDD	Power Supply
4	NC	/
5	VBAT	Secondary Power Supply
6	GND	Ground supply voltage
7	INT	Interrupt/square-wave output (open-drain)
8	SDA	Serial Data (open-drain)

Note

[1]: Recommends tying VDD of the device and VDD of all the external pull-up resistors to the same Power Supply.

Registers Table

Addr. (hex)	Function (time range BCD format)	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Time and date registers									
00	Seconds	0	SECONDS (0 to 59)						
01	Minutes	0	MINUTES (0 to 59)						
02	Hours	12/24	0	AMPM	HOURS (1 to 12) in 12-hour mode				
				HOURS (0 to 23) in 24-hour mode					
03	Weekdays	0	0	0	0	0	WEEKDAYS (0 to 6)		
04	Days	0	0	Days(1-31)					
05	Months	0	0	0	MONTHS (1 to 12)				
06	Years	YEARS (0 to 99)							
Alarm register									
07	Second_alarm	0	SECOND _ALARM (0 to 59)						
08	Minute_alarm	0	MINUTE _ALARM (0 to 59						
09	Hour_alarm	0	0	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
				HOUR_ALARM (0 to 23) in 24-hour mode					
0A	Weekday_alarm	0	AW6	AW5	AW4	AW3	AW2	AW1	AW0
0B	Day_alarm	0	0	Day_alarm (1-31)					
0C	Month_alarm	0	0	0	Month_alarm (1 to 12)				
0D	Year_alarm	YEARS (0 to 99)							
0E	Alarm enable	0	EAY	EAMO	EAD	EAW	EAH	EAMN	EAS
Control registers									
0F	CTR1	WRTC3	0	INTAF	INTDF	0	WRTC2	0	RTCF
10	CTR2	WRTC1	IM	INTS1	INTS0	FOBAT	INTDE	INTAE	INTFE
11	CTR3	ARST	0	TDS1	TDS0	FS3	FS2	FS1	FS0
12	Offset	0	F6	F5	F4	F3	F2	F1	F0
13	Timer	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
14-1F	RAM	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Time and date registers

Seconds register(0x00)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 seconds			Seconds			

Minutes register(0x01)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			Minutes			

Hours register(0x02)

D7	D6	D5	D4	D3	D2	D1	D0
D7=1;24h mode D7=0;12h mode	0	D5=0;AM D5=1;PM	HOUR_ALARM (1 to 12) in 12-hour mode				
		HOUR_ALARM (0 to 23) in 24-hour mode					

Note:
In the 24-hour mode, the highest bit of the hour is set to 1. When you read the time, discard the highest bit or set it to 0. Otherwise, the hour time is incorrect.

Weekdays register(0x03)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Weekdays		

Days register(0x04)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		Days			

Months register(0x05)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	10Months	Months			

Years register(0x06)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Note:
During power-on reset, the real-time clock data register is not cleared or set inside the chip.

Alarm register

Second_alarm register(0x07)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 seconds			Seconds			

Minute_alarm register(0x08)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			Minutes			

Hour_alarm register(0x09)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	D5=0;AM D5=1;PM	HOUR_ALARM (1 to 12) in 12-hour mode				
		HOUR_ALARM (0 to 23) in 24-hour mode					

Weekday_alarm register(0x0A)

D7	D6	D5	D4	D3	D2	D1	D0
0	AW6 Saturday	AW5 Friday	AW4 Thursday	AW3 Wednesday	AW2 Tuesday	AW1 Monday	AW0 Sunday

Note:
For example,AW6 and AW1=1, other bits are 0, corresponding to Saturday, Monday will alarm

Day_alarm register(0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		Days			

Month_alarm register(0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	10Months	Months			

Year_alarm register(0x0D)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Alarm enable register(0x0E)

D7	D6	D5	D4	D3	D2	D1	D0
0	If EAY=1 Year enable	If EAMO=1 Month enable	If EAD=1 Day enable	If EAW=1 Week enable	If EAH=1 Hour enable	If EAMN=1 Min Enable	If EAS=1 Sec enable

Control register

CTR1 register(0x0F)

Bit	Symbol	Description
7	WRTC3	**Write protection**[*1]
6	0	/
5	INTAF	**alarm flag** 0 = read: alarm flag inactive 0 = write: alarm flag is cleared 1= read: alarm flag active 1= write: alarm flag remains unchanged
4	INTDF	**timer flag** 0=no timer interrupt generated 1=flag set when timer interrupt generated
3	0	/
2	WRTC2	**Write protection**[*1]
1	0	/
0	RTCF	Power on after all power supplies fail. This bit is 1.After power-on, as long as the register is successfully written, this bit will be cleared to 0

CTR2 register(0x10)

Bit	Symbol	Description
7	WRTC1	**Write protection**[*1]
6	IM	**Alarm interrupt mode** 0:Single alarm,INT pin output low level until alarm flag is cleared to 0 1:Periodic alarm,INT pin output a periodic pulse of 250ms width until the interrupt enable bit is cleared to 0
5	INTS1	**INT pin interrupt output selection** INTS1=0,INTS0=0;Output high resistance INTS1=0,INTS0=1;Alarm interrupt output INTS1=1,INTS0=0;Frequency output INTS1=1,INTS0=1;Timer interrupt output
4	INTS0	
3	FOBAT	**VBAT power supply interrupts output selection** 0=alarm and timer disable 1=alarm and timer enable
2	INTDE	**Timer enable** 0=timer disable 1=timer enable
1	INTAE	**Alarm enable** 0=alarm disable 1=alarm enable
0	INTFE	**Frequency enable** 0=Frequency disable 1=Frequency enable

Note：

When WRTC1=WRTC2=WRTC3=1, the register allows writing values.It need to set WRTC1=1 before WRTC2=WRTC3=1
When WRTC1=WRTC2=WRTC3=0, the register cannot write values.It need to set WRTC2=WRTC3=0 before WRTC1=0.
Write disable does not affect read operations

CTR3 register(0x11)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>ARST</td><td>Reset enable
1=read CTR1 register,INTAF and INTDF clear to 0</td></tr>
<tr><td>6</td><td>0</td><td>/</td></tr>
<tr><td>5</td><td>TDS1</td><td rowspan="2">Timer frequency source selection
<table>
<tr><th>TDS1</th><th>TDS0</th><th>Timer source(Hz)</th></tr>
<tr><td>0</td><td>0</td><td>4096</td></tr>
<tr><td>0</td><td>1</td><td>64</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1/60</td></tr>
</table></td></tr>
<tr><td>4</td><td>TDS0</td></tr>
<tr><td>3</td><td>FS3</td><td rowspan="4">Frequency selection
<table>
<tr><th>FS3</th><th>FS2</th><th>FS1</th><th>FS0</th><th>频率（Hz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>32768</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>4096</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1024</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>64</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>32</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1/4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1/8</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1/16</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1s</td></tr>
</table></td></tr>
<tr><td>2</td><td>FS2</td></tr>
<tr><td>1</td><td>FS1</td></tr>
<tr><td>0</td><td>FS0</td></tr>
</table>

Offset register(0x12)

D7	D6	D5	D4	D3	D2	D1	D0
0	F6	F5	F4	F3	F2	F1	F0

Using the digital time precision adjustment circuit, the number of 32768Hz pulses contained in the current 1 second can be changed every 20 seconds to adjust the time accuracy.
When F6 = 0, the number of pulses in the register producing one second is increased to 32768+((F5,F4,F3,F2,F1,F0)-1) x 2;
When F6 is 0, the number of pulses in the register producing one second is reduced to32768-((/F5,/F4,/F3,/F2,/F1,/F0)+1) x 2;(/F5 is the complement of F5)
When (F6,F5,F4,F3,F2,F1,F0)=(*,0,0,0,0,0,*),Generates 1 second register count pulse unchanged.
Because the minimum value of increasing or decreasing the count pulse every 20s is 2, the minimum precision of adjusting the clock adjustment register is 2/(32768 x 20)=3.015ppm.

Adjustment value calculation method:
(1) When the crystal frequency is greater than 32768Hz,
Adjusted value = (crystal frequency-32768）*10+1；
(2) When the crystal frequency is less than 32768Hz,
Adjusted value = (crystal frequency-32768）*10；
The adjusted value is a value from F6 to F0, expressed in binary complement form.

For example:
(1) crystal frequency =32770Hz
Adjusted value = (32770-32768)*10+1=21;
F6 ~ F0 =(0,0,1,0,1,0,1)
(2) crystal frequency =32762Hz
Adjusted value = (32762-32768)*10=-60
F6 ~ F0=(1,0,0,0,1,0,0)

Time adjustment does not change the INT pin output frequency.
Maximum adjustment range:
1) crystal frequency greater than 32768Hz, adjustment range F6 ~F0 from (0,0,0,0,0,0,0) to (0,1,1,1,1,1,1),Actual adjustable range from -3.05ppm to -189.2ppm.
2) crystal frequency less than 32768Hz, adjustment range F6 ~F0 from (1,1,1,1,1,1,1) to (1,0,0,0,0,1,0),Actual adjustable range from 3.05ppm to 189.2ppm.

Timer register(0x13)

D7	D6	D5	D4	D3	D2	D1	D0
0-255							

RAM register(0x14 -1F)

D7	D6	D5	D4	D3	D2	D1	D0
12Bytes							

Backup battery switch function

The RS4C2078 has a backup battery switching function, and the VBAT voltage is less than VDD-0.3V. When the chip detects that the main power supply VDD falls below VBAT voltage, it automatically switches to VBAT power supply.
The following conditions must be met to switch from VDD to VBAT:
VDD < VBAT - V_{BATHYS},V_{BATHYS} =100mV.

The following conditions must be met to switch from VBAT to VDD:
VDD > VBAT + V_{BATHYS},V_{BATHYS} =100mV.

When switching to VBAT mode, the IIC communication function continues to be allowed, and the clock read and write function can be realized.
When the VBAT voltage is reduced to 1.5V, the user SRAM data can still be saved

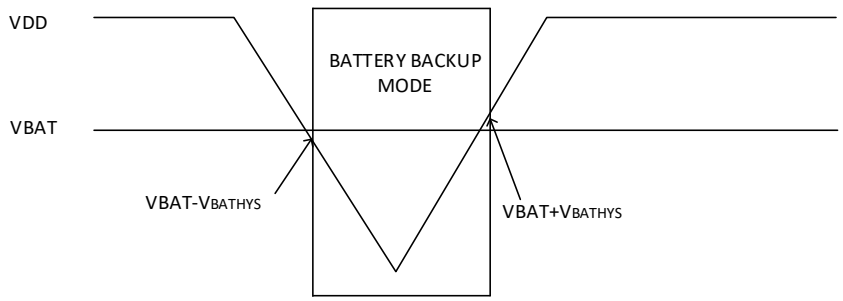


Figure3 Backup battery switch

I²C Bus Interface

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be pulled up via a pull-up resistors.
The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.

•During data transfer, the data line must remain stable whenever the clock line is high.
•Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain high.

Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

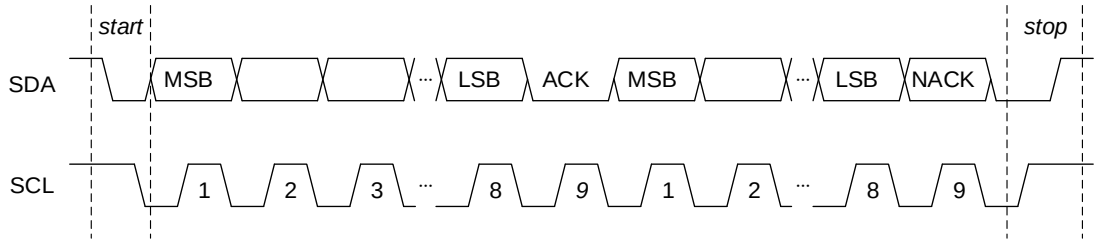


Figure4: Serial bus data transfer sequence

Read mode

In this mode, the master reads the RS4C2078 slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the
master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.
The RS4C2078 slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.
This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

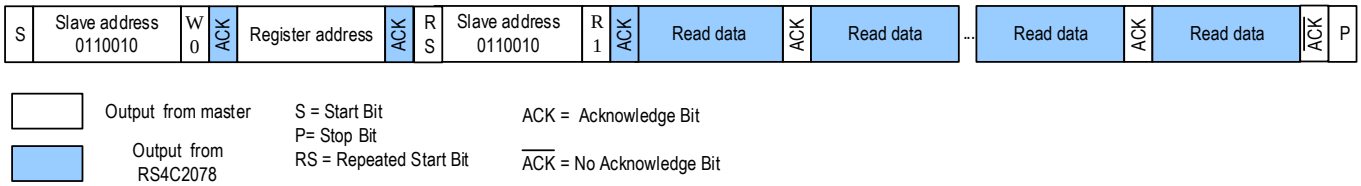


Figure5 Read Mode Sequence

Write mode

In this mode the master transmitter transmits to the RS4C2078 slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The RS4C2078 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

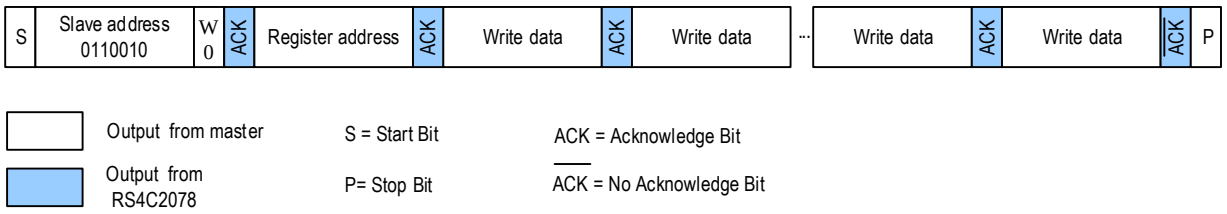


Figure6 Write Mode Sequence

Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	output voltage		-0.5	+7	V
T_{stg}	storage temperature		-60	+150	°C
T_{amb}	ambient temperature	operating device	-40	+85	°C

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VDD	Main power supply		1.8		5.3	V
VBAT	Battery Supply Voltage		1.5		5.2	
IDD1	Supply Current	VDD=5V		0.6	1	uA
		VDD=3V		0.5	1	uA
IDD2	Supply Current with IIC Active	VDD=5V		20	120	uA
IBAT	Battery Supply Current	VBAT=3V		0.5		uA
ILI	Input leakage current on SCL			100		nA
ILO	I/O leakage current on SDA			100		nA
V_{BATHYS}	VBAT Hysteresis			100		mV
INT VOL	Output low Voltage	VDD=5V,IOH=2mA			0.4V	V

I2C AC Characteristics

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals	Fast mode			300	ns
		Standard mode			1000	
t_F	Fall Time of Both SDA and SCL Signals	Fast mode			300	ns
		Standard mode			300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			

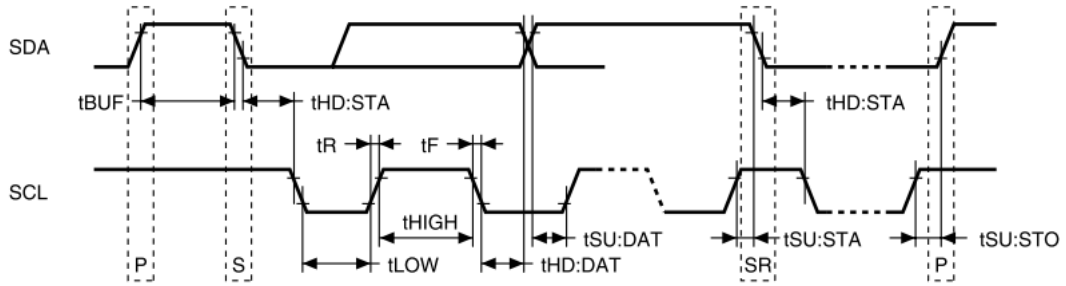
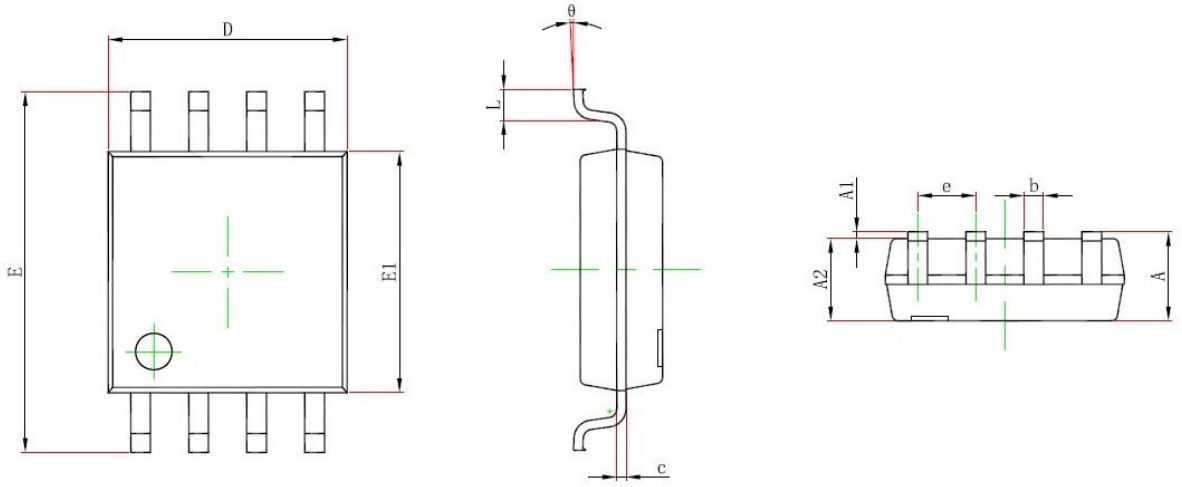


Figure7 I2C-bus timing diagram

Package Information

SOP8（208mil)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	2.150	——	0.085
A1	0.050	0.250	0.002	0.010
A2	1.700	1.900	0.067	0.075
b	0.350	0.500	0.014	0.020
c	0.100	0.250	0.004	0.010
D	5.130	5.330	0.202	0.210
E	7.700	8.100	0.303	0.319
E1	5.180	5.380	0.204	0.212
e	1.270(BSC)		0.050(BSC)	
L	0.500	0.850	0.020	0.033
θ	0°	8°	0°	8°



Note:
1. All dimensions are in mm. Angels in degrees.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MS-012

RSM SOP08 208mil(S08)
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary Release	2024/4/16
1.0	Initial Release	2024/11/26