Features

- No Direction-Control
- Max Data Rates

  24Mbps (Push-Pull)

  2Mbps (Open-Drain)
- 1.2V to 3.63V on A ports and 1.2V to 3.63V on

  B Ports
- VCCA can be Less than, Greater than or Equal to VCCB
- VCC Isolation: If Either VCC is at GND, Both Ports are in the High-Impedance State
- No Power-Supply Sequencing Required: VCCA or VCCB can be Ramped First
- Grade 1 temperature range (- 40℃ ~ +125 ℃)
- Wafer form

Applications

- I2C/SMBus
- SPI Interface
- UART
- Handheld Devices Interface

Description

The RS7LS104 is a 4-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, VCCA and VCCB respectively.

A port supporting operating voltages from 1.2V to 3.63V while it tracks the VCCA supply, and the B ports supporting operating voltages from 1.2V to 3.63V while it tracks the VCCB supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V,1.8V, 2.5V, 3.3V voltage and 3.63V nodes.

When the output-enable (EN) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, EN should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Information

Part Number	Package type
RS7LS104-WF	Wafer form

Block Diagram

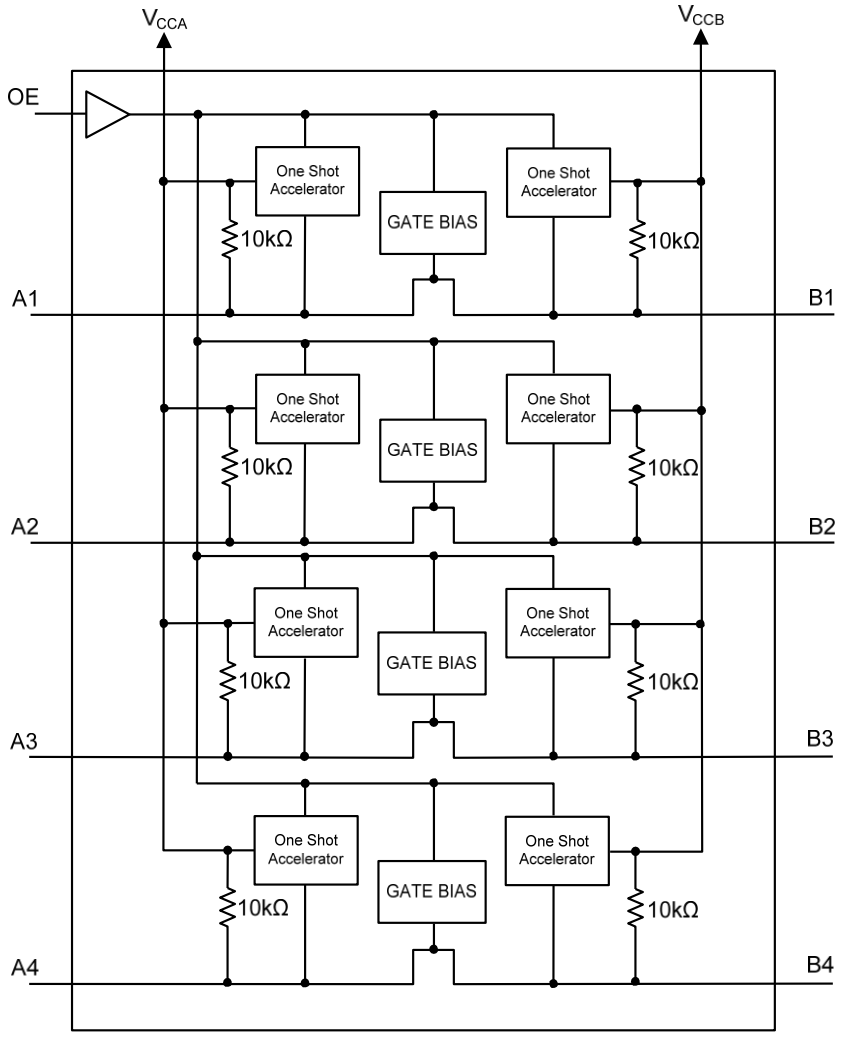
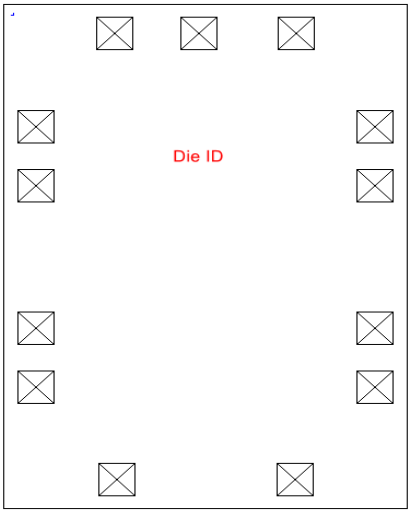


Figure 1 Block Diagram

PAD Configuration



Pad Name	X Coordinate	Y Coordinate	Spot Length	Spot Width
VCCA	-202.195	552	80	80
A1	-377	321.935	80	80
A2	-377	175.85	80	80
A3	-377	-177.310	80	80
A4	-377	-323.400	80	80
GND	-198.08	-552	80	80
B4	377	-323.4	80	80
B3	377	-177.31	80	80
B2	377	175.85	80	80
B1	377	321.935	80	80
VCCB	202.425	552	80	80
EN	200.34	-552	80	80
EN	-14.775	552	80	80

Note: Substrate is connected to GND or floating.

Die Size: 900 μm* 1250 μm (Not include scribe line), scribe line: 80μm
Pad Size: 80μm*80μm **Substrate Level:** GND or Floating

PAD Description

Pin Name	Description
VCCA	A-port supply voltage.1.2V ≤ VCCA ≤3.63 V
A1	Input/output A. Referenced to VCCA.
A2	Input/output A. Referenced to VCCA
A3	Input/output A. Referenced to VCCA
A4	Input/output A. Referenced to VCCA
GND	Ground.
OE	Output enables (active High). Pull OE low to place all outputs in 3-state mode.
B4	Input/output B. Referenced to VCCB
B3	Input/output B. Referenced to VCCB
B2	Input/output B. Referenced to VCCB
B1	Input/output B. Referenced to VCCB
VCCB	B-port supply voltage.1.2V ≤ VCCB ≤3.63V
NC	Not Connect

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
Tstore	Storage Temperature	−65	-	150	°C
VCCA	DC Supply Voltage port B	-0.3	-	5.5	V
VCCB	DC Supply Voltage port A	-0.3	-	5.5	V
VIOB	Vi(A) referenced DC Input / Output Voltage	-0.3	-	5.5	V
VIOB	Vi(B) referenced DC Input / Output Voltage	-0.3	-	5.5	V
VEN	Enable Control Pin DC Input Voltage	-0.3	-	5.5	V
Ishort	Short circuit duration (I/O to GND)			50	mA

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VCCA	VCCA Positive DC Supply Voltage	1.2	-	3.63	V
VCCB	VCCB Positive DC Supply Voltage	1.2	-	3.63	V
VEN	Enable Control Pin Voltage	GND	-	3.63	V
VIO	I/O Pin Voltage	GND	-	3.63	V
Δt /ΔV	Input transition rise or fall time	-	-	10	ns/V
TA	Operating Temperature Range	−40	-	125	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤125° C, 1.2V≤V_{CCA}≤3.63V , 1.2V≤V_{CCB}≤3.63V

Symbol	Parameter	Test Conditions*1		MIN	TYP	MAX	Unit
VIHA	A port Input HIGH Voltage	2.3V≤VCCA ≤3.63V		VCCA – 0.4			V
		1.2V≤VCCA < 2.3V		VCCA – 0.2			V
VILA	A port Input LOW Voltage	1.2V≤VCCA ≤3.63V		-	-	0.15	V
VIHB	B port Input HIGH Voltage	2.3V≤VCCB ≤3.63V		VCCB – 0.4	-	-	V
		1.2V≤VCCA < 2.3V		VCCB – 0.2			
VILB	B port Input LOW Voltage	1.2V≤VCCB ≤3.63V		-	-	0.15	V
VIH(EN)	Control Pin Input HIGH Voltage	1.2V≤VCCA ≤3.63V		0.65*VCCA	-	-	V
	Control Pin Input LOW Voltage	1.65V≤VCCA ≤3.63V		-	-	0.35* VCCA	
VIL(EN)		1.2V≤VCCA < 1.65V				0.15	V
VOHA	A port Output HIGH Voltage	A port source current= -20 μA		0.8* VCCA	-	-	V
VOLA	A port Output LOW Voltage	A port sink current =1 mA		-	-	0.4	V
VOHB	B port Output HIGH Voltage	B port source current = -20 μA		0.8*VCCB	-	-	V
VOLB	B port Output LOW Voltage	B port sink current =1 mA		-	-	0.4	V
ICCA	VCCA Supply Current	OE=High	VCCA=1.2V to 3.63V, VCCB=1.2V to 3.63V	-	0.2	2.4	μA
			VCCA= 3.63V, VCCB= 0V	-	-	2	μA
			VCCA= 0V, VCCB=3.63V	-	-	1	μA
ICCB	VCCB Supply Current	OE=High	VCCA=1.2V to 3.63V, VCCB=1.2V to 3.63V	-	0.5	10	μA
			VCCA= 3.63V, VCCB= 0V	-		1	μA
			VCCA= 0V, VCCB=3.63V	-		8	μA
ICCA +ICCB	Combined supply current		VCCA=1.2V to 3.63V, VCCB=1.2V to 3.63V			15	μA
		OE=High					
ICCZA	Static supply current VCCA	OE=Low	VCCA=1.2V to 3.63V, VCCB=1.2V to 3.63V			8	μA
ICCZB	Static supply current VCCB					8	μA
IOZ	I/O Tri−state Output Mode Leakage Current	A or B	VIA=0~VCCA			±8	μA
		Port	VIB=0~VCCB				
		A port	VCCA=0V, VCCB=1.2V to 3.63V			±8	μA
IOFF	Partial power down current	B port	VCCA=1.2V to 3.63V VCCB=0V			±8	μA
II-EN	Control pin leakage Current	VI = VCCI or GND		-	-	±2	μA
RPU	Pull−Up Resistors I/O A and B	-		-	10	-	kΩ
Ci	EN	VCCA= 3.3V, VCCB= 3.3V		-	-	1	pF
CIO	A port	VCCA= 3.3V, VCCB= 3.3V		-	-	5	pF
	B port	VCCA= 3.3V, VCCB= 3.3V		-	-	5	pF

Note:

1. All units are production tested at TA = +25°C. Limits over the operating temperature range are guaranteed by design. Typical values are for VCCB = +3.3 V, VCCA = +1.8 V and TA = +25°C.

AC Electrical characteristics

C_{LOAD} = 15pF, driver output impedance ≤ 50Ω, R_{LOAD} = 1 MΩ, TA = -40°C to 125° C,

V_{CCA}= 1.2V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB=1.8V		VCCB=2.5V		VCCB=3.3V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL_AB}	Propagation Delay A → B	Push-pull		12		10		10	ns
		Open-drain		30		30		30	ns
t_{PLH_AB}	Propagation Delay A → B	Push-pull		20		15		15	ns
		Open-drain		30		30		30	ns
t_{PHL_BA}	Propagation Delay B → A	Push-pull		12		10		10	ns
		Open-drain		30		30		30	ns
t_{PLH_BA}	Propagation Delay B → A	Push-pull		20		15		15	ns
		Open-drain		50		50		50	ns
t_{EN}	Enable Time	EN to A or B		380		200		200	ns
t_{DIS}	Disable Time	EN to A or B		200		200		200	ns
t_{RA}	A port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		120		120	ns
t_{RB}	B port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		160		160	ns
t_{FA}	A port Fall Time	Push-pull		20		20		25	ns
		Open-drain		30		30		30	ns
t_{FB}	B port Fall Time	Push-pull		20		20		25	ns
		Open-drain		30		30		30	ns
t_{SKEW}	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull	20		20		20		Mbps
		Open-drain	2		2		2		Mbps

V_{CCA}= 1.8V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB=1.2V		VCCB=2.5V		VCCB = 3.3V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL_AB}	Propagation Delay A → B	Push-pull		12		10		9	ns
		Open-drain		30		30		30	ns
t_{PLH_AB}	Propagation Delay A → B	Push-pull		20		12		11	ns
		Open-drain		30		30		30	ns
t_{PHL_BA}	Propagation Delay B → A	Push-pull		12		9		9	ns
		Open-drain		30		30		30	ns
t_{PLH_BA}	Propagation Delay B →A	Push-pull		20		14		12	ns
		Open-drain		50		50		50	ns
t_{EN}	Enable Time	EN to A or B		200		200		200	ns
t_{DIS}	Disable Time	EN to A or B		200		200		200	ns
t_{RA}	A port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		120		120	ns
t_{RB}	B port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		160		160	ns
t_{FA}	A port Fall Time	Push-pull		20		20		25	ns
		Open-drain		30		30		30	ns
t_{FB}	B port Fall Time	Push-pull		20		25		30	ns
		Open-drain		30		30		30	ns
t_{SKEW}	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull	20		20		24		Mbps
		Open-drain	2		2		2		Mbps

V_{CCA}= 2.5V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 1.2V		VCCB= 1.8V		VCCB = 3.3V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL_AB}	Propagation Delay A → B	Push-pull		10		9		9	ns
		Open-drain		30		30		30	ns
t_{PLH_AB}	Propagation Delay A → B	Push-pull		15		12		10	ns
		Open-drain		30		30		30	ns
t_{PHL_BA}	Propagation Delay B → A	Push-pull		10		10		9	ns
		Open-drain		30		30		30	ns
t_{PLH_BA}	Propagation Delay B →A	Push-pull		15		12		12	ns
		Open-drain		50		50		50	ns
t_{EN}	Enable Time	EN to A or B		200		200		200	ns
t_{DIS}	Disable Time	EN to A or B		200		200		200	ns
t_{RA}	A port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		120		120	ns
t_{RB}	B port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		160		160	ns
t_{FA}	A port Fall Time	Push-pull		20		25		30	ns
		Open-drain		30		30		30	ns
t_{FB}	B port Fall Time	Push-pull		20		20		25	ns
		Open-drain		30		30		30	ns
t_{SKEW}	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull	20		20		24		Mbps
		Open-drain	2		2		2		Mbps

V_{CCA}= 3.3V

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	VCCB= 1.2V		VCCB= 1.8V		VCCB = 2.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL_AB}	Propagation Delay A → B	Push-pull		10		9		9	ns
		Open-drain		30		30		30	ns
t_{PLH_AB}	Propagation Delay A → B	Push-pull		15		12		12	ns
		Open-drain		30		30		30	ns
t_{PHL_BA}	Propagation Delay B → A	Push-pull		10		9		9	ns
		Open-drain		30		30		30	ns
t_{PLH_BA}	Propagation Delay B →A	Push-pull		15		11		10	ns
		Open-drain		50		50		50	ns
t_{EN}	Enable Time	EN to A or B		200		200		200	ns
t_{DIS}	Disable Time	EN to A or B		200		200		200	ns
t_{RA}	A port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		120		120	ns
t_{RB}	B port Rise Time	Push-pull		30		30		30	ns
		Open-drain		160		160		160	ns
t_{FA}	A port Fall Time	Push-pull		25		25		25	ns
		Open-drain		30		30		30	ns
t_{FB}	B port Fall Time	Push-pull		25		25		25	ns
		Open-drain		30		30		30	ns
t_{SKEW}	Channel to Channel Skew			1		1		1	ns
MDR	Maximum Data Rate	Push-pull	20		24		24		Mbps
		Open-drain	2		2		2		Mbps

Parameter Measurement Information

Load Circuits

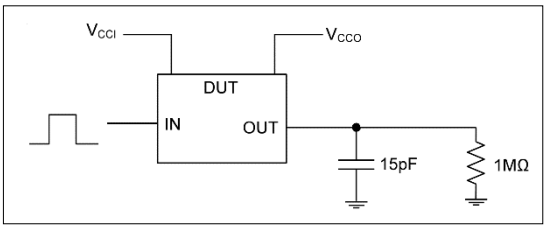


Figure 3 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

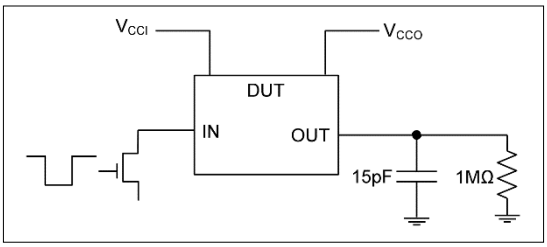
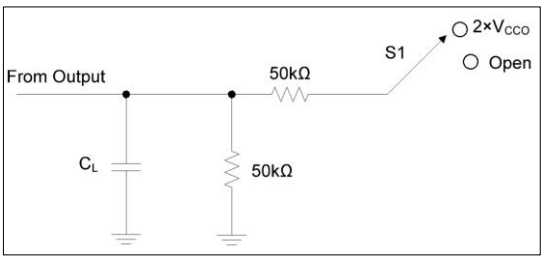


Figure 4 Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
tPZL / tPLZ	2 × VCCO
tPHZ / Tpzh	Open

Figure 5 Load Circuit for Enable-Time and Disable-Time Measurement

Notes:

1. CL includes probe and jig capacitance.
2. ten is the same as tPZL and tPZH. tdis is the same as tPLZ and tPHZ.
3. VCCI is the supply voltage associated with the input.
4. VCCO is the supply voltage associated with the input.

Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤10 MHz
- Z_O = 50 Ω
- dv/dt ≥1 V/ns

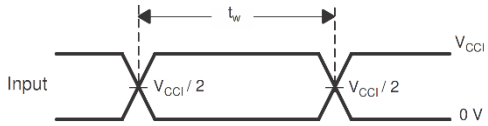


Figure 6 Pulse Duration

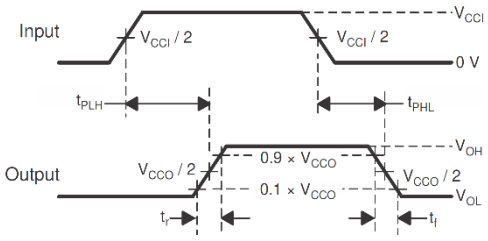
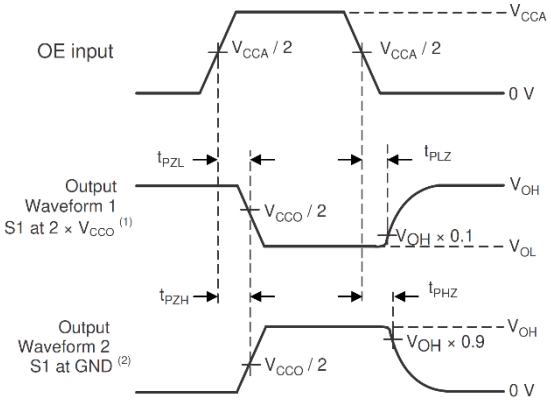


Figure 7 Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.

B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 8 Enable and Disable Times

Functional Description

Architecture

The RS7LS104 architecture does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

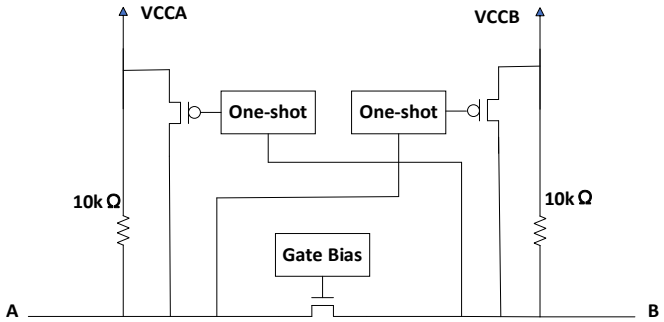


Figure 9 Level Shifter Architecture

Each A-port I/O has an internal 10kΩ pull up resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pull-up resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors for a short duration, which speeds up the low-to-high transition.

Input Driver Requirements

The rise (tR) and fall (tF) timing parameters of the open drain outputs depend on the magnitude of the pull−up resistors. In -addition, the propagation times (tPD), skew (tSKEW) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 kΩ .

Enable Input (OE)

The RS7LS104 has an Enable pin (OE) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O VCCB and I/O VCCA pins to a high impedance state. Normal translation operation occurs when the OE pin is equal to a logic high signal. The OE pin is referenced to the VCCA supply and has overvoltage tolerant protection.

Pull-up or Pull-down Resistors on I/O Lines

Each A-port I/O has an internal 10kΩ pull-up resistor to VCCA, and each B-port I/O has an internal 10 kΩ pull-up resistor to VCCB. If a smaller value of pull-up resistor is required, an external resistor must be added from the I/O to VCCA or VCCB (in parallel with the internal 10 kΩ resistors).

Device Functional Modes

The RS7LS104 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

Application Information

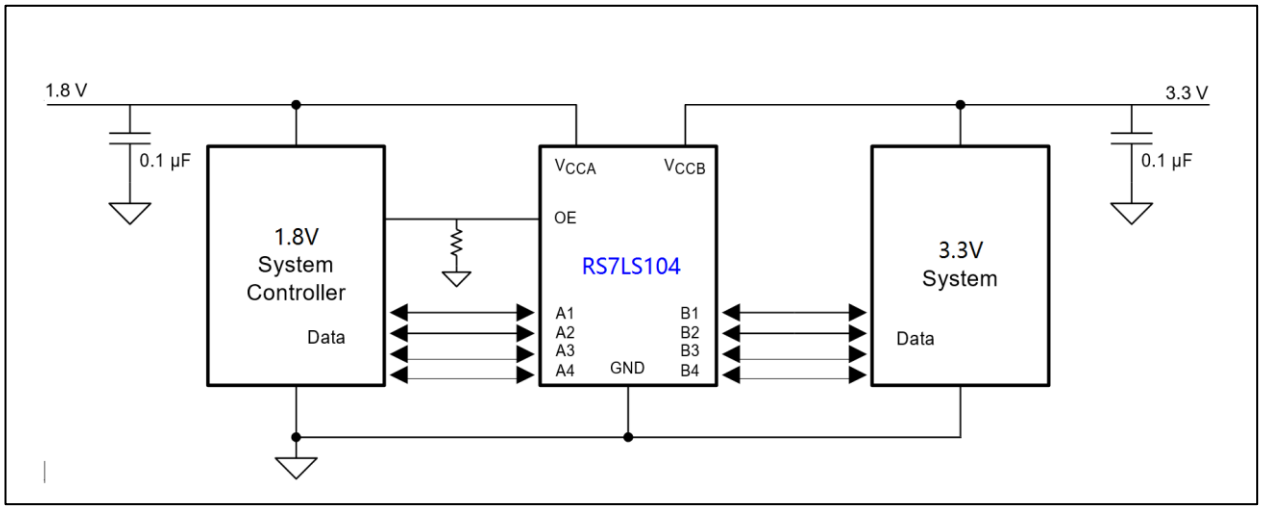


Figure 10 Application Circuit

Power Supply Guidelines

During normal operation, supply voltage V_{CCA} can be greater than, less than or equal to V_{CCB}. The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01µF to 0. 1µF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

Revision History

Revision	Description	DATE
1.0	Initial Release	2025/6/13