Features

- Control input threshold Referenced to V_{CCA} Voltage
- 1.1V to 1.95V on A Port and 1.65V to 5.5V on B Port
- V_{CC} Isolation: If Either VCC is at GND, both
- ports are in the High-Impedance State
- Output drives up to ±24mA@3.0V
- I_{OFF} circuitry provides partial Power-down mode operation
- Maximum data rates:
  - 420Mbps（1.8V to 5V Translation）
  - 210Mbps（Translate to 3.3V）
  - 140Mbps（Translate to 2.5V）
  - 75Mbps（Translate to 1.8V）
- ESD protection exceeds 4000V HBM, 1000V CDM
- Extended Temperature: -40°C to +125°C

Description

The RS7LS2T45 is a 2-bit, dual-supply transceiver that enables bidirectional level translation. It features two data input-output ports (nA and nB), a direction control input (DIR) and dual-supply pins (V_{CCA} and V_{CCB}). The nA and nB ports track the V_{CCA} supply and V_{CCB} supply respectively. The V_{CCA} pin accepts any supply voltage between1.1 V and 1.95 V. The V_{CCB} pin accepts any supply voltage between 1.65 V and 5.5 V. This makes the device suitable for low voltage bidirectional translation voltage nodes of 1.8V, 2.5V, 3.3V, and 5V. Pins nA and DIR are referenced to V_{CCA} and pins nB are referenced to V_{CCB}.

A HIGH on DIR allows transmission from nA to nB and a LOW on DIR allows transmission from nB to nA. The input circuit is always active on the two ports. A logic high or low must be set to avoid excessive supply current.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down.

Application

- Personal Electronic Devices
- Industrial and Enterprise Devices
- Telecommunications
- Personal Electronic

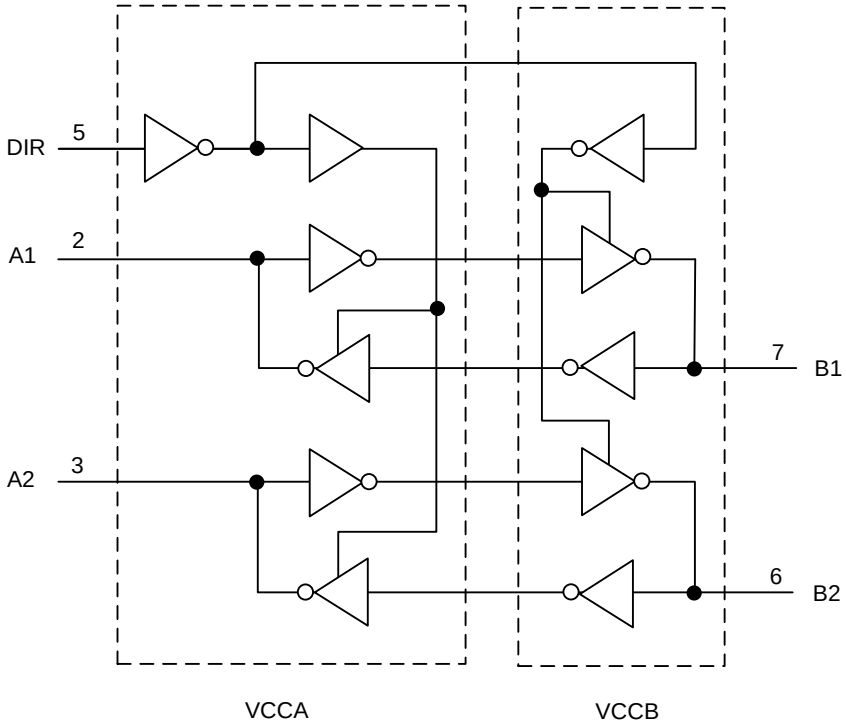
Ordering Information

Ordering Code	Package	Description
RS7LS2T45UE	MSOP8	3.00mm x 3.0mm
RS7LS2T45LE	TSSOP8	3.00mm x 4.4mm

Notes:

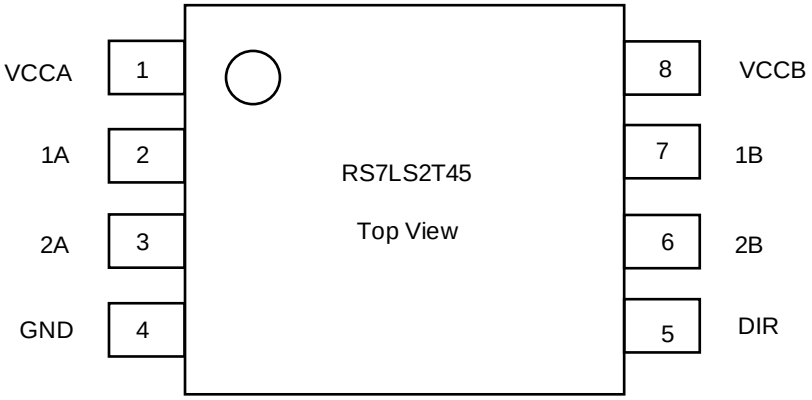
E = Pb-free and Green

Block Diagram



Functional block diagram

Pin Configuration



MSOP8/TSSOP8

PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{CCA}	1	P	A-port supply voltage. 1.1V ≤ V_{CCA} ≤ 1.95V
A1	2	I/O	Input/output A1. Referenced to V_{CCA}
A2	3	I/O	Input/output A2. Referenced to V_{CCA}
GND	4	G	Ground
DIR	5	I	Direction control signal
B2	6	I/O	Input/output B2. Referenced to V_{CCB}
B1	7	I/O	Input/output B1. Referenced to V_{CCB}
V_{CCB}	8	P	B-port supply voltage. 1.65V ≤ V_{CCB} ≤ 5.5V

I = input, O = output, P = power, G =ground

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	TYP	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage	–0.5		2.5	V
V_I Input voltage (2)		–0.5		6.5	V
V_O Voltage range applied to any output in the high-impedance or power-off state (2)		–0.5		6.5	V
V_O Voltage range applied to any output in the high or low state (2) (3)	A port	–0.5		V_{CCA} + 0.5	V
	B port	–0.5		V_{CCB} + 0.5	V
I_{IK} Input clamp current	V_I < 0	–50			mA
I_{OK} Output clamp current	V_O < 0	–50			mA
I_O Continuous output current		–50		50	mA
Continuous current through V_{CC} or GND		–100		100	mA
T_J Junction temperature				150	°C
T_{stg} Storage temperature		–65		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		V_{CCI}	V_{CCO}	MIN	TYP	MAX	UNIT
V_{CCA}	Supply voltage			1.1		1.95	V
V_{CCB}				1.65		5.5	
V_{IH} High-level input voltage	Data inputs (4)	1.1V to 1.95V		V_{CC} - 0.1			V
		2.3V to 2.7V		2.0			
		3V to 3.6V		2.5			
		4.5V to 5.5V		V_{CCI} × 0.7			
V_{IL} Low-level input voltage	Data inputs (4)	1.1V to 1.95V				0.1	V
		2.3V to 2.7V				0.5	
		3V to 3.6V				0.5	
		4.5V to 5.5V				V_{CC}× 0.3	
V_{IH} High-level input voltage	DIR (referenced to V_{CCA}) (5)	1.1V to 1.95V		V_{CC} - 0.1			V
		2.3V to 2.7V		2.0			
		3V to 3.6V		2.5			
		4.5V to 5.5V		V_{CCI} × 0.7			
V_{IL} Low-level input voltage	DIR (referenced to V_{CCA}) (5)	1.1V to 1.95V				0.1	V
		2.3V to 2.7V				0.5	
		3V to 3.6V				0.5	
		4.5V to 5.5V				V_{CC}× 0.3	
V_I Input voltage				0		5.5	V
V_O Output voltage				0		V_{CCO}	V
I_{OH} High-level output current			1.1V to 1.95V			–4	mA
			2.3V to 2.7V			–8	
			3V to 3.6V			–24	
			4.5V to 5.5V			–32	
I_{OL} Low-level output current			1.1V to 1.95V			4	mA
			2.3V to 2.7V			8	
			3V to 3.6V			24	
			4.5V to 5.5V			32	
Δt/Δv Input transition rise or fall rate	Data inputs	1.1V to 1.95V				20	ns/V
		2.3V to 2.7V				20	
		3V to 3.6V				10	
		4.5V to 5.5V				5	
	Control input	1.1V to 1.95V				5	
T_A Operating free-air temperature				-40		125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, VIL max = V_{CCI} × 0.3 V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, VIL max = V_{CCA} × 0.3 V.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C	–40°C to +125°C			UNIT
						MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100µA	$V_I = V_{IH}$	1.1V to 1.95V	1.65V to 4.5V		V_{CCO}-0.1			V
		I_{OH} = –4mA		1.1V to 1.95V	1.65V		1.2			
		I_{OH} = –8mA		1.1V to 1.95V	2.3V		1.9			
		I_{OH} = –24mA		1.1V to 1.95V	3V		2.4			
		I_{OH} = –32mA		1.1V to 1.95V	4.5V		3.8			
V_{OL}		I_{OL} = 100µA	$V_I = V_{IL}$	1.1V to 1.95V	1.65V to 4.5V				0.1	V
		I_{OL} = 4mA		1.1 V to 1.95V	1.65V				0.45	
		I_{OL} = 8mA		1.1 V to 1.95V	2.3V				0.3	
		I_{OL} = 24mA		1.1V to 1.95V	3V				0.55	
		I_{OL} = 32mA		1.1V to 1.95V	4.5V				0.55	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.1V to 1.95V	1.65V to 5.5V	±1			±2	µA
I_{off}	A port	V_I or V_O = 0 to 1.95 V		0V	0 to 5.5V	±1			±10	µA
	B port	V_I or V_O = 0 to 5.5 V		0 to 1.95V	0V	±1			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND		1.1V to 1.95V	1.65V to 5.5V	±1			±3	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1V to 1.95V	1.65V to 5.5V				10	µA
				1.95V	0V				-9	
				0V	5V				9	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1V to 1.95V	1.65V to 5.5V				12	µA
				1.95V	0V				-10	
				0V	5V				10	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.1V to 1.95V	1.65V to 5.5V				25	µA

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

AC Electrical characteristics

V_{CCA} = 1.2 V

over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.2	ns
t_{PHL}			2.8	14.3	2.2	8.5	1.8	7.1	1.7	7	
t_{PLH}	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t_{PHL}			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t_{PHZ}	DIR	A	2.2	30.9	2.1	30.5	2.1	30.5	2.1	29.3	ns
t_{PLZ}			1.9	19.7	1.9	19.6	1.9	19.5	1.9	19.4	
t_{PHZ}	DIR	B	4	27.9	3.5	14.9	3.1	11.3	2.7	8.6	ns
t_{PLZ}			3	19.5	2.9	12.6	2.9	9.7	2.4	7.1	
t_{PZH} (1)	DIR	A		37.2		28.6		25.2		22.2	ns
t_{PZL} (1)				42.2		27.8		23.9		20.8	
t_{PZH} (1)	DIR	B		37.4		29.9		27.8		26.6	ns
t_{PZL} (1)				45.2		39		37.6		36.3	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

V_{CCA} = 1.5 V

over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
t_{PHL}			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
t_{PLH}	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
t_{PHL}			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
t_{PHZ}	DIR	A	1.6	17.1	1.6	16.8	1.6	16.8	1.6	16.5	ns
t_{PLZ}			1.4	12.6	1.4	12.5	1.4	12.3	1.4	12.3	
t_{PHZ}	DIR	B	2.5	27.9	2.5	13.9	2.5	10.5	2.3	7.6	ns
t_{PLZ}			2	18.9	2	11.2	2	8.9	1.9	6.2	
t_{PZH} (1)	DIR	A		29.2		19.7		16.9		13.7	ns
t_{PZL} (1)				36.4		21.4		17.5		13.8	
t_{PZH} (1)	DIR	B		28.6		21		18.7		17.4	ns
t_{PZL} (1)				30		24.3		22.2		21.1	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

V_{CCA} = 1.8 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	15.5	1.4	8	0.7	5.6	0.7	4.4	ns
t_{PHL}			2	12.6	1.3	7	0.8	5	0.7	4	
t_{PLH}	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
t_{PHL}			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
t_{PHZ}	DIR	A	1.35	10.9	1.35	10.8	1.2	10.8	1.2	10.4	ns
t_{PLZ}			1.2	8.4	1.2	8.4	1.1	8.1	1.1	7.8	
t_{PHZ}	DIR	B	2.5	27.3	2.5	13.7	2.3	10.4	2	7.4	ns
t_{PLZ}			2	17.7	2	11.3	1.9	8.3	1.5	5.6	
t_{PZH} (1)	DIR	A		26		17.7		14.1		11	ns
t_{PZL} (1)				34.4		19.1		15.4		11.9	
t_{PZH} (1)	DIR	B		23.9		16.4		13.9		12.2	ns
t_{PZL} (1)				23.5		17.8		15.8		14.4	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

Operating Characteristics

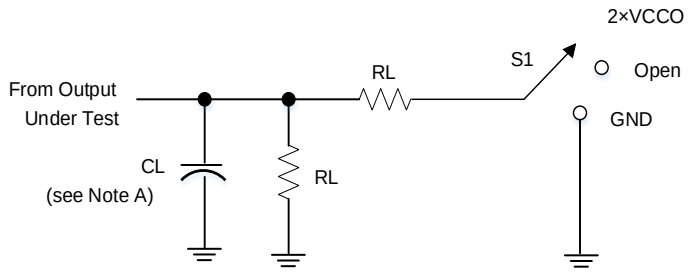
T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} =V_{CCB} = 1.8 V	V_{CCA} =V_{CCB} = 2.5 V	V_{CCA} =V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
C_{pdB} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	3	19	20	21	pF
	B-port input, A-port output		18	4	4	4	

(1) Power dissipation capacitance per transceiver.

Parameter Measurement Information

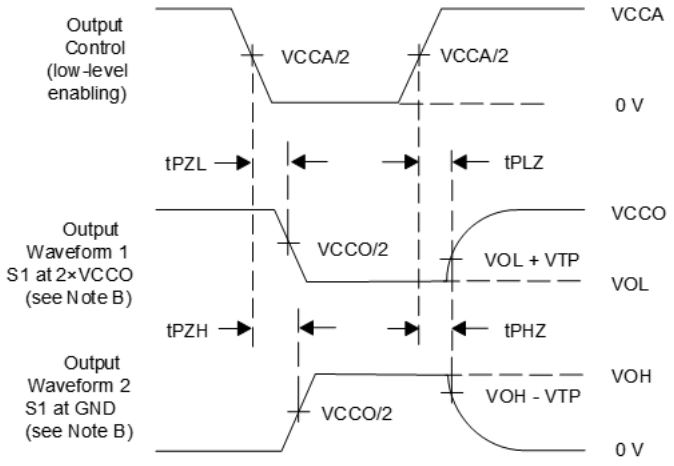
1. Circuit and voltage waveform of enable and disable times



LOAD CIRCUIT

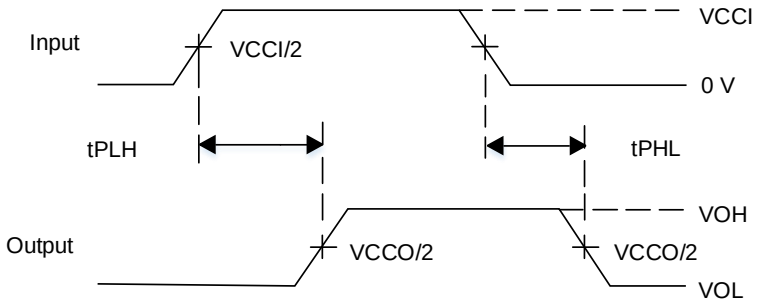
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
ENAVLLE AND DISABLE TIMES

2. Propagation Delay Times



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:

1. C_L includes probe and jig capacitance
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform2 is for an output with internal conditions such that the output is high, except when disabled by the output control
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.
10. V_{CCO} is the V_{CC} associated with the output port.

Description

Feature Description

1. **Fully Configurable Dual-Rail Design**

The V_{CCA} pin accepts any supply voltage between 1.1V and 1.95V. The V_{CCB} pin accepts any supply voltage between 1.65V and 5.5V. This makes the device suitable for low voltage bidirectional translation voltage nodes of 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V.

2. **Support High-Speed Translation**

RS7LS2T45 can support high data rate applications. The translated signal data rate can be up to 420 Mbps when signal is translated from 1.8 V to 5 V.

3. **Ioff Supports Partial-Power-Down Mode Operation**

I_{off} will prevent backflow current by disabling I/O output circuits when the device is in Partial-Power-Down mode. The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Electrical Characteristics.

4. **Balanced High-Drive CMOS Push-Pull Outputs**

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so impedance matching and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for a stronger output drive strength. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

5. **V_{CC} Isolation**

The I/O's of both ports will enter a high-impedance state when either of the supplies are at GND, while the other supply is still connected to the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Electrical Characteristics.

Device Functional Modes

lists the functional modes of the RS7LS2T45 device.

Function Table (Each Transceiver)(1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

Application and Implementation

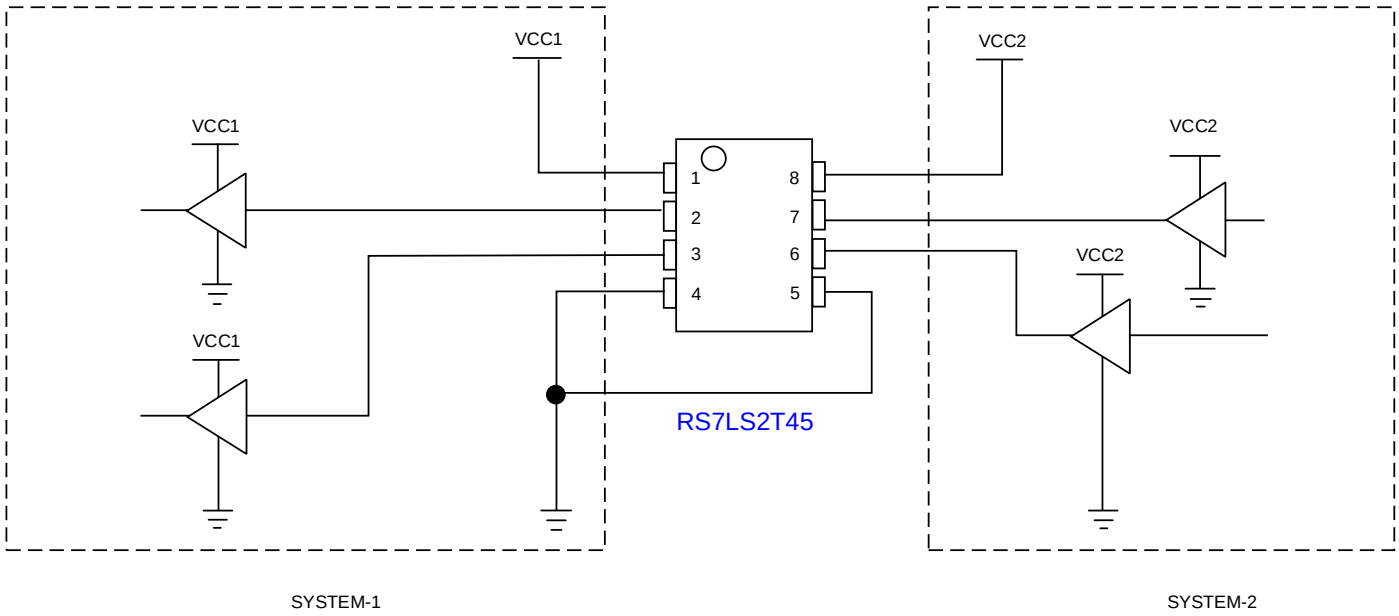
Application Information

The RS7LS2T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 420 Mbps when the device translates signal from 1.8V to 5V. It is recommended to tie all unused I/Os to GND. The device should not have any floating I/Os when changing translation direction.

Typical Applications

1. Unidirectional Logic Level-Shifting Application

This figure shows an example of the RS7LS2T45 being used in a unidirectional logic level-shifting application.



Unidirectional Logic Level-Shifting Application

(1) Design Requirements

RS7LS2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.1V to 1.95V)
2	A1	OUT1	Output level depends on VCC1 voltage.
3	A2	OUT2	Output level depends on VCC1 voltage.
4	GND	GND	Device GND.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	B2	IN2	Input threshold value depends on V_{CC2} voltage.
7	B1	IN1	Input threshold value depends on V_{CC2} voltage.
8	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.65 V to 5.5V)

(2) Detailed Design Procedure

To begin the design process, determine the following：

- Input voltage range

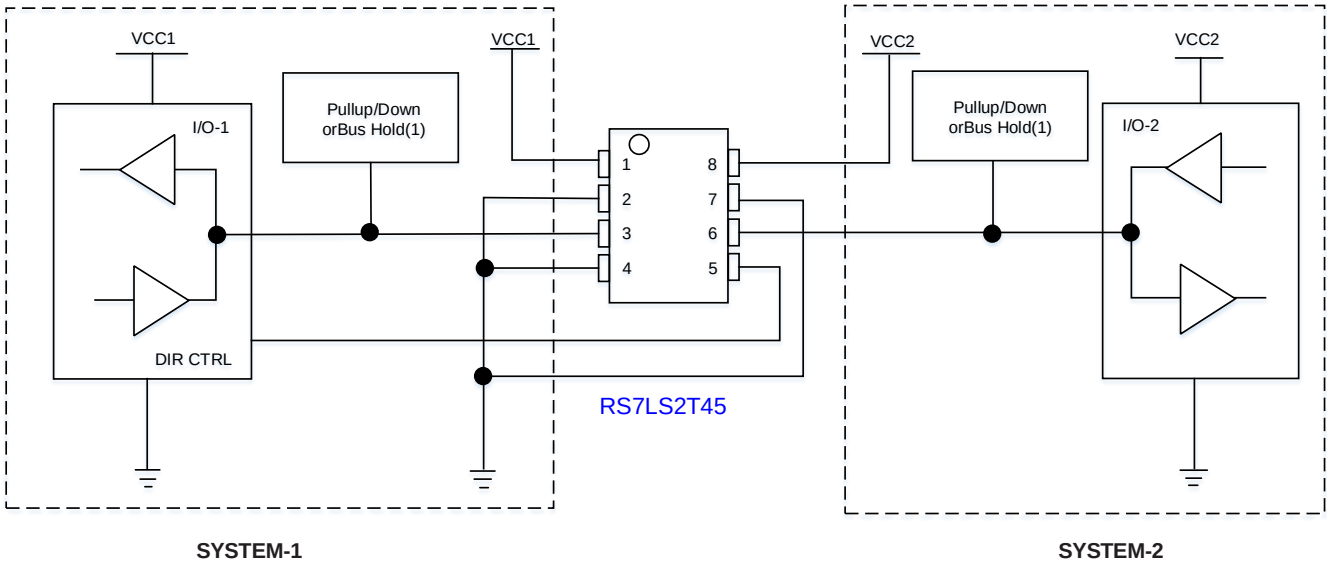
– Use the supply voltage of the device that is driving the RS7LS2T45 device to determine the input voltage range. For a valid logic high, the value must exceed the VIH of the input port. For a valid logic low, the value must be less than the VIL of the input port

- Output voltage range

– Use the supply voltage of the device that the RS7LS2T45 device is driving to determine the output voltage range

2. Bidirectional Logic Level-Shifting Application

This figure shows the RS7LS2T45 being used in a bidirectional logic level-shifting application. Because the RS7LS2T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions



Bidirectional Logic Level-Shifting Application

(1) Detailed Design Procedure

Data Transmission Sequence

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus- line state depends on pullup or pulldown. (1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. (1)
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

3. Enable Time

Calculate the enable times for the RS7LS2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the RS7LS2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

Power Supply Recommendations

Power-Up Considerations

A proper power-up sequence with inputs held at ground should be followed as listed:
(1) Connect ground before any supply voltage is applied.
(2) Power up $V_{CCA.}$
(3) V_{CCB} can be ramped up along with or after $V_{CCA.}$

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. The recommendation is to first power-up the input supply rail to help avoid internal floating while the output supply rail ramps up. However, both power-supply rails can be ramped up simultaneously.

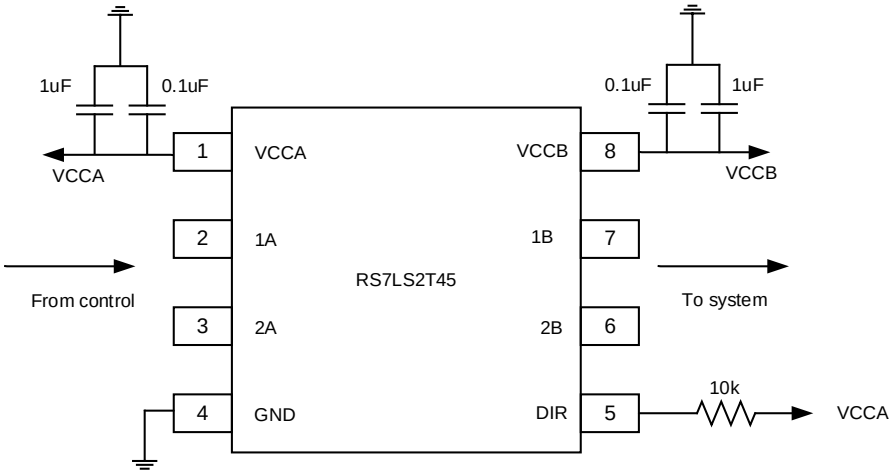
Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µF is recommended. If there are multiple V_{CC} pins, 0.01µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

Layout

Layout Guidelines

It is recommended to follow common printed-circuit board layout guidelines to ensure reliability of the device, such as the following:

- Use bypass capacitors on the power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements



Package Information

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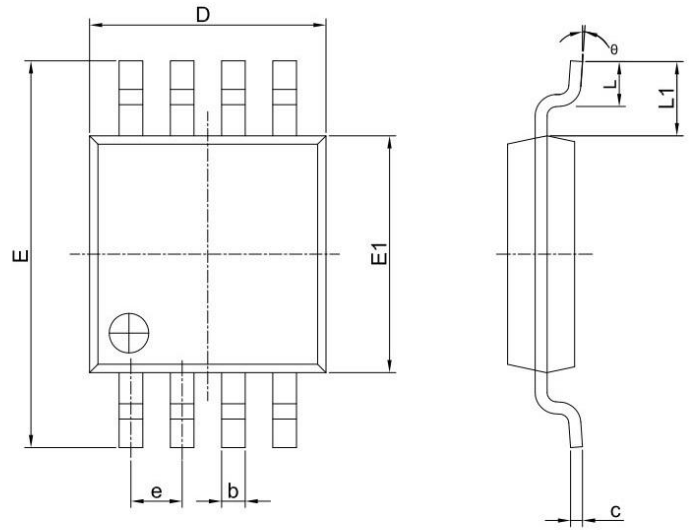
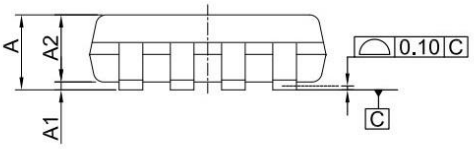


PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°



Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-187
3.Dimensions exclude burrs, mold flash or protrusions.

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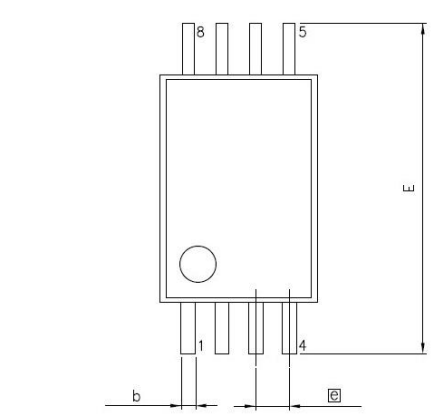
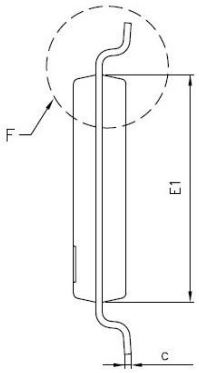
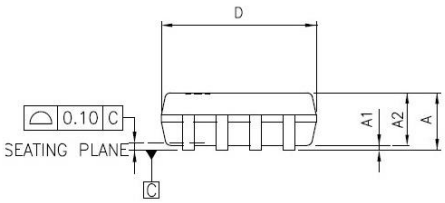
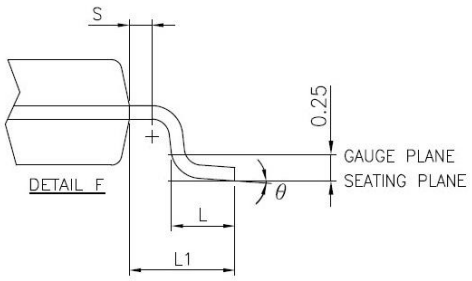




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E	6.20	6.40	6.60
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

UNIT : MM





Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-153F
3.Dimensions exclude burrs, mold flash or protrusions.

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Revision History

Revision	Description	DATE
V0.9	Preliminary	2024/6/14
V1.0	Initial Release	2025/6/20