Features

- Using external 32.768kHz quartz crystal
- I^2C-Bus Supports high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Oscillator stop flag
- Low backup current: typ. 400nA at V_{DD}=3.0V and T_A=25°C
- Operating range: 1.7V to 5.5V
- Operating Temperature Range: -40~125 ºC
- AEC-Q 100 qualified. PPAP capable, and manufactured in IATF 16949 certified facilities.

Description

The IT8563Q serial real-time clock is a low-power clock/calendar with a programmable square-wave output.

Address and data are transferred serially via a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in the 24-hour format indicator.

IT8653Q is suitable for automotive applications requiring specific change control.

Table 1 shows the basic functions of IT8563Q. More details are shown in section overview of functions.

Ordering Information

Part Number	Package	Description
IT8563QWE	W	SOIC8
IT8563QUE	U	MSOP8

Note：E= Green Package

Table 1. Basic functions of IT8563Q

Item	Function			IT8563Q
1	Oscillator	Source: Crystal: 32.768kHz		√
		Oscillator enable/disable		-
		Oscillator fail detect		√
2	Time	Time display	12-hour	-
			24-hour	√
		Century bit		-
		Time count chain disable		-
3	Interrupt	Alarm interrupt		√
4	Programmable square wave output (Hz)			1, 32, 1.024k, 32.768k
5	Communication	2-wire I²C bus		√
		Burst mode		√
6	Control	Write protection		-
		External clock test mode		√
		Power-on reset override		√

Function Block

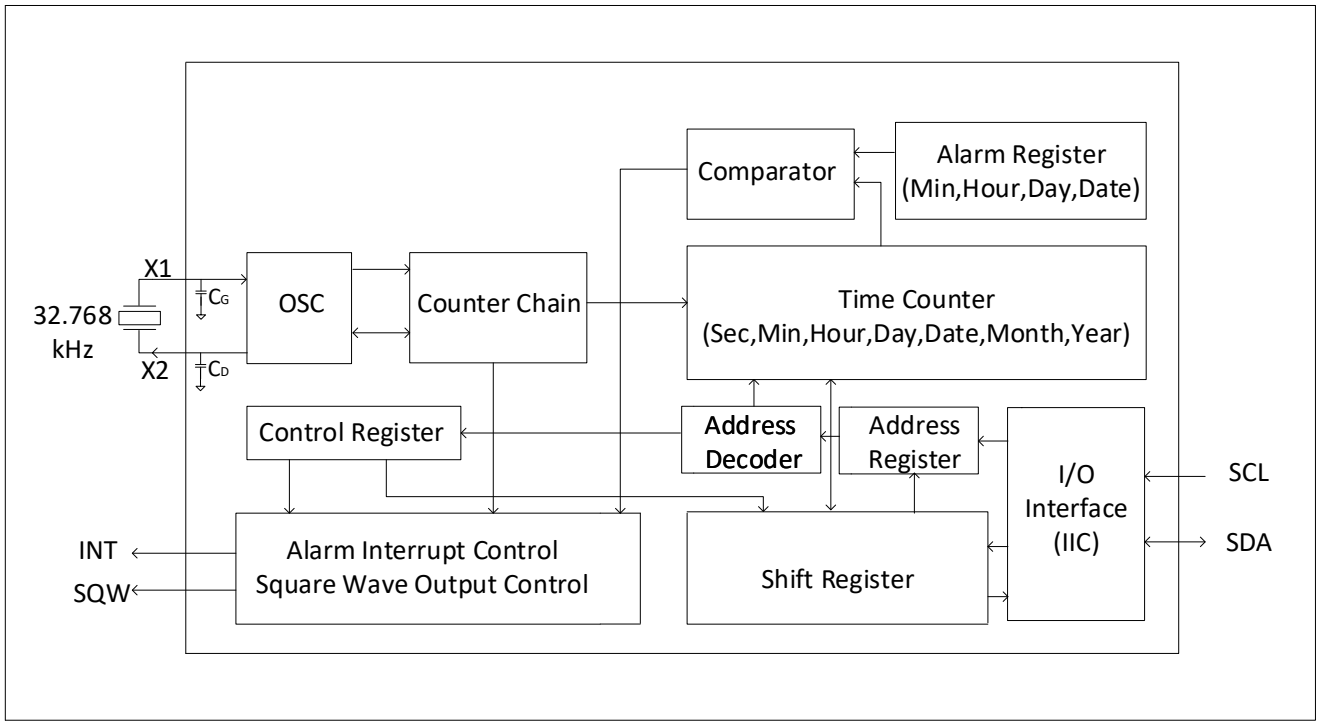


Figure 1. Function Block

Pin Configuration

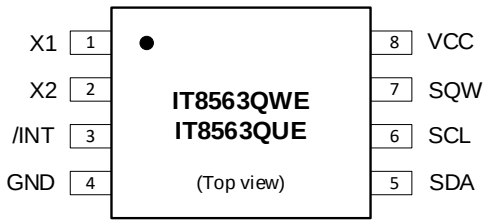


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them.
3	/INT	O	**Interrupt Output.** Open drain, active low.
4	GND	P	**Ground.**
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
7	SQW	O	**Clock Output.** Open drain. Four frequencies selectable: 32.768k, 1.024k, 32, 1Hz when SQWE bit is set to 1.
8	VCC	P	**Power.**

Typical Application Circuit

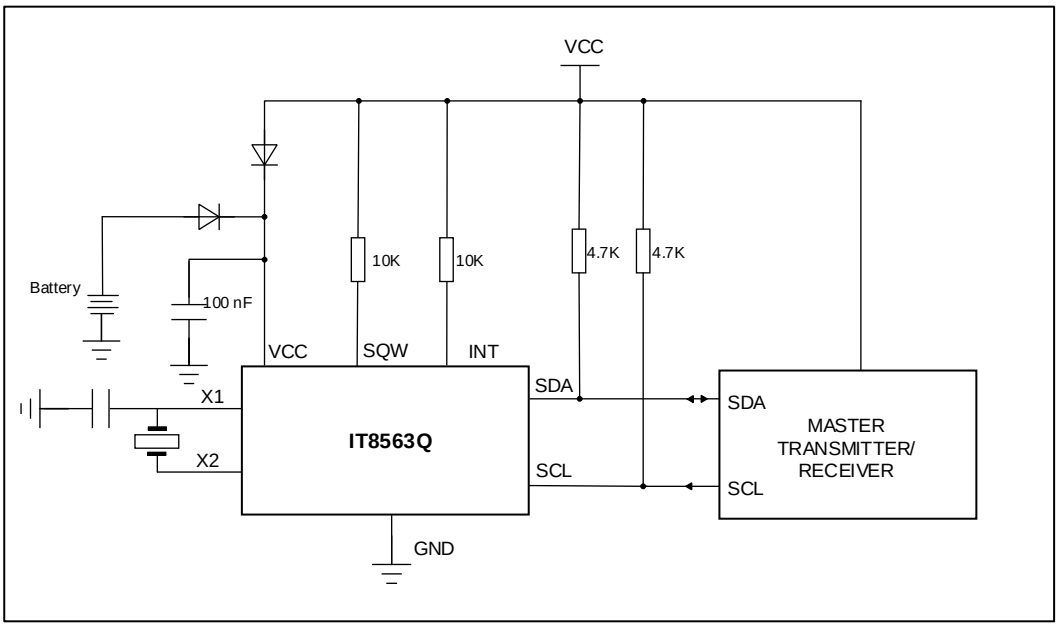


Figure 3. Typical application circuit

Note:

1、For non-P versions:

X1 build-in capacitors is 0pF, external matching capacitor is required for design.

X2 build-in capacitors is 23pF, external matching capacitors are not required.

2、For P versions:

X1 build-in capacitors is 5pF, external matching capacitor is required for design.

X2 build-in capacitors is 19pF, external matching capacitors are not required.

Function Description

1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

2. Alarm function

This device has one alarm system that outputs interrupt signals from /INT of IT8563Q when the date, day of the week, hour or minute correspond to the setting. Each of them may output interrupt signal separately at a specified time.

3. Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. Four frequencies are selectable: 1, 32, 1.024k, 32.768k Hz.

4. IIC Interface

Data is read and written via the I^2C bus ,the SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

5. Oscillator fail detect

When oscillator fail, OSF bit will be set.

Registers

Registers map

Addr. (hex)	Function (time range BCD format)	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Control/status 1	×	×	×	×	×	×	×	×
01	Control/status 2	×	×	×	×	AF*1	×	AIE*2	×
02	Seconds (00-59)	OSF*3	S40	S20	S10	S8	S4	S2	S1
03	Minutes (00-59)	×	M40	M20	M10	M8	M4	M2	M1
04	Hours (00-23)	×	×	H20	H10	H8	H4	H2	H1
05	Dates (01-31)	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week (00-06)	×	×	×	×	×	W4	W2	W1
07	Months (01-12)	×	×	×	MO10	MO8	MO4	MO2	MO1
08	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
09	Alarm: Minutes (00-59)	AE*4	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours (00-23)	AE*4	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates (01-31)	AE*4	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday (00-06)	AE*4	×	×	×	×	W4	W2	W1
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0

Notes:

*1. Alarm interrupt flag bits.

*2. Alarm interrupt enable bits.

*3. Oscillator fail indicates. Indicate clock integrity.

*4. Alarm enable bit. Alarm will be active when related time is matching if AE = 0.

*5. All bits marked with "×" are not implemented.

Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Control/status 1	×	×	×	×	×	×	×	×
	(default)	0	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined
01	Control/status 2	×	×	×	×	AF	×	AIE	×
	(default)	Undefined	Undefined	Undefined	0	Undefined	Undefined	0	0
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	0	0

a) Alarm Interrupt

- **AIE:** Alarm Interrupt Enable bit.

AIE	Data	Description	
Read / Write	0	Alarm interrupt disabled	Default
	1	Alarm interrupt enabled	

- **AF:** Alarm Flag

AF	Data	Description
Read	0	Alarm flag inactive
	1	Alarm flag active
Write	0	Alarm flag is cleared
	1	Alarm flag remains unchanged

b) SQW control

- **SQWE:** SQW output clock enable bit.

SQWE	Data	Description	
Read / Write	0	the SQW output is inhibited and SQW output is set to high impedance	
	1	the SQW output is activated	Default

- **RS1, RS0:** SQW output frequency select.

RS1, RS0	Data	SQW output freq. (Hz)	
Read / Write	00	32.768k	Default
	01	1.024k	
	10	32	
	11	1	

Time Counter

1. Time digit display (in BCD code):

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
02	Seconds	OSF*1	S40	S20	S10	S8	S4	S2	S1
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
04	Hours	×	×	H20	H10	H8	H4	H2	H1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note1:Indicate clock integrity. When the bit is 1, the clock integrity is no longer guaranteed and the time need be adjusted.

2. Weekday Counter

The Weekday counter is a divide-by-7 counter that counts from 00 to 06 and up 06 before starting again from 00. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
06	Days of the week	×	×	×	×	×	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

3. Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
05	Dates	×	×	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
07	Months	×	×	×	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
08	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Alarm Register

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
09	Alarm: Minutes	AE*1	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm: Hours	AE*2	×	H20	H10	H8	H4	H2	H1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm: Dates	AE*3	×	D20	D10	D8	D4	D2	D1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm: Weekday	AE*4	×	×	×	×	W4	W2	W1
	(default)	Undefined	0	0	0	0	Undefined	Undefined	Undefined

Notes:
1: Minute alarm enable bit.
2: Hour alarm enable bit.
3: Date alarm enable bit.
4: Weekday alarm enable bit.

Alarm Function

	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	Control/status 2	×	×	×	×	AF	×	AIE	×
02	Seconds	OSF	S40	S20	S10	S8	S4	S2	S1
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
04	Hours	×	×	H20	H10	H8	H4	H2	H1
05	Dates	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week	×	×	×	×	×	W4	W2	W1
09	Alarm: Minutes	AE	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours	AE	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates	AE	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday	AE	×	×	×	×	W4	W2	W1

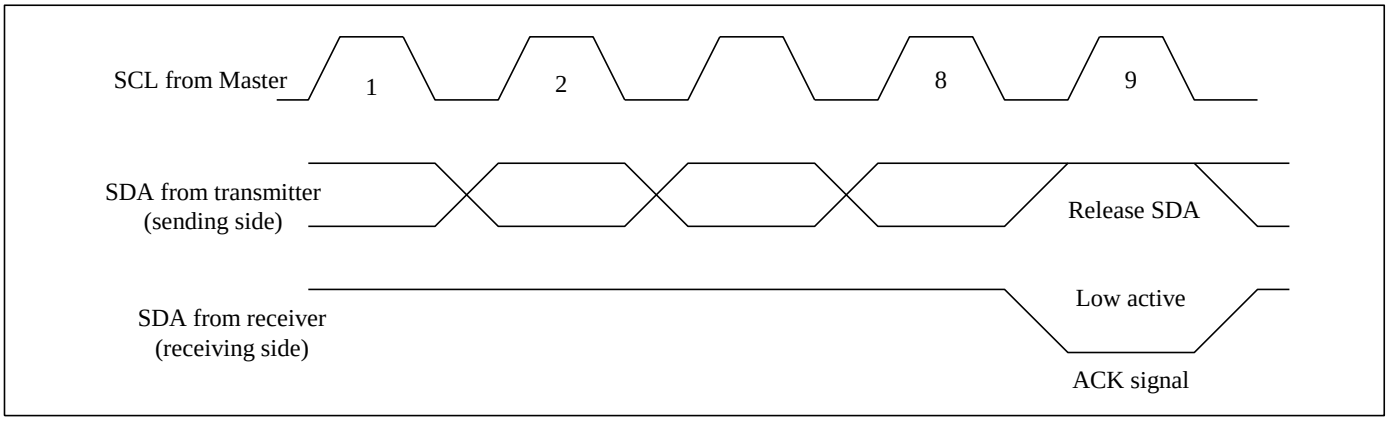
Notes:
1、one or more of alarm registers are loaded with a valid minute, hour, day or weekday and its corresponding bit Alarm Enable (AE) is logic 0
2、compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set to 1.
3、AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more.
4、Alarm registers which have their bit AE at logic 1 will be ignored.

I²C Bus Interface

Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

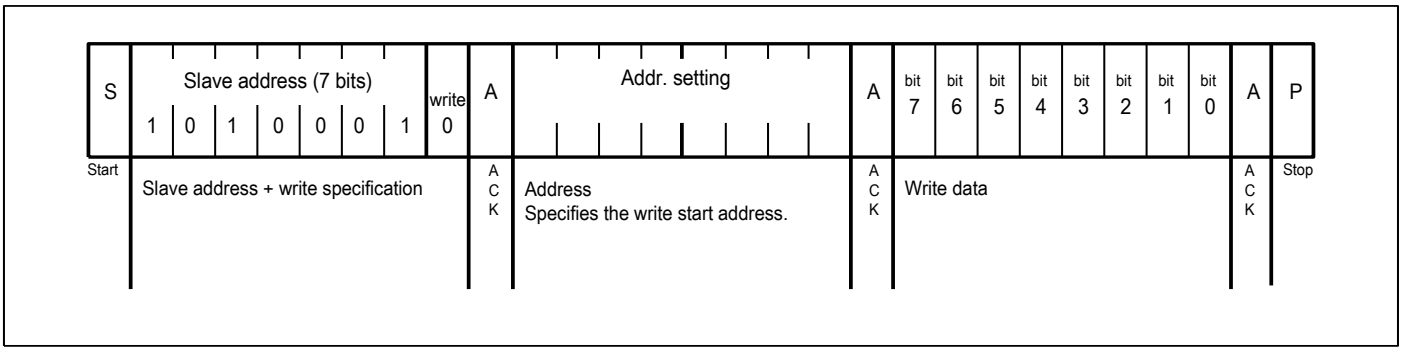
Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

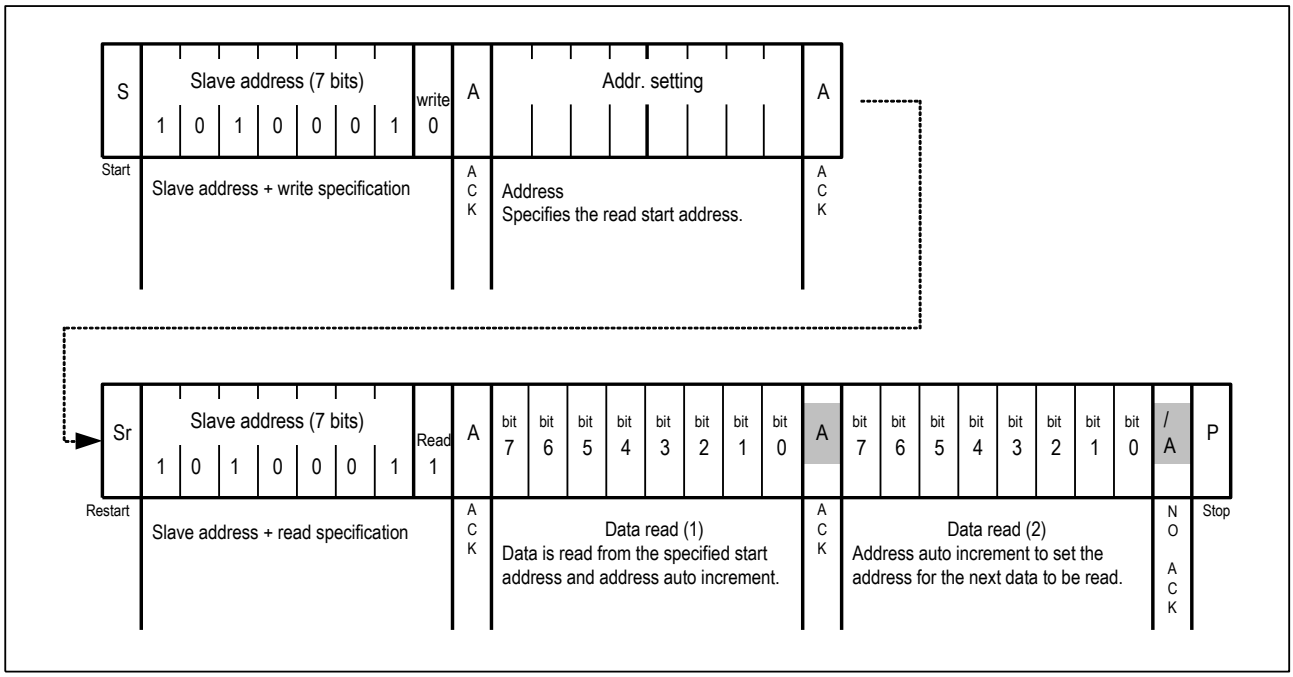
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Write via I²C bus

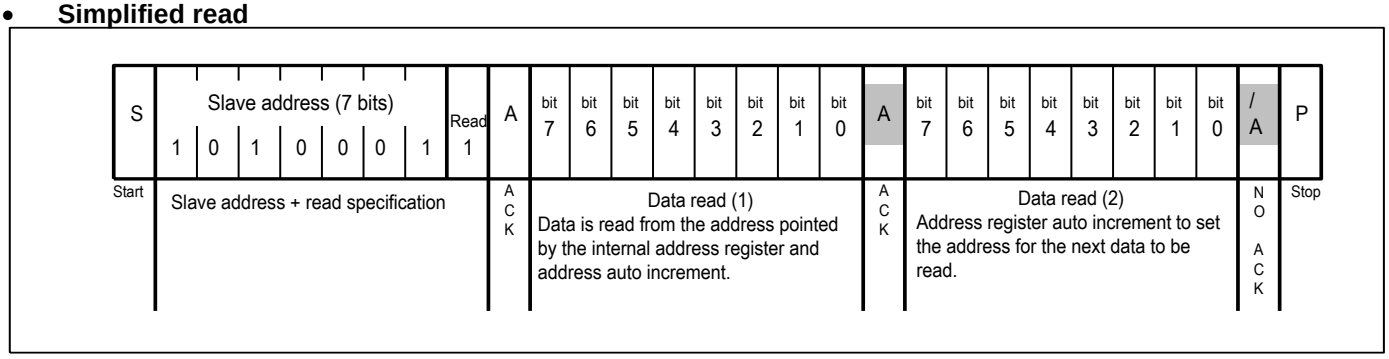


Read via I²C bus

Standard read



- **Simplified read**



Note:

1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.

Absolute Maximum Ratings

Storage Temperature	-65° C to +150° C
Ambient Temperature with Power Applied	-40° Cto +125° C
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to (Vcc+0.3V)
DC Output Voltage (SDA, /INT pins)	-0.3V to +6.5V
Power Dissipation	320mW (Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
V_{CC}	Power voltage	1.7	-	5.5	V
V_{IH}	Input high level	0.7 V_{CC}	-	V_{CC}+0.3	
V_{IL}	Input low level	-0.3	-	0.3 V_{CC}	
T_A	Operating temperature	-40	-	125	ºC

DC Electrical Characteristics

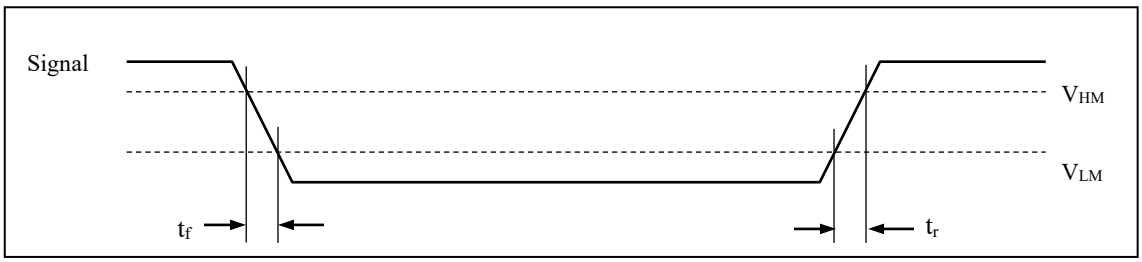
Unless otherwise specified, GND =0V, V_{CC} = 1.7 ~ 5.5 V, T_A = -40 °C to +125 °C, f_{OSC} = 32.768kHz.

Symbol	Description	Pin	Conditions		MIN	TYP	MAX	Unit
V_{CC}	Supply voltage	V_{CC}	Interface inactive. T_A = 25°C 1)		1.5	-	5.5	V
			Interface active. f_{SCL} = 400kHz 1)		1.7	-	5.5	
	Supply voltage for clock data integrity	V_{CC}	-		1.5	-	5.5	
I_{CC}	Supply current	V_{CC}	Interface active	f_{SCL} = 400kHz	-	-	25	µA
				f_{SCL} = 100kHz	-	-	15	
			Interface inactive (f_{SCL} = 0Hz), pin 7 disabled T_A=-40~125°C	V_{CC} = 5.0V	-	0.45	1.5	uA
				V_{CC} = 3.0V	-	0.4	1.5	
			Interface inactive (f_{SCL} = 0Hz), pin 7 enabled at 32kHz T_A=-40~125°C	V_{CC} = 5.0V	-	0.65	1.5	uA
				V_{CC} = 3.0V	-	0.6	1.5	
V_{IL1}	Low-level input voltage	SCL	-		0	-	0.3V_{CC}	V
V_{IH1}	High-level input voltage	SCL	-		0.7V_{CC}	-	V_{CC}	
I_{OL}	Low-level output voltage	SDA	V_{OL} = 0.4V, V_{CC} = 5V		-3	-	-	mA
		/INT, SQW	V_{OL} = 0.4V, V_{CC} = 5V		-1	-	-	
I_{IL}	Input leakage current	SCL	-		-	-	±1	µA
I_{OZ}	Output current when OFF	-	-		-	-	±1	µA

Note:
1、For reliable oscillator start-up at power-up: $V_{CC(min)power-up}$ = $V_{CC(min)}$ + 0.3 V

AC Electrical Characteristics

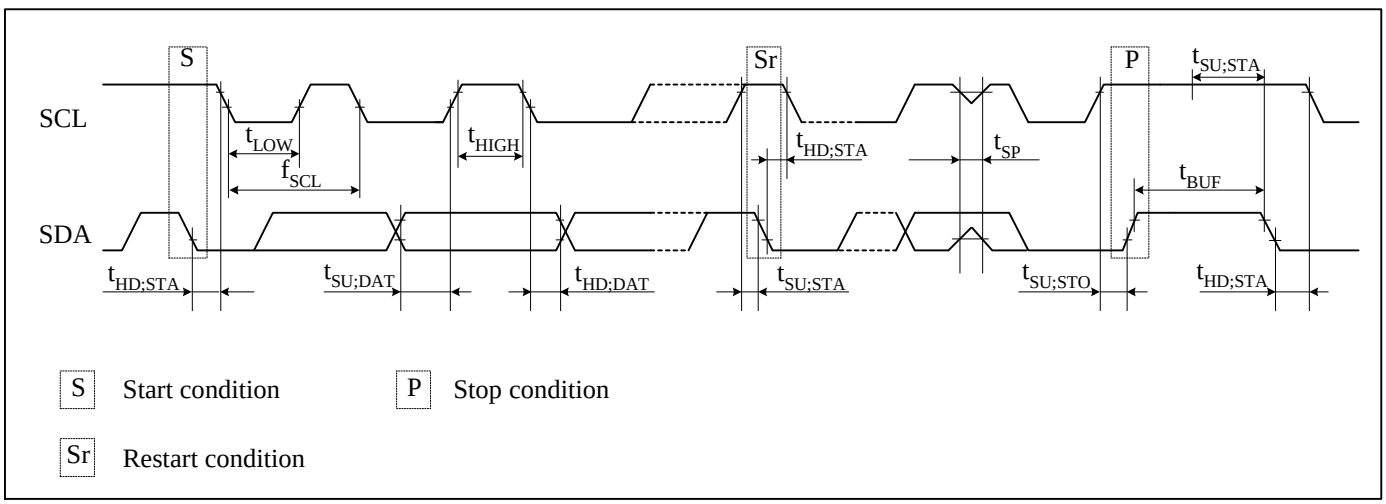
Symbol	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{LM}	Rising and falling threshold voltage low	0.2 V_{CC}	V



Over the operating range

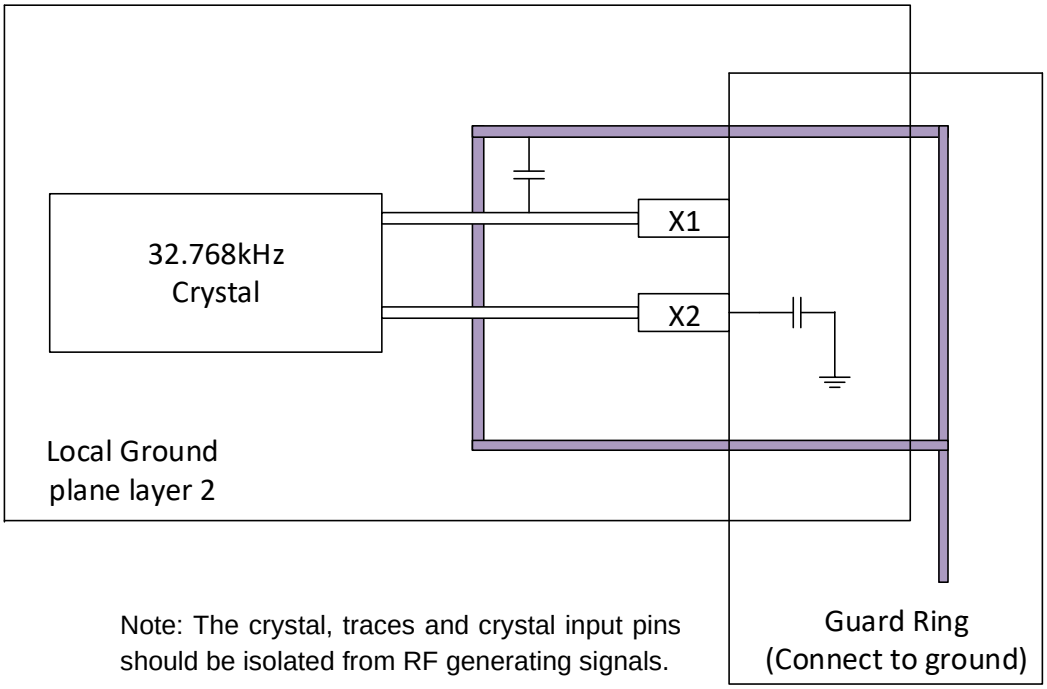
Symbol	Description	MIN	TYP	MAX	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
$t_{SU;STA}$	START condition set-up time	0.6	-	-	µs
$t_{HD;STA}$	START condition hold time	0.6	-	-	µs
$t_{SU;DAT}$	Data set-up time (RTC read/write in Fast mode)	100	-	-	ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35	-	-	ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0	-	-	µs
$t_{SU;STO}$	STOP condition setup time	0.6	-	-	µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3	-	-	µs
t_{LOW}	When SCL = "L"	1.3	-	-	µs
t_{HIGH}	When SCL = "H"	0.6	-	-	µs
t_r	Rise time for SCL and SDA	-	-	0.3	µs
t_f	Fall time for SCL and SDA	-	-	0.3	µs
t_{SP}*	Allowable spike time on bus	-	-	50	ns
C_B	Capacitance load for each bus line	-	-	400	pF

Note: Only reference for design.



Recommended Layout for Crystal

Not P Version：



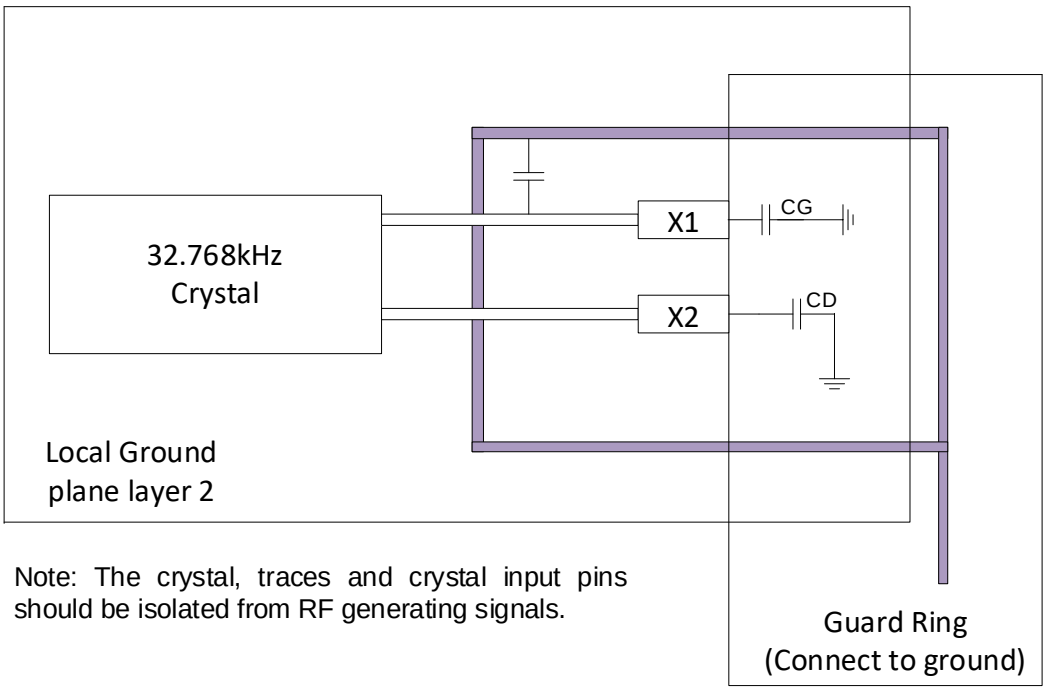
Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Symbol	Parameter		TYP	Unit
C_G	Build-in capacitors	X1 to GND	0	pF
C_D		X2 to GND	23	pF
C1	Recommended External capacitors for crystal **CL=12.5pF**	X1 to GND	22	pF
C2		X2 to GND	0	pF
C1	Recommended External capacitors for crystal **CL=6pF**	X1 to GND	7	pF
C2		X2 to GND	0	pF

P Version：

（The first letter of the last line of silk-screen printing is "P".）



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

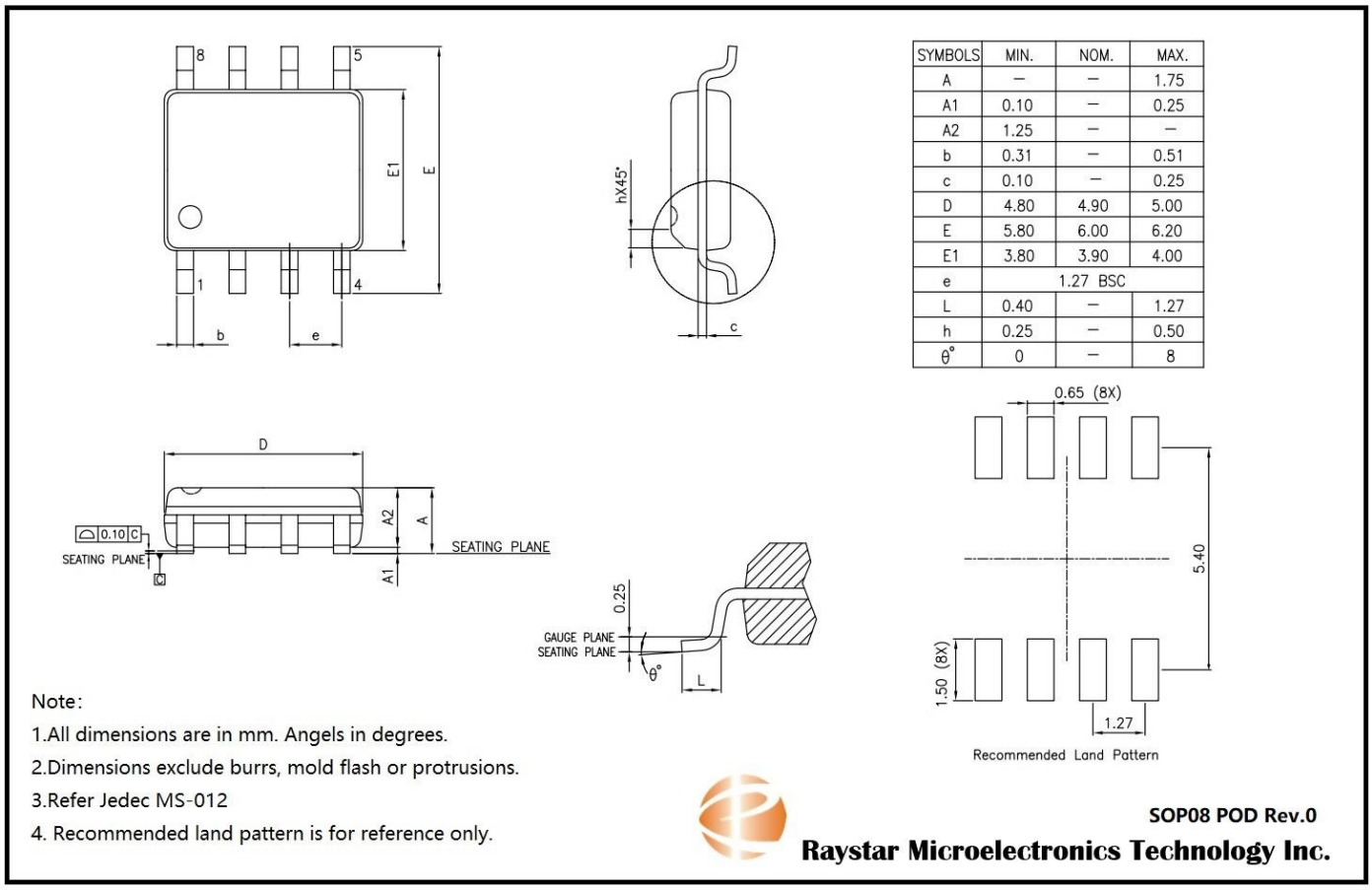
Symbol	Parameter		TYP	Unit
CG	Build-in capacitors	X1 to GND	**5**	pF
CD		X2 to GND	**19**	pF
C1	Recommended External capacitors for crystal **CL=12.5pF**	X1 to GND	22	pF
C2		X2 to GND	0	pF
C1	Recommended External capacitors for crystal **CL=6pF**	X1 to GND	0	pF
C2		X2 to GND	0	pF

Crystal Specifications

Symbol	Parameter	MIN	TYP	MAX	Unit
fo	Nominal Frequency	-	32.768	-	kHz
ESR	Series Resistance	-	-	70	kΩ
CL	Load Capacitance	-	6/12.5	-	pF

Package Information

WE (Lead free SOP8)

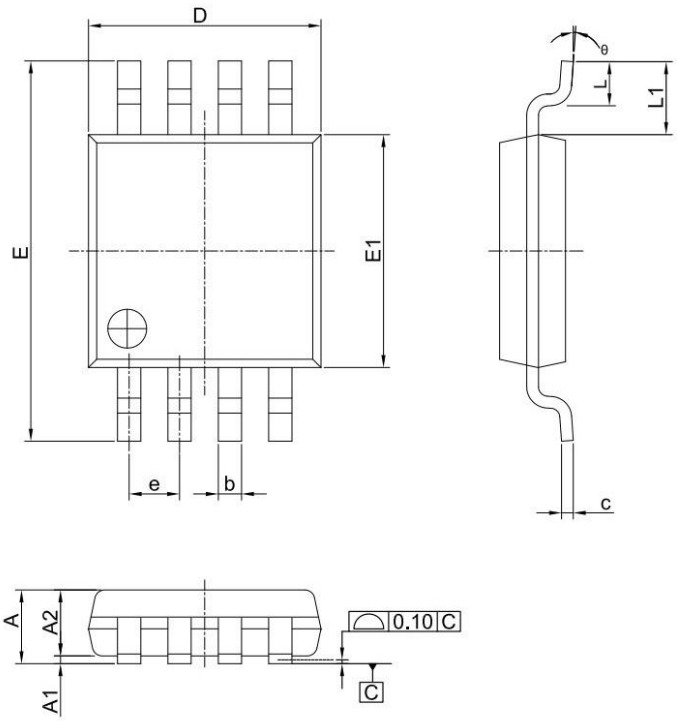


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD Rev.0
Raystar Microelectronics Technology Inc.

UE (Lead free and Green MSOP-8)



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-187
3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08 POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.9	Modify POD	2023/4/23
V2.0	Update Data set-up time (RTC read/write in Fast mode) to 100ns	2023/6/01
V2.1	Add feature of AEC-Q100 qualified	2023/6/12
V2.2	Update ICC spec	2023/10/9
V2.3	Add reference design circuit	2024/7/16
V2.4	Delete a TSSOP8 package	2024/12/10
V2.5	Add descriptions of internal matching capacitors for different versions	2025/4/27