Features

- 2.97 to 3.63V operating supply voltage range
- Operating frequency optional:
  74.25MHz,100MHz,125MHz,148.5MHz
  150MHz,156.25MHz,162MHz,200MHz,
  212.5MHz,250MHz,312.5MHz,625MHz
- Operating Temperature Range: -40 to +125℃
- Differential LVDS/LVPECL output
- Standby function
- Power-saving pull-up resistor built-in (Pin OE)
- TDFN-8L package

Applications

- Automotive, and other high reliability electronics
- Infotainment systems, collision detection device

Electrical Characteristics

Table 1: Electrical Characteristics – Common to LVPECL and LVDS

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Output Frequency Range	F_{OUT}	74.25		625	MHz	Refer Features
Operating Temperature Range	T_{USE}	-20	-	+70	°C	AEC-Q100 Grade 4
		-40	-	+85	°C	AEC-Q100 Grade 3
		-40	-	+105	°C	AEC-Q100 Grade 2
		-40	-	+125	°C	AEC-Q100 Grade 1
Supply Voltage	V_{DD}	2.97	3.3	3.63	V	
Input Voltage High	V_{IH}	0.7	-	-	V_{DD}	
Input Low High	V_{IL}	-	-	0.3	V_{DD}	
Current consumption1	I_{EE1}	-	70	90	mA	OE= H or floating
Current consumption2	I_{EE2}	-	50	70	mA	OE=L
Duty Cycle	DC	45	-	55	%	
Rise Time	T_R	-	0.2	0.4	ns	20 to 80% output swing
Fall Time	T_F	-	0.2	0.4	ns	80 to 20% output swing
RMS Phase Jitter	Jitter	-	0.3	0.4	ps	100MHz@12K~20M, T_A=25℃
Start-time	T_{STAR}	-	-	3	ms	Measured from the time V_{DD} reaches its rated minimum value
OE Enable Time	T_{OE}	-	-	5	us	f = 625MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z.
OE Disable Time	T_{OD}	-	-	200	ns	

Note: All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 2: Electrical Characteristics – LVPECL

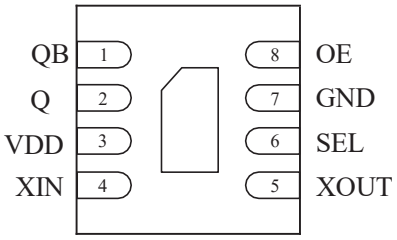
3.3V operation (V_{DD} = 2.97 to 3.63V, T_A = -40 to +125°C, GND = 0V, unless otherwise noted.)

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
HIGH-level output voltage	V_{OH}	V_{DD}-1.4		V_{DD}-0.8	V	
LOW-level output voltage	V_{OL}	V_{DD}-2		V_{DD}-1.6	V	
Output swing	V_{OPP}	0.6	-	1	V	

Table 3: Electrical Characteristics – LVDS
3.3V operation (V_{DD} = 2.97 to 3.63V, T_A = -40 to +125°C, GND = 0V, unless otherwise noted.)

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
HIGH-level output voltage	V_{OH}	-	1.4	-	V	
LOW-level output voltage	V_{OL}	-	1.0	-	V	
Output swing	V_{OPP}	-	0.4	-	V	See Figure 4
Differential Output Voltage	VOD	250		450	mV	See Figure 4
VOD Magnitude Change	ΔVOD			50	mV	See Figure 4
Offset Voltage	VOS	1.125		1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS			50	mV	See Figure 4

Pad Description



Pin	Type	Description
1	QB	Output pin (complementary).
2	Q	Output pin (true).
3	VDD	Supply voltage.
4	XIN	Crystal Oscillator Input.
5	XOUT	Crystal Oscillator Output.
6	SEL	Efuse control pin. Pull-down resistor built-in. Tri-state pin
7	GND	Ground (-).
8	OE	Output enable pin. Output off when OE=L Power-saving pull-up resistor built-in. Tri-state pin

Note: A capacitor of value 0.1 µF or higher between V_{DD} and GND is required. An additional 10 µF capacitor between V_{DD} and GND is required for the best phase jitter performance

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage Temperature	-55	150	°C
Supply Voltage range	-0.5	4.0	V
Input voltage range	GND-0.5	VDD+0.5	V
Output voltage range	GND-0.5	VDD+0.5	V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Waveform Diagrams

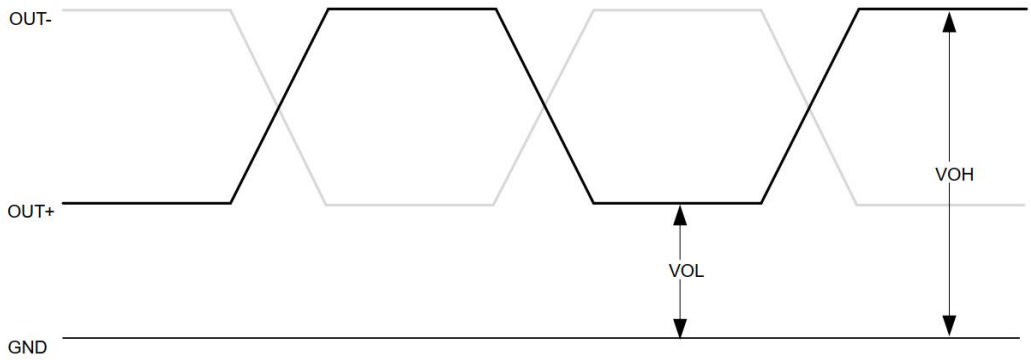


Figure 2: LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

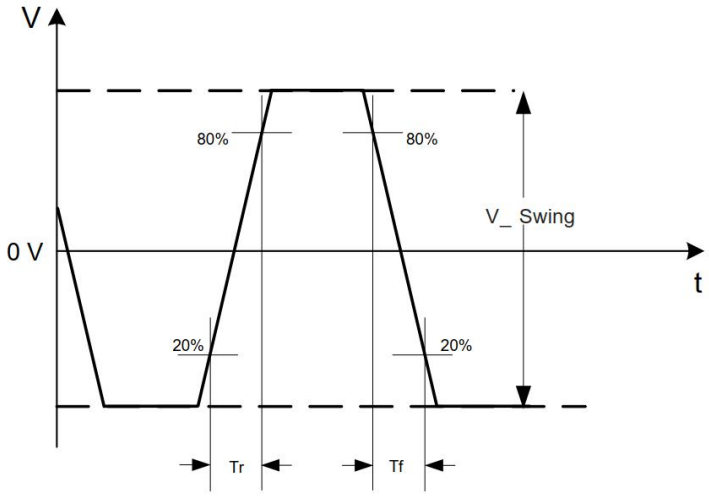


Figure 3: LVPECL Voltage Levels across Differential Pair

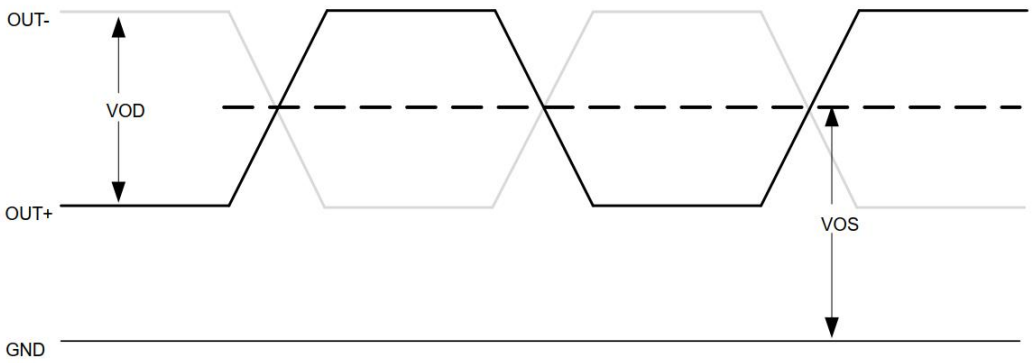


Figure 4: LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Waveform Diagrams (Continued)

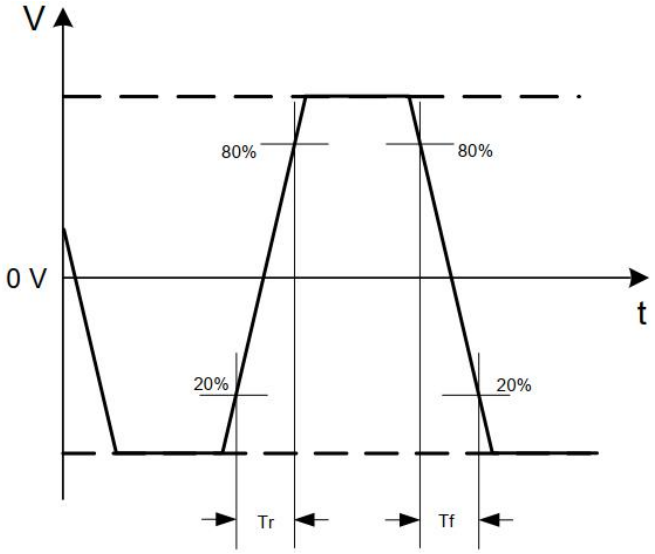


Figure 5: LVDS Differential Waveform

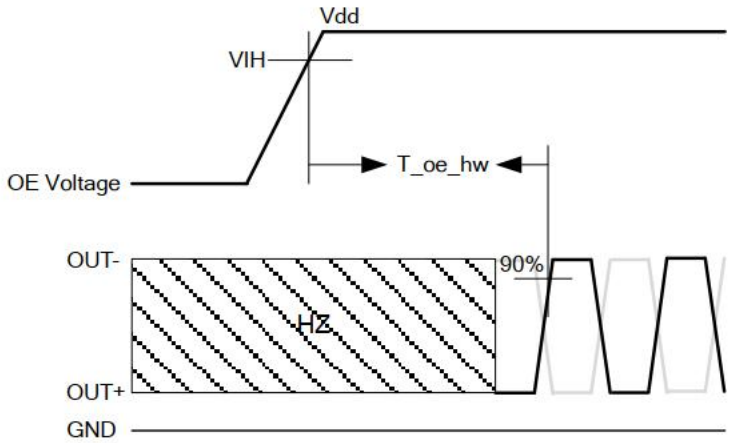


Figure 6: Hardware OE Enable Timing

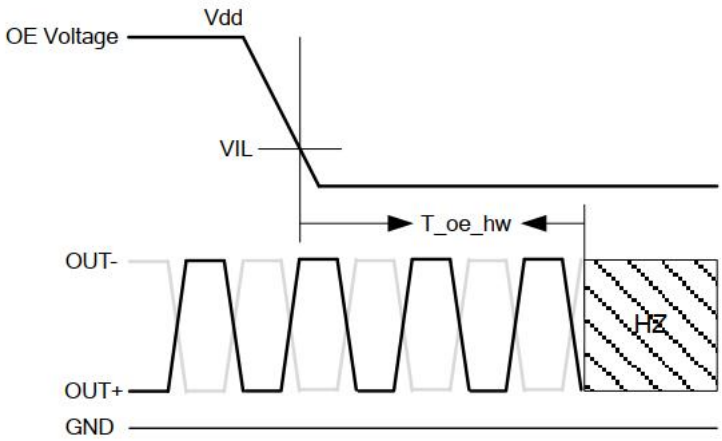


Figure 7: Hardware OE Disable Timing

Termination Diagrams

LVPECL

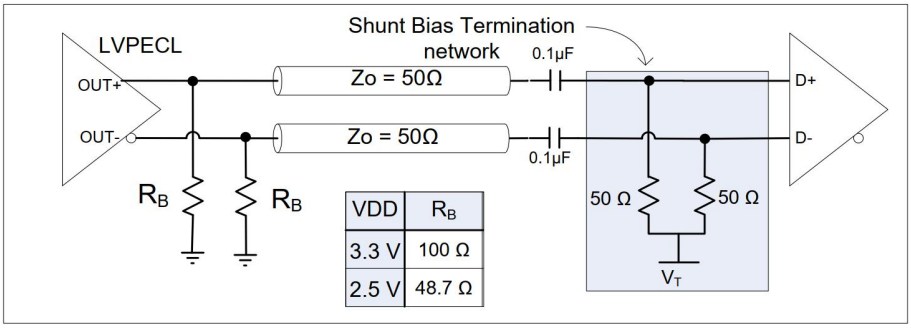


Figure 8: LVPECL with AC-coupled termination

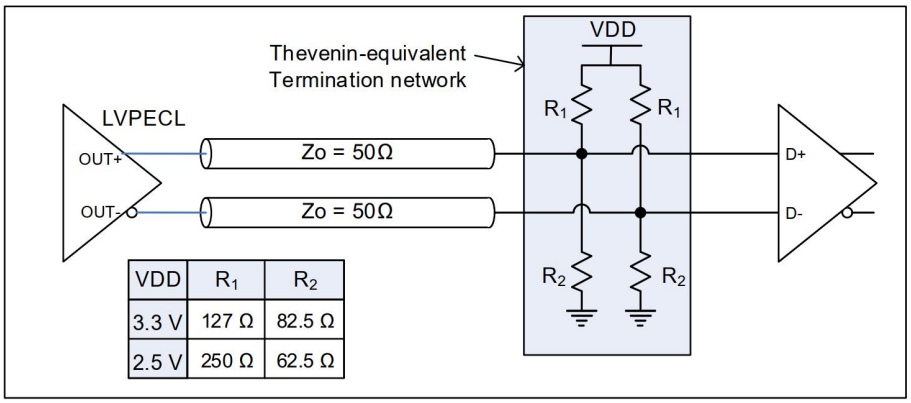


Figure 9: LVPECL DC-coupled load termination with Thevenin equivalent network

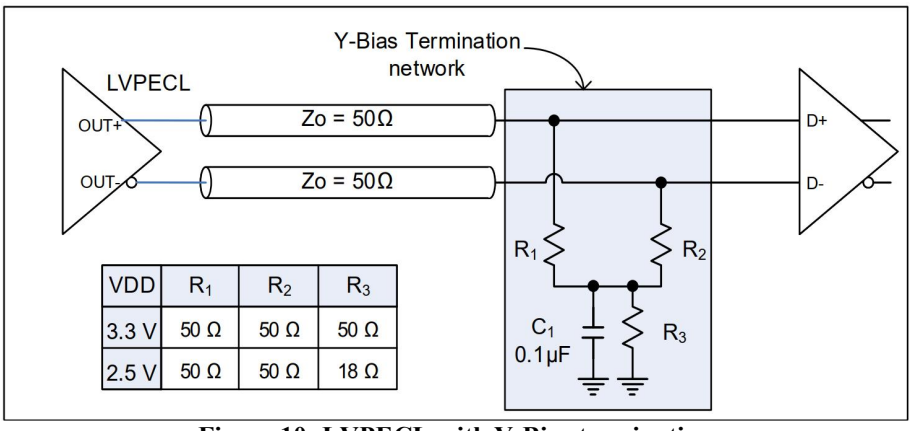


Figure 10: LVPECL with Y-Bias termination

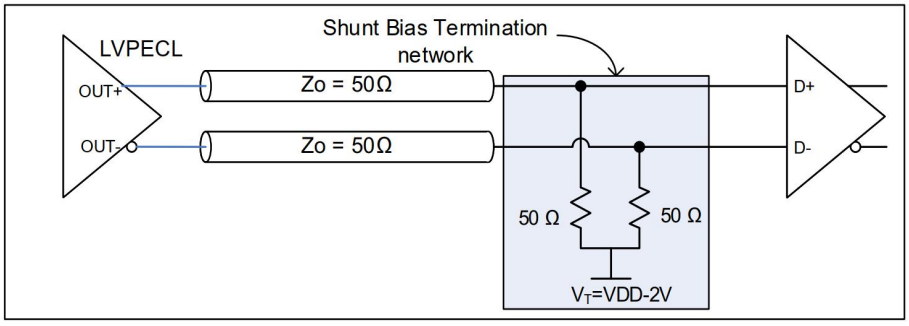


Figure 11: LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (Continued)

LVDS

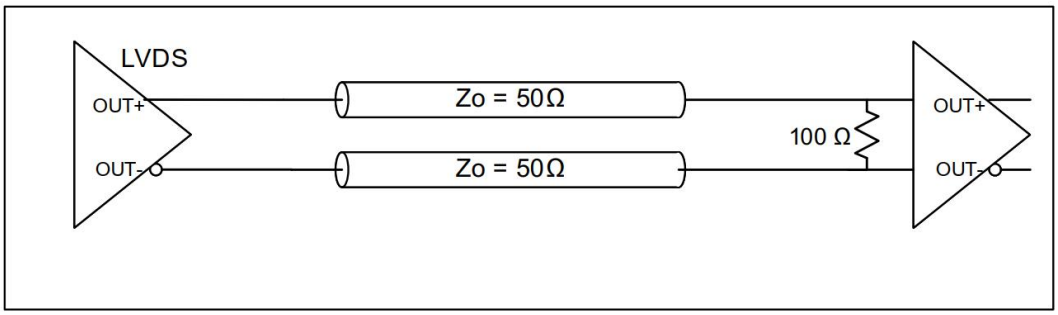


Figure 12: LVDS single DC termination at the load

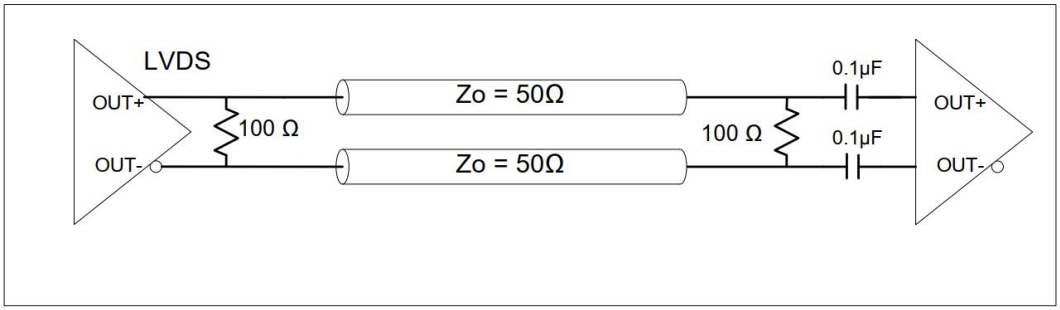


Figure 13: LVDS double AC termination with capacitor close to the load

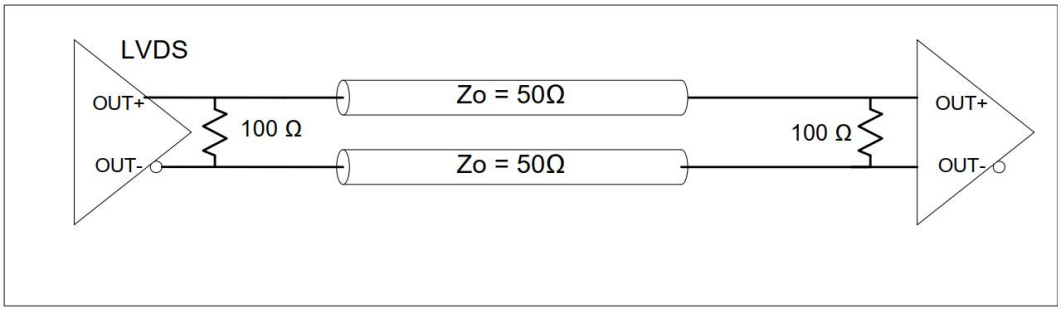
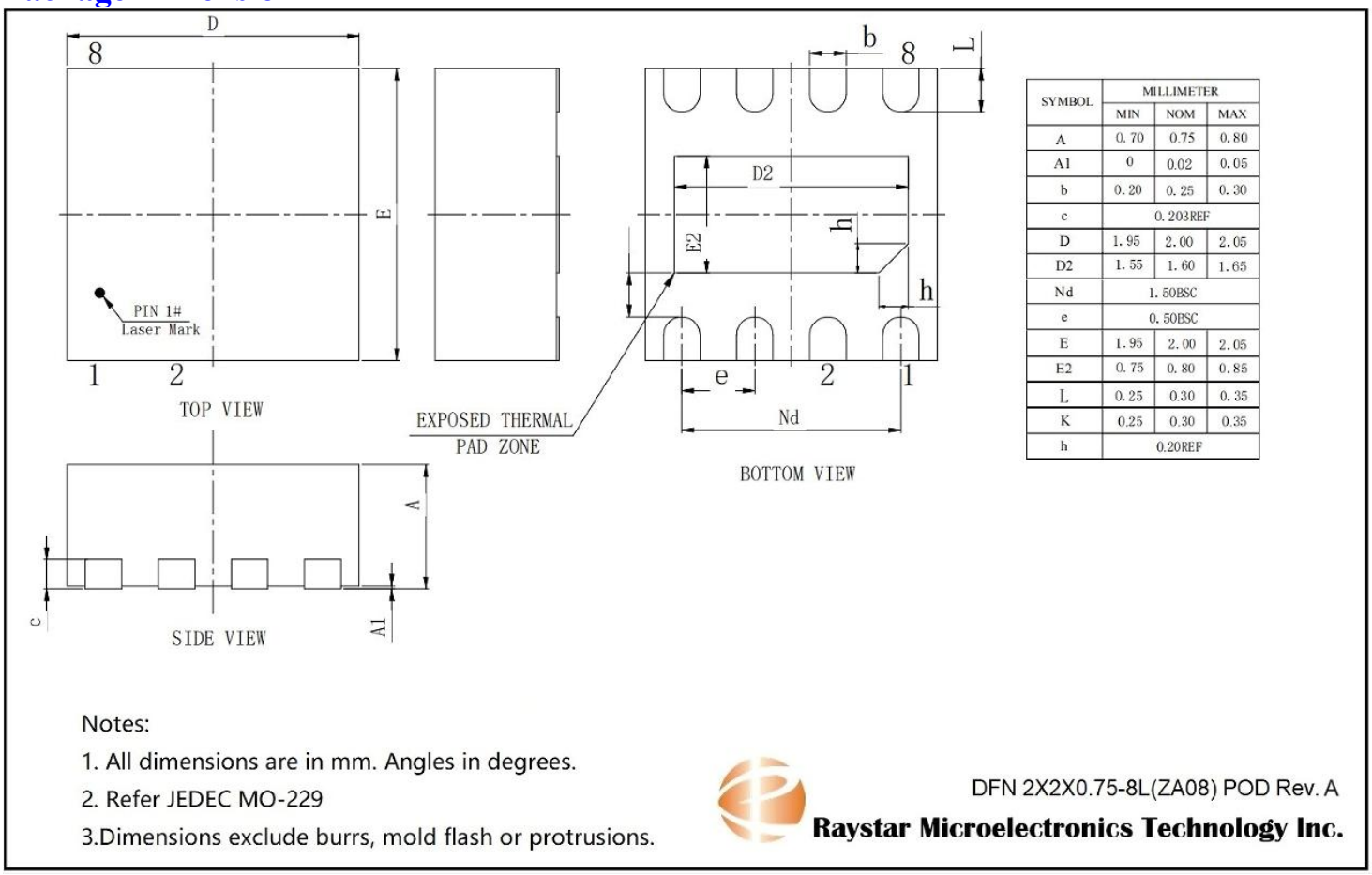


Figure 14: LVDS double DC termination

Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	1.95	2.00	2.05
D2	1.55	1.60	1.65
Nd	1.50BSC		
e	0.50BSC		
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
L	0.25	0.30	0.35
K	0.25	0.30	0.35
h	0.20REF		

Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-229
3.Dimensions exclude burrs, mold flash or protrusions.

DFN 2X2X0.75-8L(ZA08) POD Rev. A
Raystar Microelectronics Technology Inc.

Ordering Information

RS1XO5090ZAE -100M

Frequency:
Ex:100M

Ordering Code	Package	Description
RS1XO5090ZAE	TDFN-8L	2 x 2 x 0.75 mm,0.5mm Pitch

Revision History

Revision	Description	Date
1.0	1. Official release	2025/3/24