Features

- No Direction-Control Signal Needed
- Maximum Data Rates
  - 110 Mbps (Push Pull)
  - 1.2 Mbps (Open Drain)
- 1.1 V to 1.95 V on A Port and 1.65 V to 5.5 V on B Port (VCCA ≤ VCCB)
- No Power-Supply Sequencing Required – Either VCCA or VCCB Can Be Ramped First
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection
  - 8000 V Human Body Model
  - 1000 V Charged-Device Model

Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

Description

This device is a 8-bit non-inverting level translator which uses two separate configurable power-supply rails. The A port tracks the VCCA pin supply voltage. The VCCA pin accepts any supply voltage between1.1 V and 1.95 V. The B port tracks the VCCB pin supply voltage. The VCCB pin accepts any supply voltage between 1.65 V and 5.5 V. Two input supply pins allows for low Voltage bidirectional translation between any of the 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state.

To ensure the Hi-Z state during power-up or power-down periods, tie OE to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Information

Part Number	Package	Description
RS7LS108LE	TSSOP-20	6.5 mm × 6.4 mm
RS7LS108ZCE	QFN-20	3.5 mm × 4.5 mm

Notes: E = Pb-free and Green

Block Diagram

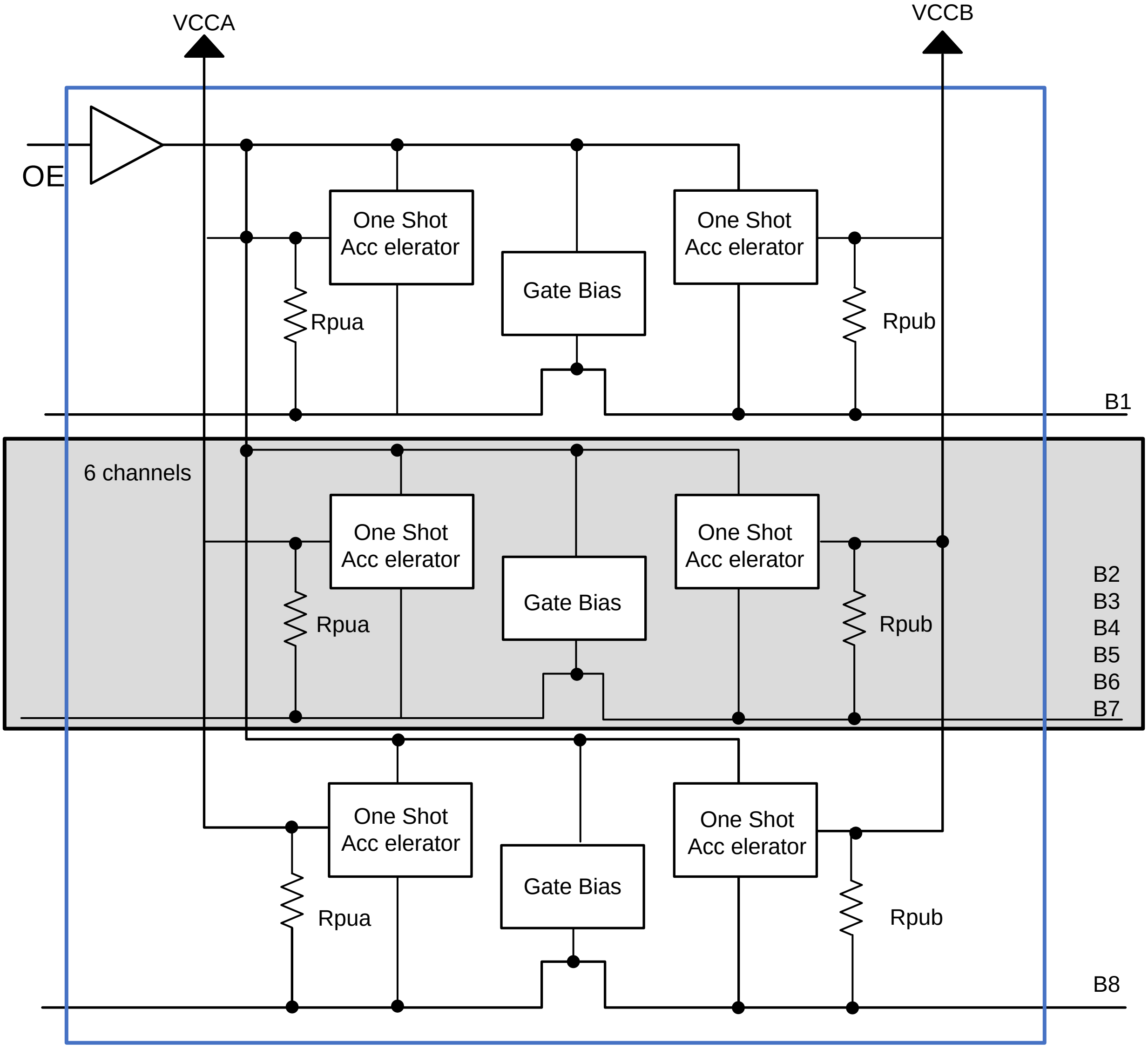
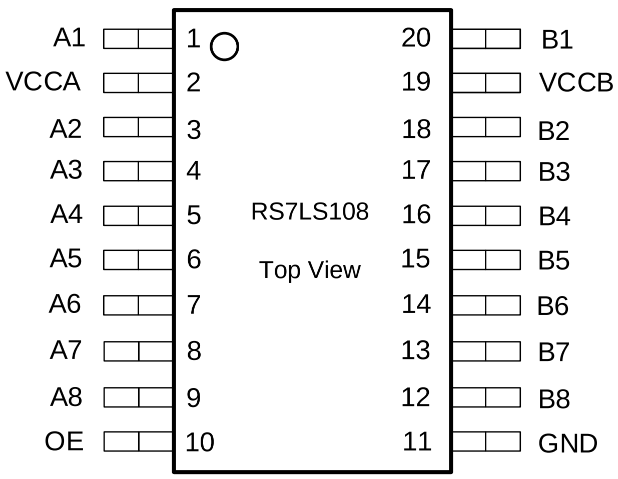


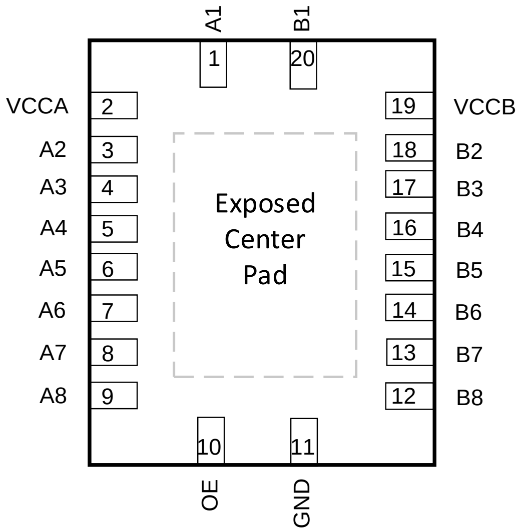
Figure 1. RS7LS108 block diagram

Pin Configuration

TSSOP-20



QFN-20



Pin Name	TSSOP-20	QFN-20	Type	Description
A1	1	1	I/O	Input/output 1. Referenced to VCCA
A2	3	3	I/O	Input/output 2. Referenced to VCCA
A3	4	4	I/O	Input/output 3. Referenced to VCCA
A4	5	5	I/O	Input/output 4. Referenced to VCCA
A5	6	6	I/O	Input/output 5. Referenced to VCCA
A6	7	7	I/O	Input/output 6. Referenced to VCCA
A7	8	8	I/O	Input/output 7. Referenced to VCCA
A8	9	9	I/O	Input/output 8. Referenced to VCCA
B1	20	20	I/O	Input/output 1. Referenced to VCCB
B2	18	18	I/O	Input/output 2. Referenced to VCCB
B3	17	17	I/O	Input/output 3. Referenced to VCCB
B4	16	16	I/O	Input/output 4. Referenced to VCCB
B5	15	15	I/O	Input/output 5. Referenced to VCCB
B6	14	14	I/O	Input/output 6. Referenced to VCCB
B7	13	13	I/O	Input/output 7. Referenced to VCCB
B8	12	12	I/O	Input/output 8. Referenced to VCCB
GND	11	11	—	Ground
OE	10	10	Input	Tri-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to VCCA.
VCCA	2	2	Power	A-port supply voltage. 1.1 V ≤ VCCA ≤ 1.95 V, VCCA ≤ VCCB.
VCCB	19	19	Power	B-port supply voltage. 1.65 V ≤ VCCB ≤ 5.5 V.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	MAX	UNIT
Supply voltage, VCCA		–0.5	4.6	V
Supply voltage, VCCB		–0.5	6.5	V
Input voltage, VI	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high-impedance or power-off state, VO	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high or low state, VO	A port	–0.5	VCCA + 0.5	V
	B port	–0.5	VCCB + 0.5	V
Input clamp current, IIK	VI < 0	–50		mA
Output clamp current, IOK	VO < 0	–50		mA
Continuous output current, IO		–50	50	mA
Continuous current through VCCA, VCCB, or GND		–100	100	mA
Junction temperature, TJ		150		°C
Storage temperature, Tstg		–65	150	°C

Note：Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condtions is not implied.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter					MIN	MAX	UNIT
VCCA	Supply voltage				1.1	1.95	V
VCCB	Supply voltage				1.65	5.5	V
VIH	High-level input voltage	A-Port I/Os	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	VCCI – 0.2	VCCI	V
		B-Port I/Os	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	VCCI – 0.4	VCCI	V
		OE	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	VCCA × 0.65	5.5	V
VIL	Low-level input voltage	A-Port I/Os	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	0	0.15	V
		B-Port I/Os	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	0	0.15	V
		OE	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	0	VCCA × 0.35	V
Δt/Δv	Input transition rise or fall rate	A-Port I/Os Push-pull	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	10		ns/V
		B-Port I/Os Push-pull	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	10		ns/V
		Control input	VCCA (V) = 1.1 to 1.95	VCCB (V) = 1.65 to 5.5	10		ns/V
TA	Operating free-air temperature				–40	125	°C

Electrical Characteristics:

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCCA (V)	VCCB (V)	TA = 25°C MIN	TYP	MAX	UNIT
VOHA	Port A output high voltage	IOH = –20 μA VIB ≥ VCCB – 0.4 V	1.1	1.65 to 5.5	VCCA × 0.67			V
VOLA	Port A output low voltage	IOL = 180 μA, VIB ≤ 0.15 V	1.1	1.65 to 5.5			0.4	
		IOL = 220 μA, VIB ≤ 0.15 V	1.65	1.65 to 5.5			0.4	
		IOL = 300 μA, VIB ≤ 0.15 V	1.95	1.65 to 5.5			0.4	V
VOHB	Port B output high voltage	IOH = –20 μA, VIA ≥ VCCA – 0.2 V	1.1	1.65 to 5.5	VCCB × 0.67			V
VOLB	Port B output low voltage	IOL = 220 μA, VIA ≤ 0.15 V	1.1 to 1.95	1.65			0.4	
		IOL = 300 μA, VIA ≤ 0.15 V	1.1 to 1.95	2.3			0.4	
		IOL = 400 μA, VIA ≤ 0.15 V	1.1 to 1.95	3			0.55	V
		IOL = 620 μA, VIA ≤ 0.15 V	1.1 to 1.95	4.5			0.55	
Ii	Input leakage current	OE: VI = VCCI or GND	1.1	1.65 to 5.5			±1	μA
IOZ	High-impedance state output current	A or B port	1.1	1.65 to 5.5			±1	μA
ICCA	VCCA supply current	VI = VO = Open, IO = 0	1.1	1.65 to 5.5		1		
			1.2 to 1.95	2.3 to 5.5		1		
			1.95	0			1	μA
			0	5.5			–1	
ICCB	VCCB supply current	VI = VO = Open, IO = 0	1.1	1.65 to 5.5		2		
			1.2 to 1.95	2.3 to 5.5		2		
			1.95	0			–1	μA
			0	5.5			1	
ICCA + ICCB	Combined supply current	VI = VCCI or GND, IO = 0	1.1	2.3 to 5.5		3		μA
			1.2 to 1.95	2.3 to 5.5		3		
ICCZA	High-impedance state VCCA supply current	VI = VO = Open, IO = 0, OE = GND	1.1	1.65 to 5.5		0.05		μA
ICCZB	High-impedance state VCCB supply current	VI = VO = Open, IO = 0, OE = GND	1.1	1.65 to 5.5		4		μA

VCCI is the VCC associated with the data input port.
VCCO is the VCC associated with the output port.
VCCA must be less than or equal to VCCB, and VCCA must not exceed 1.95V.

AC Electrical characteristics

VCCA = 1.2 V，over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		VCCB = 1.8 V		VCCB = 2.5 V		VCCB = 3.3 V		VCCB = 5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPHL	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving		11		9.2		8.6		8.6	ns
			Open-drain driving	4	14.4	3.6	12.8	3.5	12.2	3.5	12	
tPLH	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		12		10		9.8		9.7	
			Open-drain driving	182	720	143	554	114	473	81	384	
tPHL	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		12.7		11.1		11		12	ns
			Open-drain driving	3.4	13.2	3.1	9.6	2.8	8.5	2.5	7.5	
tPLH	Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		9.5		6.2		5.1		1.6	
			Open-drain driving	186	745	147	603	118	519	84	407	
ten	Enable time	OE-to-A or B	Push-pull driving	100		100		100		100		
tdis	Disable time	OE-to-A or B	Push-pull driving		400		400		400		400	
trA	Input rise time	A-port rise time	Push-pull driving	3.5	13.1	3	9.8	3.1	9	3.2	8.3	ns
			Open-drain driving	147	982	115	716	92	592	66	481	
trB	Input rise time	B-port rise time	Push-pull driving	2.9	11.4	1.9	7.4	0.9	4.7	0.7	2.6	ns
			Open-drain driving	135	1020	91	756	58	653	20	370	
tfA	Input fall time	A-port fall time	Push-pull driving	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	
			Open-drain driving	2.4	10	2.1	7.9	1.7	7	1.5	6.2	
tfB	Input fall time	B-port fall time	Push-pull driving	2	8.7	1.3	5.5	0.9	3.8	0.8	3.1	ns
			Open-drain driving	1.2	11.5	1.3	8.6	1	9.6	0.5	7.7	
tSK(O)	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns
Maximum data rate		A or B	Push-pull driving	40		60		60		60		Mbps
			Open-drain driving	0.8		0.8		1		1		

VCCA = 1.5 V

over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		VCCB = 1.8 V		VCCB = 2.5 V		VCCB = 3.3 V		VCCB = 5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPHL	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving		8.2		6.4		5.7		5.6	ns
			Open-drain driving	3.6	11.4	3.2	9.9	3.1	9.3	3.1	8.9	
tPLH	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		9		2.1		6.5		6.3	ns
			Open-drain driving	194	729	155	584	126	466	90	346	
tPHL	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		9.8		8		7.4		7	ns
			Open-drain driving	3.4	12.1	2.8	8.5	2.5	7.3	2.1	6.2	
tPLH	Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		10.2		7		5.8		5	ns
			Open-drain driving	197	733	159	578	129	459	93	323	
ten	Enable time	OE-to-A or B	Push-pull driving	100		100		100		100		ns
tdis	Disable time	OE-to-A or B	Push-pull driving		410		410		410		410	ns
trA	Input rise time	A-port rise time	Push-pull driving	3.1	11.9	2.6	8.6	2.7	7.8	2.8	7.2	ns
			Open-drain driving	155	996	124	691	100	508	72	350	
trB	Input rise time	B-port rise time	Push-pull driving	2.8	10.5	1.8	7.2	1.2	5.2	0.7	2.7	ns
			Open-drain driving	132	1001	106	677	73	546	32	323	
tfA	Input fall time	A-port fall time	Push-pull driving	2.1	8.8	1.6	6.6	1.4	5.7	1.4	4.9	ns
			Open-drain driving	2.2	9	1.7	6.7	1.4	5.8	1.2	5.2	
tfB	Input fall time	B-port fall time	Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	ns
			Open-drain driving	0.8	10.5	0.7	10.7	1	9.6	0.6	7.8	
tSK(O)	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns
Maximum data rate		A or B	Push-pull driving	45		65		70		70		Mbps
			Open-drain driving	0.8		0.8		0.8		1		

VCCA = 1.8 V

over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		VCCB = 1.8 V		VCCB = 2.5 V		VCCB = 3.3 V		VCCB = 5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPHL	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving		8.2		6.4		5.7		5.6	ns
			Open-drain driving	3.6	11.4	3.2	9.9	3.1	9.3	3.1	8.9	
tPLH	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		9		2.1		6.5		6.3	ns
			Open-drain driving	194	729	155	584	126	466	90	346	
tPHL	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		9.8		8		7.4		7	ns
			Open-drain driving	3.4	12.1	2.8	8.5	2.5	7.3	2.1	6.2	
tPLH	Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		10.2		7		5.8		5	ns
			Open-drain driving	197	733	159	578	129	459	93	323	
ten	Enable time	OE-to-A or B	Push-pull driving	100		100		100		100		ns
tdis	Disable time	OE-to-A or B	Push-pull driving		400		400		400		400	ns
trA	Input rise time	A-port rise time	Push-pull driving	3.1	11.9	2.6	8.6	2.7	7.8	2.8	7.2	ns
			Open-drain driving	155	996	124	691	100	508	72	350	
trB	Input rise time	B-port rise time	Push-pull driving	2.8	10.5	1.8	7.2	1.2	5.2	0.7	2.7	ns
			Open-drain driving	132	1001	106	677	73	546	32	323	
tfA	Input fall time	A-port fall time	Push-pull driving	2.1	8.8	1.6	6.6	1.4	5.7	1.4	4.9	ns
			Open-drain driving	2.2	9	1.7	6.7	1.4	5.8	1.2	5.2	
tfB	Input fall time	B-port fall time	Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	ns
			Open-drain driving	0.8	10.5	0.7	10.7	1	9.6	0.6	7.8	
tSK(O)	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns
Maximum data rate		A or B	Push-pull driving	45		65		70		70		Mbps
			Open-drain driving	0.8		0.8		0.8		1		

Parameter Measurement Information

Load Circuits

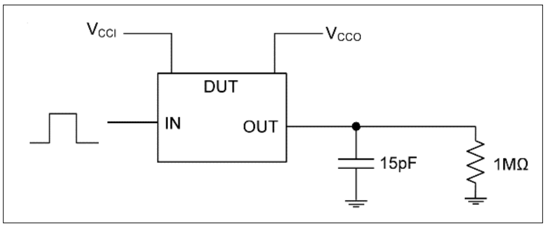


Figure 3 **Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver**

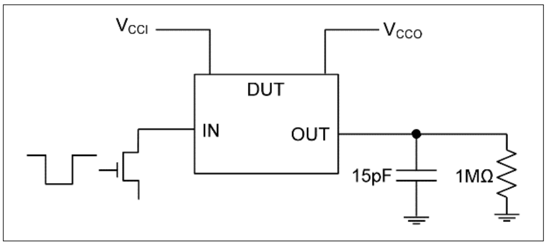
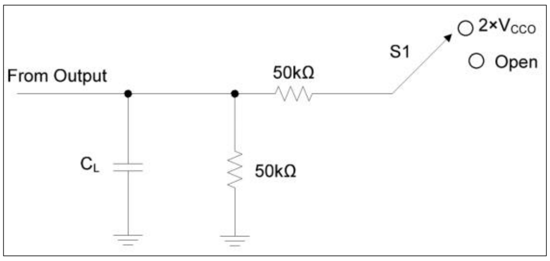


Figure 4 **Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver**



TEST	S1
tPZL / tPLZ	2 × VCCO
tPHZ / tPZH	Open

Figure 5 **Load Circuit for Enable-Time and Disable-Time Measurement**

Notes:

1. CL includes probe and jig capacitance.
2. ten is the same as tPZL and tPZH. tdis is the same as tPLZ and tPHZ.
3. VCCI is the supply voltage associated with the input.
4. VCCO is the supply voltage associated with the input.

Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤10 MHz
- Z_O = 50 Ω
- dv/dt ≥1 V/ns

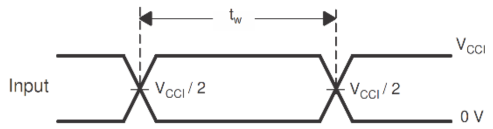


Figure 6 Pulse Duration

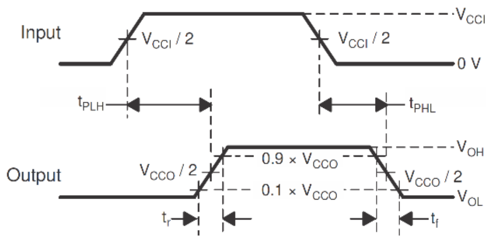
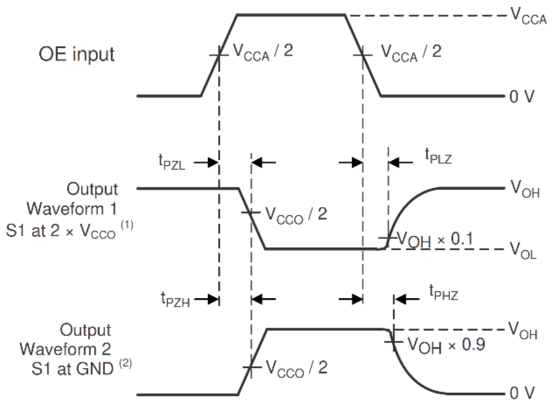


Figure 7 Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.

B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 8 Enable and Disable Times

Functional Description

Overview

The RS7LS108 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.1 V to 1.95 V. The B-port accepts I/O voltages from 1.65 V to 5.5 V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

Each A-port I/O has a pull-up resistor (RPUA) to VCCA and each B-port I/O has a pull-up resistor (RPUB) to VCCB. RPUA and RPUB have a value of 40 kΩ when the output is driving low. RPUA and RPUB have a value of 4 kΩ when the output is driving high. RPUA and RPUB are disabled when OE = Low.

Architecture

Figure 9 describes semi-buffered architecture design this application requires for both push-pull and open- drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300 Ω to 500 Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design needs no direction- control signal (to control the direction of data flow from A to B or from B to A). The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

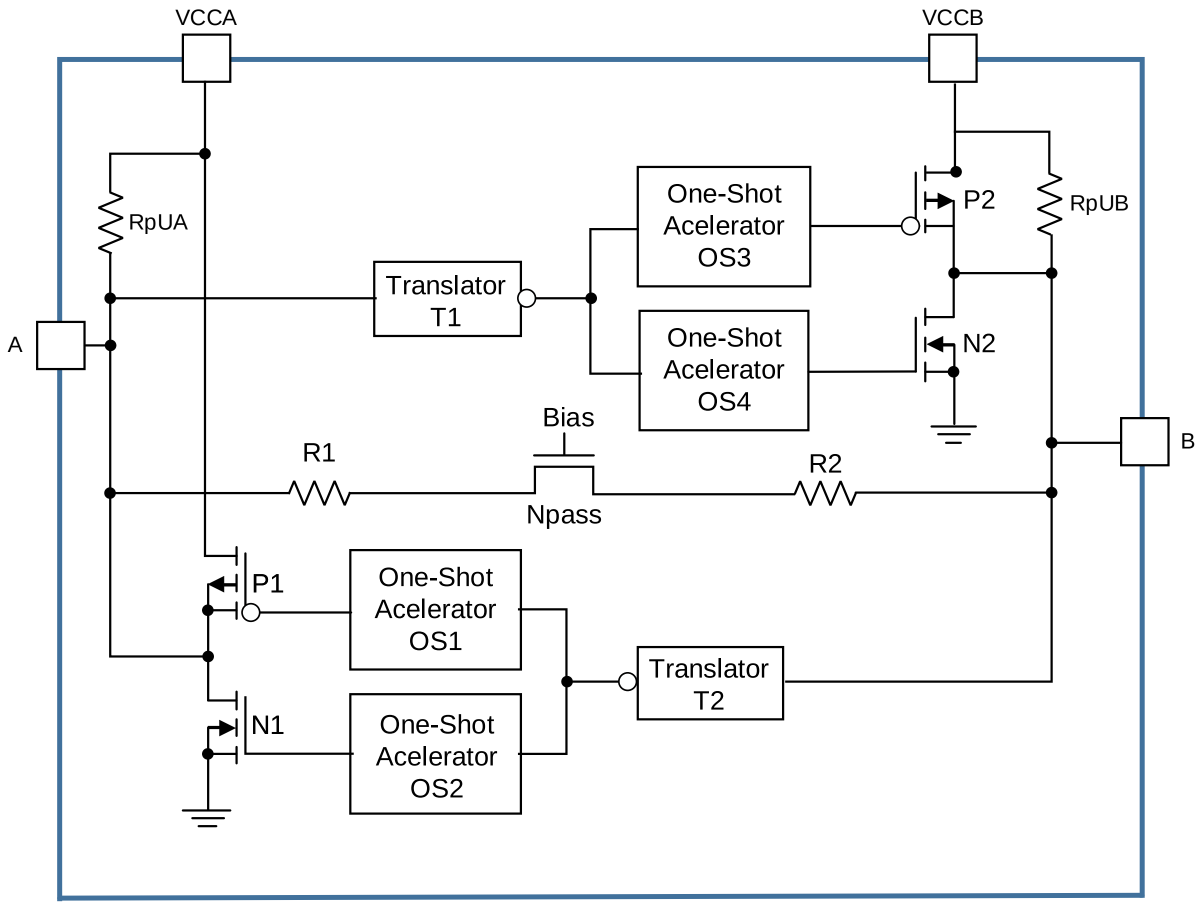


Figure 9. Architecture of a RS7LS108 Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and these speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

Input Driver Requirements

The continuous DC-current sinking capability is determined by the external system-level open-drain (or push- pull) drivers that are interfaced to the RS7LS108 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current sourcing capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time (tfA, tfB) of a signal depends on the edge-rate and output impedance of the external device driving RS7LS108 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the tPHL and maximum data rates also depend on the output impedance of the external driver. The values for tfA, tfB, tPHL, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

Output Load Considerations

Raystar recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the RS7LS108 output. Therefore, Raystar recommends that this lumped-load capacitance is considered in order to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Enable and Disable

The RS7LS108 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (tdis) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (ten) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

Pull-up or Pull-down Resistors on I/O Lines

The RS7LS108 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (RPUA) to VCCA and each B-port I/O has a pull-up resistor (RPUB) to VCCB. RPUA and RPUB have a value of 40 kΩ when the output is driving low. RPUA and RPUB have a value of 4 kΩ when the output is driving high. RPUA and RPUB are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower VOL values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

Device Functional Modes

The RS7LS108 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

Application Information

The RS7LS108 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device, (SCES650) 4-Bit Bidirectional Voltage-Level Translator might be a better option for such push-pull applications. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

Typical Application

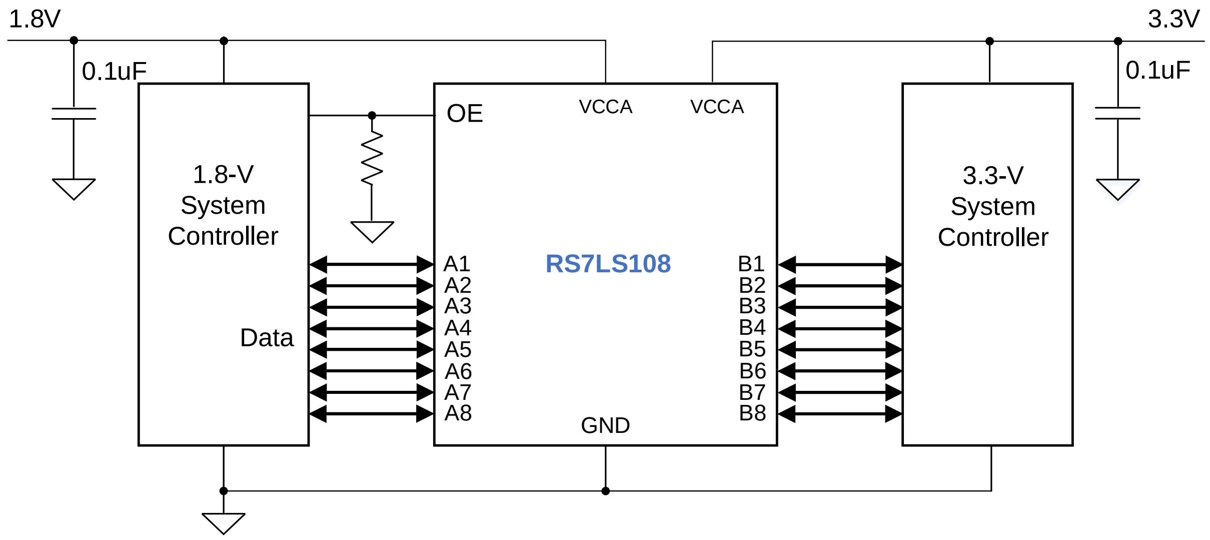


Figure 10 Typical Application Circuit

Design Requirements

To begin the design process, determine the following:

Use the supply voltage of the device that is driving the RS7LS108 device to determine the input and output voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.

The RS7LS108 device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary. An external pull-down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull-down resistor.

$$VOH = VCCx \times RPD / (RPD + 4\ k\Omega)$$

Power Supply Recommendations

During operation, ensure that VCCA ≤ VCCB at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by VCCA and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until VCCA and VCCB are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

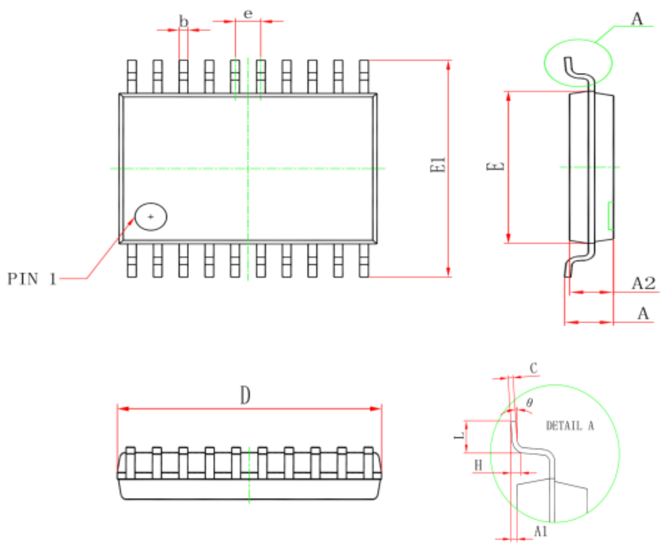
Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.

Short trace lengths should be used to avoid excessive loading.

PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

Package Information

TSSOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Note:
1. All dimensions are in mm. Angels in degrees.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MS-012

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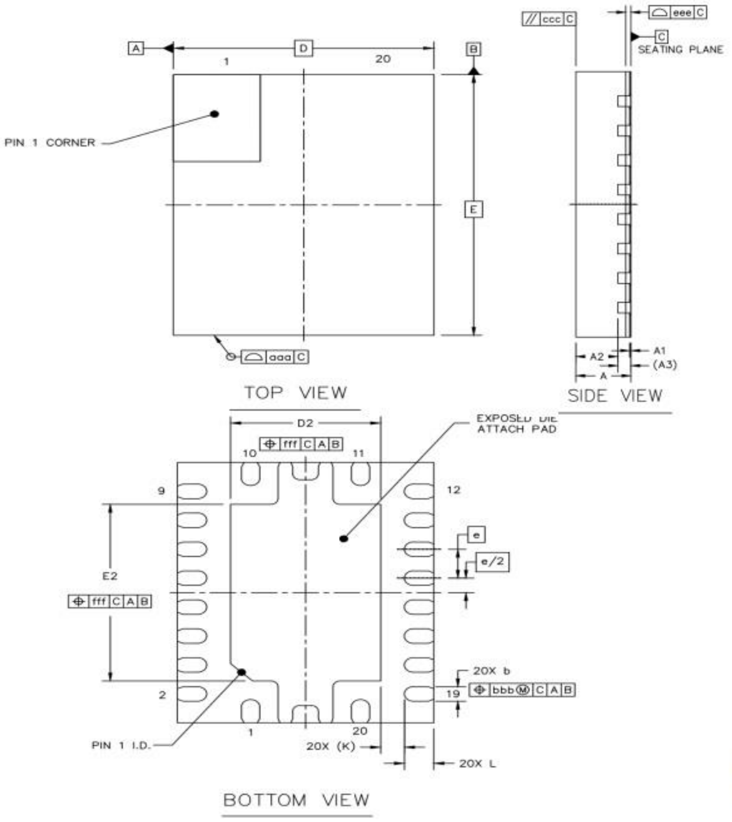
QFN-20



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.95	2.05	2.15
	Y	E2	2.95	3.05	3.15
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Note:
1. All dimensions are in mm.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MO-220

QFN 3.5×4.5-20L(ZC20) POD Rev.0

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Revision History

Revision	Description	DATE
1.0	Initial release	2024/11/6