Features

- PCIe Gen5 Phase Jitter < 80fs rms
- 3.3V operation voltage
- 85Ω differential Low-Power HCSL (LP-HCSL) outputs eliminate 52 resistors
- selectable SMBus addresses
- Supports 0%, -0.3% and -0.5% spread-spectrum amounts
- 6 x 6 mm TQFN-48L

Output Features

- 1 – 50MHz output pairs
- 6 – 100MHz output pairs
- 6 – MXCLK output pairs multiplexable between 100MHz and 50MHz
- Dedicated Platform Time Input clock

Application

- Cloud/High-performance Computing
- nVME Storage
- Networking
- PCIe switch

Description

The RS2CG2013 is a single-chip, PCIe Gen5 clock synthesizer. It is designed to work as a complete clock solution which matches PCIe Gen5 specification or in combination with DB2000QL-compliant clock buffers. It is part of the next generation clock generator family supporting the latest dual and multi-socket Intel server platforms.

PCIe Clocking Architecture

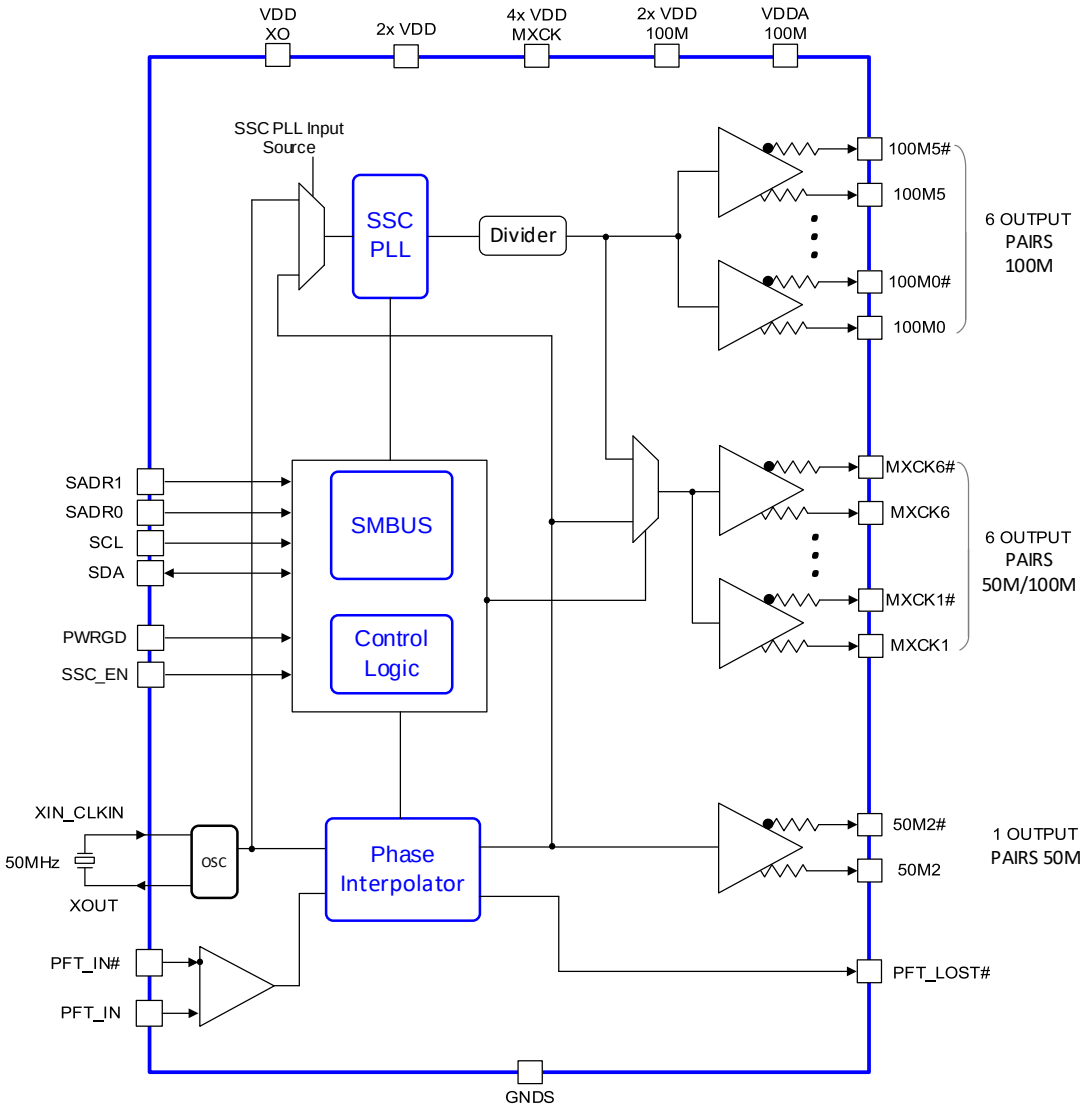
- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Ordering Information

Ordering Code	Package	Description
RS2CG2013ZLE	TQFN_48L	6 x 6 x 0.75 mm,0.4mm Pitch

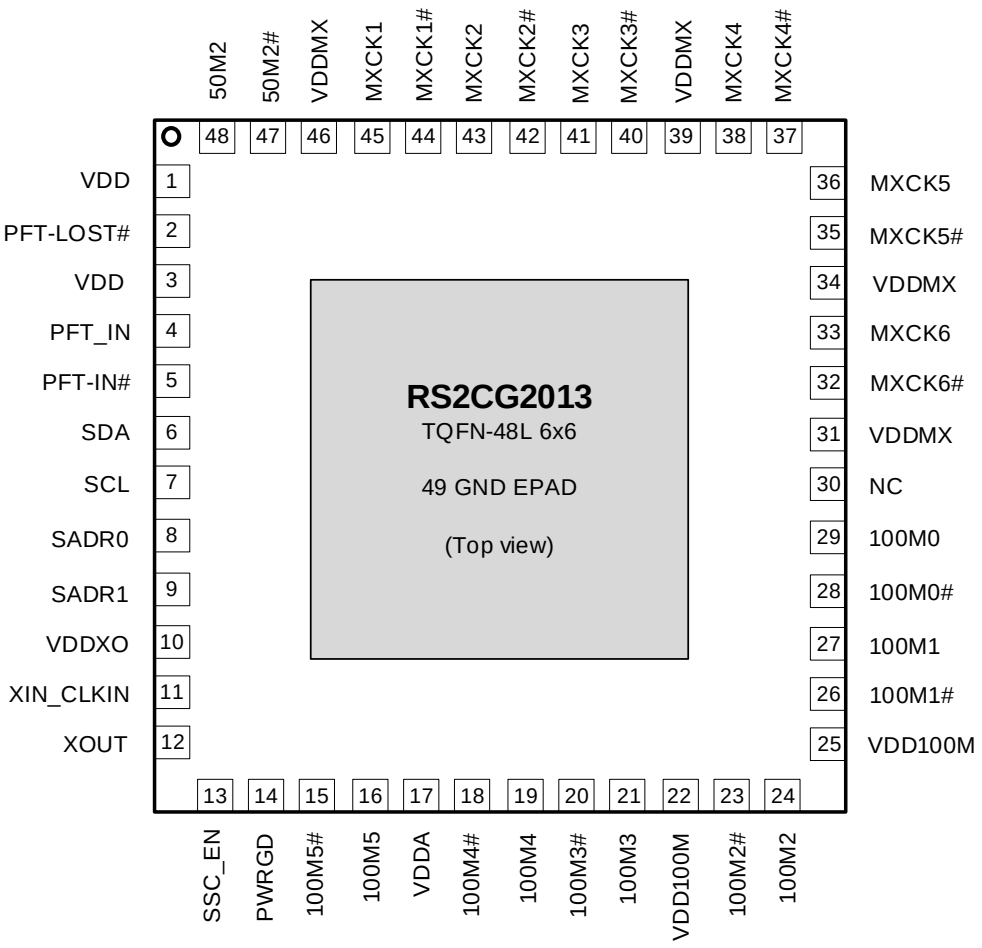
Notes:
[1] E = Pb-free and Green

Block Diagram

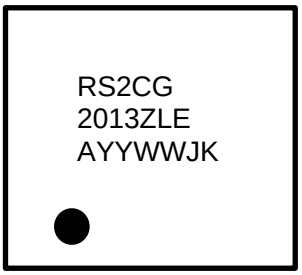


Pin Configuration

Figure 1. Pin Assignments for 6×6 mm TQFN-48L Package – Top View



Top Marking



RS2CG2013ZLE—Part Number
AYYWWJK—Production Tracing Code

Pin Description

Table 1. Pin Descriptions

Pin Name	Number	Type	Description
100M0	29	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
100M0#	28	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
100M1	27	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
100M1#	26	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
100M2	24	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
100M2#	23	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
100M3	21	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
100M3#	20	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
100M4	19	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
100M4#	18	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
100M5	16	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
100M5#	15	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
50M2	48	O, DIF	±0.7V LP-HCSL differential 50MHz true output.
50M2#	47	O, DIF	±0.7V LP-HCSL differential 50MHz complement output.
GND	49	GND	GND EPAD.
MXCK1	45	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
MXCK1#	44	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
MXCK2	43	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
MXCK2#	42	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
MXCK3	41	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
MXCK3#	40	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
MXCK4	38	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
MXCK4#	37	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
MXCK5	36	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
MXCK5#	35	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
MXCK6	33	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
MXCK6#	32	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
NC	30	—	No connection.
PFT_IN	4	I, DIF, PDT	±0.7V 50MHz differential platform time input.
PFT_IN#	5	I, DIF, PDT	±0.7V 50MHz differential platform time input.
PFT_LOST#	2	OD, SE	Asserts when PFT_IN, PFT_IN# clock is not present.
PWRGD	14	I, SE, PU	3.3V LVTTL input to power up or power down the device.
SADR0	8	I, SE, PD, PU	3.3V tri-level LVTTL input to select SMBus address. Refer to tri-level input threshold table.
SADR1	9	I, SE, PD, PU	3.3V tri-level LVTTL input to select SMBus address. Refer to tri-level input threshold table.
SDA	6	IO, OD, PDT	Open drain bi-directional SMBus data.
SCL	7	I, SE, PDT	SMBus slave clock input.
SSC_EN	13	I, SE, PD	Tri-level input to enable or disable spread spectrum. Refer to tri-level input threshold table. 0 = SSC off, MID = -0.3% max, and HIGH = -0.5% max.
VDD100M	22	Power	Power supply for 100M outputs.
VDD100M	25	Power	Power supply for 100M outputs.
VDDA	17	Power	Analog power supply for 100M outputs.
VDDMX	46	Power	Power supply for MXCK outputs.

Pin Name	Number	Type	Description
VDDMX	39	Power	Power supply for MXCK outputs.
VDDMX	34	Power	Power supply for MXCK outputs.
VDDMX	31	Power	Power supply for MXCK outputs.
VDD	1	Power	Power supply for 50M outputs and platform time circuit and digital.
VDD	3	Power	Power supply for 50M outputs and platform time circuit and digital.
VDDXO	10	Power	Power supply for internal crystal oscillator.
XIN_CLKIN	11	I, SE, PDT	Crystal input / Single-ended input.
XOUT	12	O, SE	Output of internal crystal oscillator. This pin should be left floating if CLK_IN function is being used.

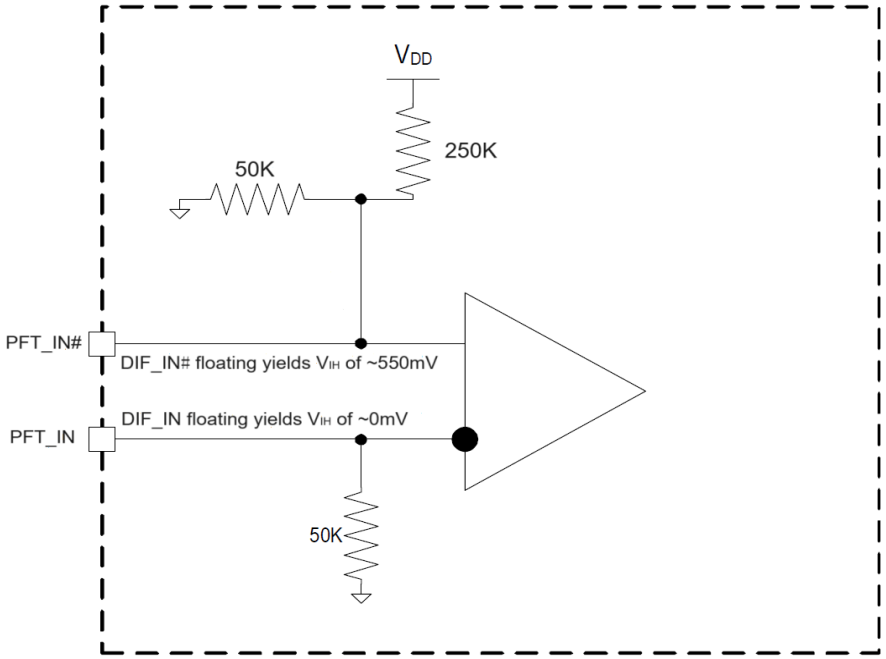
Table 2. Signal Types

Term	Description
I	Input
O	Output
OD	Open Drain Output
I/O	Bi-Directional
PD	Pull-down
PU	Pull-up
Z	Tristate
D	Driven
X	Don’t care
SE	Single-ended
DIF	Differential
Power	3.3V power
GND	Ground
PDT	Power Down Tolerant: These signals must tolerate being driven when the device is powered down.

Platform Time Input

The RS2CG2013 support a dedicated Platform Time Input clock. These pins receive clock from another clock device to keep synchronization across servers. PFT_IN allows different devices to frequency lock the 50 MHz clocks to a single time base. The local 50 MHz frequency locks to the PFT_IN clock if it is present. If PFT_IN is not present, the local 50MHz frequency is sourced from the local crystal.

Figure 2. PFT Bias Network



Output Enable Control

The outputs of RS2CG2013 is controlled by using the SMBus output enable bits. Any of the 13 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set that can enable or disable the clock outputs. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

Table 3. OE Functionality for 100M [5:0] Outputs

PWRGD	SMBus OE Bit	100M [5:0]
0	X	Disabled
1	0	Disabled
	1	Running

Note: Disabled in this table means both the true and complement output are low.

Table 4. OE Functionality for 50M [2] and MXCK [6:1] Outputs

PWRGD	SMBus OE Bit	MXCK [6:1]	50M [2]
0	X	Disabled	Disabled
1	0	Disabled	Disabled
	1	Running	Running

Note: Disabled in this table means both the true and complement output are low.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CG2013 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Supply Voltage	V_{DDX}				3.9	V	1
3.3V Input High Voltage	V_{IH}				3.9	V	2
3.3V Input Low Voltage	V_{IL}		-0.5			V	
Storage Temperature	T_S		-65		150	°C	
Junction Temperature	T_J	Maximum operating junction temperature.			125	°C	
Input ESD Protection	ESD	Human Body Model.	2000			V	

1. Operation over these conditions is neither implied nor guaranteed.
2. Maximum VIH is not to exceed maximum VDD.

Electrical Characteristics

TA = TAMB. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 6. AC Characteristics for SMBus

Parameter	Symbol	100K Class		Specification Limits 100K Class		400K Class		Specification Limits 400K Class		Units	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
SMBus Operating Frequency	f_{SMB}	10	100	10	100	10	400	10	400	kHz	
Bus Free Time between STOP and START Condition	t_{BUF}	4.7	—	4.7	—	1.3	—	1.3	—	µs	
Hold Time after (REPEATED) START Condition	$t_{HD:STA}$	4	—	4	—	0.6	—	0.6	—	µs	1
REPEATED START Condition Setup Time	$t_{SU:STA}$	4.7	—	4.7	—	0.6	—	0.6	—	µs	
STOP Condition Setup Time	$t_{SU:STO}$	4	—	4	—	0.6	—	0.6	—	µs	
Data Hold Time	$t_{HD:DAT}$	300	—	300	—	300	—	0	—	ns	2
Data Setup Time	$t_{SU:DAT}$	250	—	250	—	100	—	100	—	ns	
Detect SMBDAT Low Timeout	$t_{TIMEOUT}$	25	35	25	35	25	35	25	35	ms	3
Detect Clock Low Timeout	$t_{TIMEOUT}$	25	35	25	35	25	35	25	35	ms	4
Clock Low Period	t_{LOW}	4.7	—	4.7	—	1.3	—	1.3	—	µs	
Clock High Period	t_{HIGH}	4	50	4	50	0.6	50	0.6	50	µs	5
Clock/Data Fall Time	t_F	—	300	—	300	–	300	—	300	ns	6
Clock/Data Rise Time	t_R	—	1000	—	1000	–	300	—	300	ns	6
Time in which a device must be operational after power-on reset	t_{POR}		5		500		5		500	ms	7

[1] After this period, the first clock is generated.

[2] The RS2CG2013 device maintains 300ns data hold time for backwards compatibility with the SMBus 2.0 specification. Newer versions of the SMBus specification call out 0ns data hold time for both 100kHz and 400kHz classes.

[3] The RS2CG2013 provided additional SMBus protection by implementing a timeout for SDA being held low in excess of $t_{TIMEOUT}$, in addition to the SCLK low timeout.

[4] Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT}$, Minimum. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT}$, Maximum. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT}$, Maximum or longer.

[5] t_{HIGH}, Maximum provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than t_{HIGH}, Maximum.

[6] The rise and fall time measurement limits are defined as follows:
Rise Time Limits: (VIL, MAX - 0.15V) to (VIH,MIN + 0.15V)
Fall Time Limits: (VIH,MIN + 0.15 V) to (VIL,MAX - 0.15V)

[7] Power must be applied and PWRGD must be a 1 for the SMBus to be active.

Table 7. DC Characteristics for Input/Supply/Common

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Supply Voltage	V_{DDX}	3.3V ±5%.	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	No airflow.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, and tri-level inputs.	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, and tri-level inputs.	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-level inputs.	2.5		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Tri-level inputs.	1.2	$V_{DD}/2$	1.8	V	
Input Low Voltage	V_{IL}	Tri-level inputs.	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
	I_{INPUPD}	Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors. V_{IN} = V_{DD}; Inputs with internal pull-down resistors.	-50	±40	50	µA	
Internal Resistor Values	P_{UP}/P_{DN}	Value of internal pull-up and pull-down resistors, except PFT_IN/PFT_IN#.		120		kΩ	
	$P_{DN\_PFT\_IN/\#}$	Value of internal pull-down resistor on PFT_IN or PFT_IN#.		50		kΩ	
	$P_{UP\_PFT\_IN\#}$	Value of internal pull-up resistor to 0.55V on PFT_IN#.		250		kΩ	
Input Frequency	F_{IN}			50		MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.			4.5	pF	1
	C_{INDIF_IN}	Differential clock inputs.			2.7	pF	1
	C_{OUT}	Output pin capacitance.			4.5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or de-assertion of PWRDN# to			5	ms	1,2
Tdrive_PD#	t_{DRVPD}	Differential output enable after PWRDN# de-assertion.			300	µs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	2
Trise	t_R	Rise time of control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Refers to device differential input clock.

Table 9. Skew, Jitter and Duty Cycle

T_{AMB} = over the specified range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Specification Limit	Units	Notes
Output to Output Skew within a Group	$t_{SKEWGRP}$	Groups are 50M[2], MXCK[6:1], and 100M[5:0].		100		TBD	ps	1,2
Output to Output Skew Across Groups	$t_{SKEWGRP2GRP}$	Across 50M[2] and MXCK[6:1] set to 50MHz or 100M[5:0] and MXCK[6:1] set to 100MHz.		0.5		1	ns	1,2
Cycle to Cycle Jitter	t_{JCC50}	50MHz Outputs and MXCLK outputs set to 50MHz.		0.5		1	ns	1,2
	t_{JCC100}	100MHz Outputs and MXCLK outputs set to 100MHz.		25		1	ps	1,2
Duty Cycle	t_{DC100}	100MHz Outputs and MXCLK outputs set to 100MHz.	45	50	55	1	%	1,2
	t_{DC50}	50MHz Outputs and MXCLK outputs set to 50MHz with XTAL as source.	45	50	55	1	ps	1,2
	t_{DC50}	50MHz Outputs and MXCLK outputs set to 50MHz with XO as source with 44/55% duty cycle.	43	50	57	1	ps	1,2

[1] Measured into AC test load.

[2] Measured from differential cross-point to differential cross-point.

Table 10. PCIe Phase Jitter

TAMB = over the specified range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Limit	Units	Notes
PCIe Phase Jitter (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s)		20		86	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0 GT/s)		0.70		3	ps (RMS)	1,2
		PCIe Gen2 Lo Band (5.0 GT/s)		0.50		3.1	ps (RMS)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s)		0.20		1	ps (RMS)	1,2,3
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s)		0.20		0.4	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s)		0.04		0.08	ps (RMS)	1,2,3,5
PCIe Phase Jitter (SRIS Architecture)	$t_{jphPCIeG1-SRIS}$	PCIe Gen1 (2.5 GT/s)		10		N/A	ps (RMS)	1,2,6
	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (5.0 GT/s)		0.50			ps (RMS)	1,2,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (8.0 GT/s)		0.25			ps (RMS)	1,2,6
	$t_{jphPCIeG4-SRIS}$	PCIe Gen4 (16.0 GT/s)		0.26			ps (RMS)	1,2,6
	$t_{jphPCIeG5-SRIS}$	PCIe Gen5 (32.0 GT/s)		0.05			ps (RMS)	1,2,6

[1] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. Values for the Common Clock architecture are calculated with spread off and spread on at -0.5%. SRIS values are calculated for spread off and spread on at ≤ -0.3%. The worst case results for each data rate are summarized in this table. If oscilloscope data is used, equipment noise is removed from all results. See Test Load for PCIe Phase Jitter Measurements.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO)

with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. And additional consideration is the value for which to divide by √2. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by √2, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A “rule-of-thumb” SRIS limit would be either 0.5ps RMS/√2 = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/√2 = 0.5ps RMS if the clock chip is near the clock input.

Table 11. Differential Clock Outputs Driving High Impedance Receiver

TAMB = over the specified range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Specification Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on, fast setting.	2	3		2 – 4	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		0		20	%	1
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value. (scope averaging off).		800		1150	mV	1,7,8
Minimum Voltage	Vmin			0		-300 to +150		1,5,7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.		400		250 – 550	mV	1,6,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		0		140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] Includes 300mV of overshoot for Vmax and 300mV of undershoot for Vmin.

Table 12. Differential Clock Outputs Driving Terminated Receiver (Double Termination)

TAMB = over the specified range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Specification Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on, fast setting.	1	2		1 – 3	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		0	20	20	%	
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value. (scope averaging off).		400		330 – 575	mV	7,8
Minimum Voltage	Vmin			0		-150 – 75		1,5,7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.		200		125 – 275	mV	1,6,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		0		70	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±75mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±37mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] Includes 150mV of overshoot for Vmax and 150mV of undershoot for Vmin.

Table 13. Crystal Parameters

TA = TAMB. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Crystal Frequency	F_{IN}			50		MHz	
Shunt Capacitance	C_O				4	pF	
Load Capacitance	CL	Small range around CL only.		8		pF	1
Equivalent Series Resistance	ESR	ESR defined at frequency of oscillation.			50	Ω	
Drive Level	DL	Drive Level to the crystal.		100		μW	
Frequency Tolerance	$\triangle F/ F_{IN}$	All operating temperature range.			±20	PPM	2

[1] When driven by an external oscillator via the XIN_CLKIN pin, XOUT should be floating.

[2] These parameters depend on specific customer requirements and may differ from the values listed here.

Table 14. PFT_IN Clock Input Parameters

TA = TAMB. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Input Crossover Voltage	V_{CROSS}	Crossover voltage.	100		1000	mV	
Input Swing	V_{SWING}	Differential value.	200		2000	mV	
Input Slew Rate	dv/dt	Measured differentially.	0.7			V/ns	1
Input Leakage Current	I_{IN}	V_{IN} = 0.8V, V_{IN} = GND.	-10		16	µA	

[1] Slew rate measured through ±75mV window centered around differential zero.

Table 15. Current Consumption

TA = TAMB. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Operating Supply Current	I_{DDMXCK}	VDDMXCK, MXCK[6:1] at 100MHz.		70		mA	1
	I_{DD100M}	VDD100M, 100M[5:0].		55		mA	1
	I_{DDXO}	VDDXO, 50MHz XTAL.		25		mA	1
	I_{DD}	50M[2] on. PFT circuit active.		30		mA	1
		50M[2] on. PFT circuit not used (no PFT_IN)		28		mA	1
	$I_{DDA100M}$	VDDA100M, 100M[5:0] at 100M, SSC_EN =0		30		mA	1
Power Down Supply Current	I_{DDMXCK}			2.5		mA	2
	I_{DD100M}			2.5		mA	2
	I_{DDXO}			5		mA	2
	I_{DD}			15		mA	2
	$I_{DDA100M}$			0.5		mA	2

[1] PWRGD = 1, all outputs enabled.

[2] PWRGD = 0.

Table 16. Power Supply Noise Profile

TA = TAMB. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Power Supply Noise	V_{DD_AC}	Single tone AC noise, swept.		40		mV	1
	V_{DDA_AC}	V_{DD} electrical noise > 20MHz.		20		mV	1
	V_{DDXO}	V_{DD} electrical noise 12kHz to 25MHz.		TBD		mV	1

[1] Peak-to-peak values. The device meets all AC/DC parameters in the presence of at least this much noise.

Test Loads

Figure 10. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

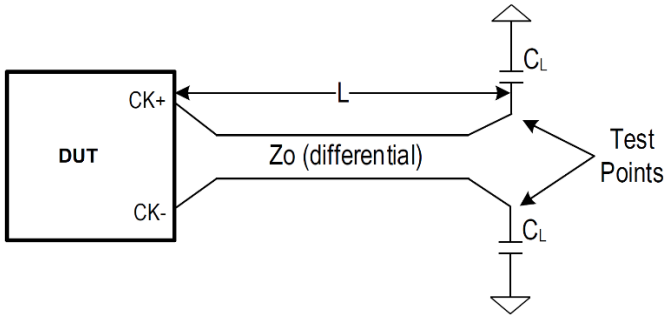


Table 17. Parameters for AC/DC Test Load

Rs (Ω)	Zo (Ω)	L (cm)	C_L (pF)
Internal	85	25.4	2

Figure 11. Test Load for PCIe Phase Jitter Measurements

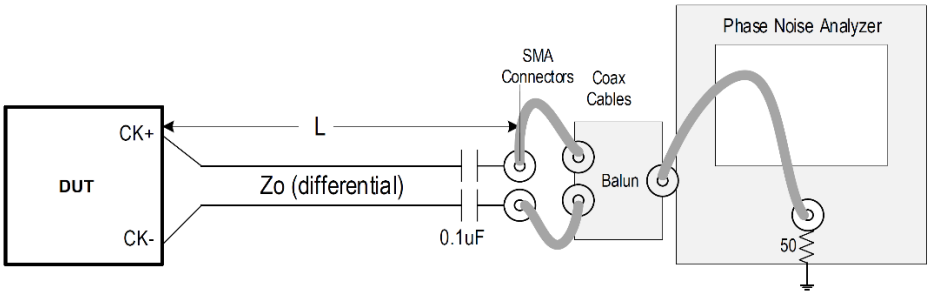


Table 18. Parameters for PCIe Gen5 Jitter Measurement

Rs (Ω)	Zo (Ω)	L (cm) *	C_L (pF)
Internal	85	25.4	N/A

* Note: PCIe Gen5 specifies L = 0cm. L = 25.4cm is more conservative.

SMBus Interface Information

Write Operation

- Controller (host) sends a start bit
- Controller (host) sends the write address
- RSM clock will acknowledge
- Controller (host) sends the beginning byte location = N
- RSM clock will acknowledge
- Controller (host) sends the byte count = X
- RSM clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- RSM clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

Write Operation			
Controller (Host)			**RSM (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stop bit		

Read Operation

- Controller (host) will send a start bit
- Controller (host) sends the write address
- RSM clock will acknowledge
- Controller (host) sends the beginning byte location = N
- RSM clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- RSM clock will acknowledge
- RSM clock will send the data byte count = X
- RSM clock sends Byte N+X-1
- RSM clock sends Byte 0 through Byte X (if X(H) was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Read Operation			
Controller (Host)			**RSM (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat start		
Slave Address			
RD	Read		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stop bit		

Table 19. SMBus Address Selection

SADR1	SADR0	SMBus Address
L	L	D2
L	M	D4
L	H	D6
M	L	B2
M	M	B4
M	H	B6
H	L	BA
H	M	BC
H	H	BE

Table 20. Byte 0: Output Enable Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Reserved (Should be write to 1b'0)					
6	Reserved (Should be write to 1b'0)					
5	Output Enable 100M5	Disabled	Enabled	RW	1	100M5
4	Output Enable 100M4	Disabled	Enabled	RW	1	100M4
3	Output Enable 100M3	Disabled	Enabled	RW	1	100M3
2	Output Enable 100M2	Disabled	Enabled	RW	1	100M2
1	Output Enable 100M1	Disabled	Enabled	RW	1	100M1
0	Output Enable 100M0	Disabled	Enabled	RW	1	100M0

Table 21. Byte 1: Output Enable Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Reserved (Should be write to 1b'0)					
6	Output Enable MXCK6	Disabled	Enabled	RW	1	MXCK6
5	Output Enable MXCK5	Disabled	Enabled	RW	1	MXCK5
4	Output Enable MXCK4	Disabled	Enabled	RW	1	MXCK4
3	Output Enable MXCK3	Disabled	Enabled	RW	1	MXCK3
2	Output Enable MXCK2	Disabled	Enabled	RW	1	MXCK2
1	Output Enable MXCK1	Disabled	Enabled	RW	1	MXCK1
0	Reserved (Should be write to 1b'0)					

Table 22. Byte 2: Output Enable Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	MXCK_SEL	100MHz	50MHz	R/W	0	MXCK [6:1]
6	MXCK_SEL Control (1)	Reserved	Register control	R/W	0	MXCK [6:1]
5	Reserved					
4	Reserved					
3	Reserved					
2	Output Enable 50M2	Disabled	Enabled	RW	1	50M2
1	Reserved					
0	Reserved					

Note:

The MXCK_SEL Control (bit 6) should be set to '1' then MXCK [6:1] outputs are controlled with MXCK_SEL bit (bit 7).

Table 23. Byte 3: PFT Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Realtime Readback of PFT_LOST#	PFT_LOST# low	PFT_LOST# high	R	Realtime	
6	Stop Delta Frequency Update (Byte 4 and 5)	Disabled	Enabled	R/W	0	Reserved
5	Clear Delta Frequency Registers (Byte 4 and 5)		All bits reset to 0	RW	0	Reserved
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	Reserved				0	Reserved
1	Reserved				0	Reserved
0	Reserved				0	Reserved

Note:

Prior to reading the delta frequency between PFT_IN and local 50MHz XO (Bytes 4 and 5), user should set bit 6 to prevent the case where one of the PFT Frequency Delta Registers is read before and the other after the internal update. The bit should be cleared after the read has been completed.

Table 24. Byte 4: PFT Frequency Delta Register 0 (Least Significant Byte)

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	PFT – 50 MHz XO bit 7			R	Realtime	
6	PFT – 50 MHz XO bit 6			R	Realtime	
5	PFT – 50 MHz XO bit 5			R	Realtime	
4	PFT – 50 MHz XO bit 4			R	Realtime	
3	PFT – 50 MHz XO bit 3			R	Realtime	
2	PFT – 50 MHz XO bit 2			R	Realtime	
1	PFT – 50 MHz XO bit 1			R	Realtime	
0	PFT – 50 MHz XO bit 0			R	Realtime	

Note:

These bits contain the least significant byte of average PPM difference between the PFT clock and the local 50MHz reference.

Table 25. Byte 5: PFT Frequency Delta Register 1 (Most Significant Byte)

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	PFT – Sign Bit	Positive Number	Negative Number	R	Realtime	
6	PFT – 50 MHz XO bit 14			R	Realtime	
5	PFT – 50 MHz XO bit 13			R	Realtime	
4	PFT – 50 MHz XO bit 12			R	Realtime	
3	PFT – 50 MHz XO bit 11			R	Realtime	
2	PFT – 50 MHz XO bit 10			R	Realtime	
1	PFT – 50 MHz XO bit 9			R	Realtime	
0	PFT – 50 MHz XO bit 8			R	Realtime	

Note:

These bits contain the most significant byte of average PPM difference between the PFT clock and the local 50MHz reference. The representation is 2's complement, signed magnitude with Byte 5 bit 7 being the sign bit.

Table 26. Byte 6: SSC PLL Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Reserved				Reserved	Reserved
6	Reserved				Reserved	Reserved
5	Readback of SSC_EN pin	Bit [1:0]: SSC State 00: SSC Off, 01: SSC = -0.3% 10: Reserved, 11: SSC = -0.5%		R	Realtime	100M[5:0] and MXCK[6:1] if MXCK_SEL= 0
4				R	Realtime	
3	SSC PLL Input Source	XTAL	Filter PLL	RW	0	
2	SSC Pin Control	Pin Control	Software Control	RW	0	
1	SSC Select	Bit [1:0]: SSC State 00: SSC Off, 01: SSC = -0.3% 10: Reserved, 11: SSC = -0.5%		RW	Latch SSC pin on power-up	
0				RW	Latch SSC pin on power-up	

Byte 7: Reserved

Table 27. Byte 8: Vendor/Revision Identification Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Revision Code Bit 3	0000 is 1st Silicon		R	0	
6	Revision Code Bit 2			R	0	
5	Revision Code Bit 1			R	0	
4	Revision Code Bit 0			R	0	
3	Vendor ID Bit 3	0001 is RSM		R	0	
2	Vendor ID Bit 2			R	0	
1	Vendor ID Bit 1			R	0	
0	Vendor ID Bit 0			R	1	

Table 28. Byte 9: Device ID Control Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Device ID 7 (MSB)	RS2CG2013 is 0h40		R	0	
6	Device ID 6			R	1	
5	Device ID 5			R	0	
4	Device ID 4			R	0	
3	Device ID 3			R	0	
2	Device ID 2			R	0	
1	Device ID 1			R	0	
0	Device ID 0			R	0	

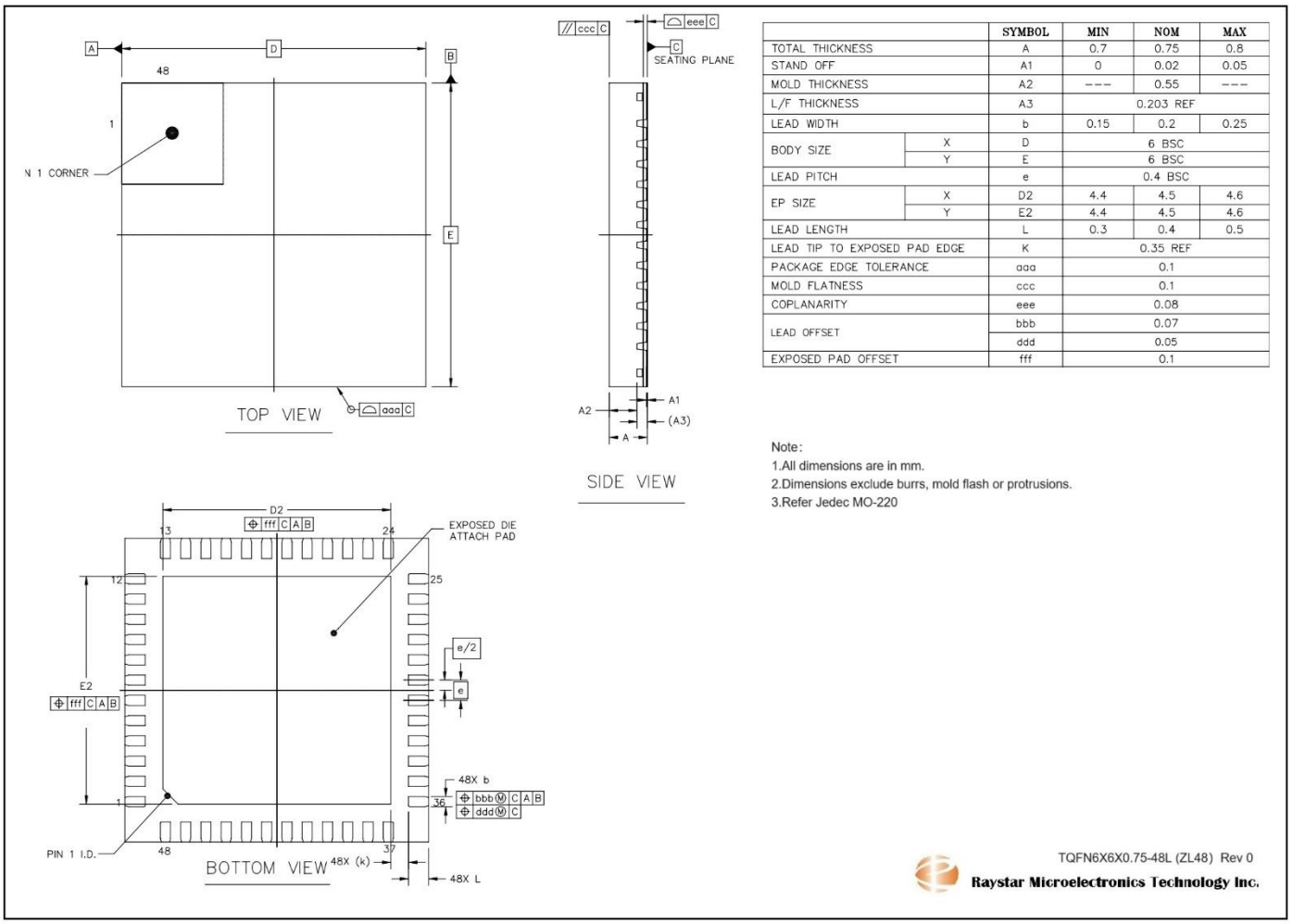
Table 29. Byte 10: Byte Count Register

Bit	Description	Bit = 0	Bit = 1	Type	Default	Output(s) Affected
7	Reserved				0	
6	Reserved				0	
5	BC5 - Writing to this register configures how many bytes will be read back			RW	0	
4	BC4 - Writing to this register configures how many bytes will be read back			RW	0	
3	BC3 - Writing to this register configures how many bytes will be read back			RW	1	
2	BC2 - Writing to this register configures how many bytes will be read back			RW	0	
1	BC1 - Writing to this register configures how many bytes will be read back			RW	0	
0	BC0 - Writing to this register configures how many bytes will be read back			RW	0	

Byte 11~Byte16: Reserved

Package Information

TQFN_48L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.4	4.5	4.6
	Y	E2	4.4	4.5	4.6
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TQFN6X6X0.75-48L (ZL48) Rev 0
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary release	2024/08/06
1.0	Initial release	2024/12/18