Features

- PCIe Gen5 additive phase jitter: 12fs RMS
- PCIe Gen6 additive phase jitter: 5fs RMS
- DB2000QL additive phase jitter: 15fs RMS
- 12kHz to 20MHz additive phase jitter: 33fs RMS at 156.25MHz
- Power Down Tolerant (PDT) inputs
- Flexible Startup Sequencing (FSS)
- Automatic Clock Parking (ACP) upon loss of CLKIN
- Selectable output slew rate via pin or SMBus
- 4-wire Side-Band Interface supports high-speed
- serial output enable and device daisy-chaining
- 9 selectable SMBus addresses
- SMBus write protection features
- Spread-spectrum tolerant
- 85Ω or 100Ω (-100 suffix) output impedance
- CLKIN accepts HCSL or LVDS signal levels
- -40 to +105°C, 3.3V ±10% 1.8V ±5% operation

Applications

- Cloud/High-performance Computing
- NVMe Storage
- Networking
- Accelerators

Description

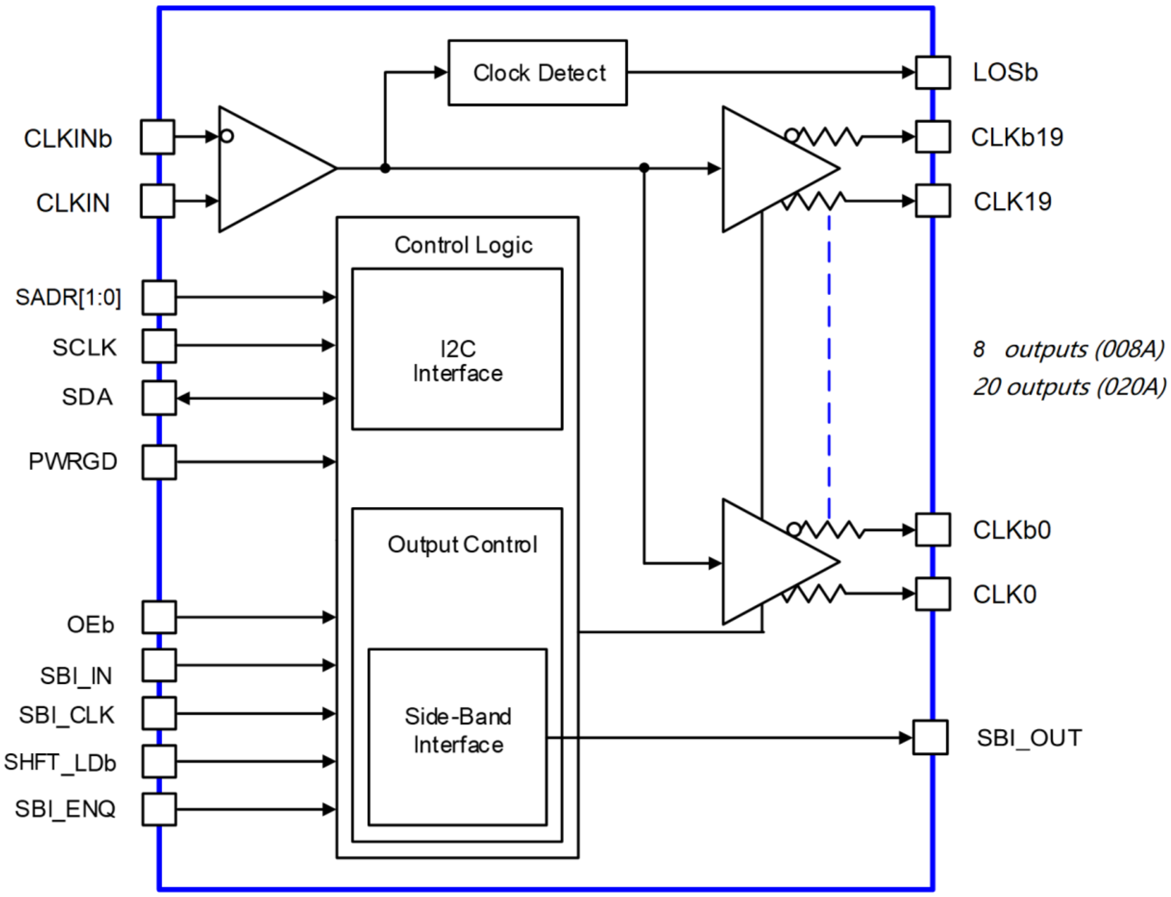
The RS2CB19008A ultra-high performance series fanout buffers support PCIe Gen5 and Gen6. They provide a Loss-Of-Signal (LOS) output for system monitoring and redundancy. The devices also incorporate Power Down Tolerant (PDT) and Flexible Startup Sequencing (FSS) features, easing system design. They can drive both source-terminated and double terminated loads, operating up to 400MHz.
The RS2CB19008A devices offer higher output counts in smaller packages compared to earlier buffer families.
The buffers support both Common Clock (CC) and Independent Reference (IR) PCIe clock architectures.

Ordering Information

Part Number	Number of Outputs	Differential Output Impedance (Ω)	Package	Operation Temperature
RS2CB19008AZLAE	8	85	TQFN-40L	-40 to +105°C
RS2CB19008A-100ZLAE	8	100		

1.1 RS2CB19008A Block Diagram

Figure 1. RS2CB19008A/020A Block Diagram



1.2 RS2CB19008A Pin Assignments

Figure 2. RS2CB19008A TQFN-40L (Top View)

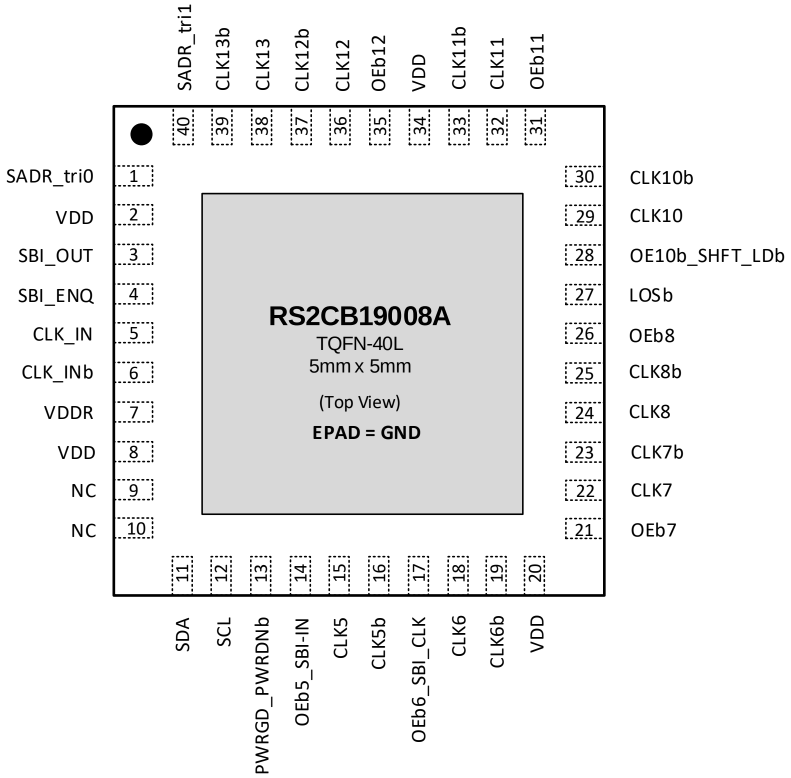


Table 1. RS2CB19008A Pin Descriptions

Pin Number	Pin Name	Type	Description
1	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables.
2	VDD	PWR	Clock power supply.
3	SBI_OUT	I, SE, PD	Tthe SBI shift register data output. The function is this pin is controlled by the SBI_ENQ. For more information, see Side-Band Interface (SBI).
4	SBI_ENQ	I, SE, PD, PDT	Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change. 0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins.
5	CLKIN	I, DIF	True clock input.
6	CLKINb	I, DIF	Complementary clock input.
7	VDDR	PWR	Power supply for clock input (receiver).
8	VDD	PWR	Clock power supply.
9	NC	PWR	Not connect
10	NC	PWR	Not connect
11	SDA	I/O, SE, OD	Data pin for SMBus interface.
12	SCL	I, SE	Clock pin of SMBus interface.
13	PWRGD_PWRDNb	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
14	OEb5_SBI_IN	I, SE, PD, PDT	Active low input for enabling output 5 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI). OE mode: 0 = Enable output, 1 = Disable output. Side-Band mode: Clocks data into the SBI on the rising edge.
15	CLK5	O, DIF	True clock output.
16	CLK5b	O, DIF	Complementary clock output.
17	OEb6_SBI_CLK	I, SE, PD, PDT	Active low input for enabling output 5 or the clock pin for the SBI shift register. The function is this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI). OE mode: 0 = Enable output, 1 = Disable output. Side-Band mode: Clocks data into the SBI on the rising edge.
18	CLK6	O, DIF	True clock output.
19	CLK6b	O, DIF	Complementary clock output.
20	VDD	PWR	Clock power supply.
21	OEb7	I, SE, PD, PDT	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output.

Pin Number	Pin Name	Type	Description
22	CLK7	O, DIF	True clock output.
23	CLK7b	O, DIF	Complementary clock output.
24	CLK8	O, DIF	True clock output.
25	CLK8b	O, DIF	Complementary clock output.
26	OEb8	I, SE, PD, PDT	Active low input for enabling output 6. 0 = Enable output, 1 = Disable output.
27	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open-drain output and requires an external pull-up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
28	OEb10_SHFT_LDb	I, SE, PD, PDT	Active low input for enabling output 13 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_ENQ pin. For more information, see Side-Band Interface (SBI). OE mode: 0 = Enable output, 1 = Disable output. Side-Band mode: 0 = Disable SBI shift register, 1 = Enable SBI shift register. A falling edge transfers SBI shift register contents to SBI output control register.
29	CLK10	O, DIF	True clock output.
30	CLK10b	O, DIF	Complementary clock output.
31	OEb11	I, SE, PD, PDT	Active low input for enabling output 11. 0 = Enable output, 1 = Disable output.
32	CLK11	O, DIF	True clock output.
33	CLK11b	O, DIF	Complementary clock output.
34	VDD	PWR	Clock power supply.
35	OEb12	I, SE, PD, PDT	Active low input for enabling output 12. 0 = Enable output, 1 = Disable output.
36	CLK12	O, DIF	True clock output.
37	CLK12b	O, DIF	Complementary clock output.
38	CLK13	O, DIF	True clock output.
39	CLK13b	O, DIF	Complementary clock output.
40	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables.
41	EPAD	GND	Ground pin.

2. Specifications

2.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin	-0.5	3.9	V
V_{IN}	Input Voltage	[1]	-0.5	3.9	V
V_{IN}	Input Voltage	[2]	-0.5	V_{DDx} + 0.3	V
I_{IN}	Input Current	All SE inputs and CLKIN [2]	-	±50	mA
I_{OUT}	Output Current – Continuous	CLK	-	30	mA
		SDATA, SBI_OUT	-	25	mA
	Output Current – Surge	CLK	-	60	mA
		SDATA, SBI_OUT	-	50	mA
T_J	Maximum Junction Temperature	-	-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C

1. Pins designated Power Down Tolerant (PDT) in the pin description tables.
2. Pins not designated Power Down Tolerant (PDT) in the pin description tables.

2.2 ESD Ratings

Symbol	Parameter	Condition	Rating	Unit
ESD	Human Body Model	ANSI/ESDA/JEDECJS-001-2023 Classification	8000	V
	Charged Device Model	ANSI/ESDA/TEDECJS-002-2022 Classification	1000	V

2.3 Recommended Operation Conditions

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	25	105	°C
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin, 3.3V ±10% supply.	2.97	3.3	3.63	V
		Any VDD pin, 1.8V ±5% supply.	1.71	1.8	1.89	V
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

2.4 Thermal Information

Package [1]	Symbol	Condition	Typical Value (°C/W)
5 × 5 mm TQFN-40L (3.4 × 3.4 mm ePad)	θ_{Jc}	Junction to Case	44
	θ_{Jb}	Junction to Base	2
	θ_{JA0}	Junction to Air, still air	33
	θ_{JA1}	Junction to Air, 1 m/s air flow	29
	θ_{JA3}	Junction to Air, 3 m/s air flow	28
	θ_{JA5}	Junction to Air, 5 m/s air flow	27

1. ePad soldered to board.

2.5 Electrical Characteristics

2.5.1 Phase Jitter

Table 2. PCIe Refclk Phase Jitter - Normal Conditions[1][2][3][8]

Symbol	Parameter	Condition	TYP	MAX	Specification Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5%	PCIe Gen1 (2.5 GT/s)	610	15000	86000 [6]	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	120	310	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	10	20	3,000 [6]	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	15	25	1,000 [6]	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [3] [4]	15	25	500 [6]	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [3] [5]	12	25	150 [6]	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [3] [5]	5	18	100 [6]	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC ≤ -0.3%	PCIe Gen2 (5.0 GT/s)	80	300	[7]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	50	150		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3] [4]	40	100		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3] [5]	15	30		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3] [5]	12	30		

1. The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 6.0, Revision 1.0*. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The *PCI Express Base Specification 6.0, Revision 1.0* provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.
8. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns

Table 3. PCIe Refclk Phase Jitter - Degraded Conditions[1][2][3][8]

Symbol	Parameter	Condition	TYP	MAX	Specification Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5%	PCIe Gen1 (2.5 GT/s)	692	839	86,000 [6]	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	41	49	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	11	14	3,000 [6]	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	20	24	1,000 [6]	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	20	24	500 [6]	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	8	9.3	150 [6]	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	5	6	100 [6]	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC ≤ -0.3%	PCIe Gen2 (5.0 GT/s)	52	63	[7]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	14	17		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	14	17		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	12	15		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	15	19		

1. The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 6.0, Revision 1.0*. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The *PCI Express Base Specification 6.0, Revision 1.0* provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 800mV and input slew rate = 1.5V/ns

Table 4. Non-PCIe Refclk Phase Jitter [1][2][3]

Symbol	Parameter	Condition	TYP	MAX	Specification Limit	Unit
tjphDB2000Q	Additive Phase Jitter - normal conditions[4]	100MHz, Intel-supplied filter [3]	10	12	80 [5]	fs RMS
tjph12k-20M		156.25MHz (12kHz to 20MHz)	30	36	N/A	
tjphDB2000Q	Additive Phase Jitter - degraded conditions [6]	100MHz, Intel-supplied filter [3]	13	16	80 [5]	
tjph12k-20M		156.25MHz (12kHz to 20MHz)	39	48	N/A	

1. See Test Loads for test configuration.
2. SMA100B used as signal source.
3. The RS2CB19008A devices meet all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
4. Differential input swing = 1,600mV and input slew rate = 3.5V/ns.
5. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
6. Differential input swing = 800mV and input slew rate = 1.5V/ns.

2.5.2 Output Frequencies, Startup Time, and LOS Timing

Table 5. Output Frequencies, Startup Time, and LOS Timing

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
f_{OP}	Operating Frequency	Automatic Clock Parking (ACP) Circuit disabled	1	-	400	MHz
		Automatic Clock Parking (ACP) Circuit enabled	25	-	400	
$t_{STARTUP}$	Start-up Time	[1]	-	1.2	3	ms
$t_{STARTUP}$	Start-up Time	[2]	-	0.3	1	ms
t_{LATOEb}	OEb latency	OEb assertion/de-assertion CLK start/stop latency. Input clock must be running.	4	5	10	clks
$t_{LOSAssert}$	LOS Assert Time	Time from disappearance of input clock to LOS assert. [3][4]	-	123	200	ns
$t_{LOSDeassert}$	LOS De-assert Time	Time from appearance of input clock to LOS de-assert. [3][5]	-	6	9	clks

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. PWRGD_PWRDNb tied to VDD in this case.
2. VDD stable, measured from de-assertion of PWRGD_PWRDNb.
3. The clock detect circuit does not qualify the accuracy of the input clock. The first input clock must appear to release the power on reset and enable the LOS circuit at power up.
4. PWRGD_PWRDNb high. The Automatic Clock Parking (ACP) circuit - if enabled - will park the outputs in a low/low state within this time. See Byte4, bit 4 LOSb_ACP_ENABLE.
5. PWRGD_PWRDNb high. The device will drive the outputs to a high/low state within this time and then begin clocking the outputs

2.5.3 RS2CB19008A CLK AC/DC Output Characteristics

Table 6. RS2CB19008A 85Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe [1]

Symbol	Parameter	Conditions	MIN	TYP	MAX	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1092	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-166	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	678	819	994	-	
V_{LOW}	Voltage Low [3]		-88	29	146	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 800mV, scope averaging off.	278	403	543	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		-	1	97	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging	2.0	2.8	4.0	2 to 5	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging	1.6	2.2	3.3	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3] [11]	V_{HIGH} set to 800mV. Fast slew rate.	-	4	19	20	%

		V_{HIGH} set to 800mV. Slow slew rate.	-	6	24	N/A	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	719	903	1090	-	mV
V_{LOW}	Voltage Low [3]		-115	37	163	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 900mV, scope averaging off.	289	445	582	250 to 600	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		-	1	105	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, Fast slew rate, scope averaging	2.1	2.9	4.3	2 to 5	V/ns
		V_{HIGH} set to 900mV, Slow slew rate, scope averaging	1.7	2.3	3.5	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Fast slew rate.	-	5	18	20	%
		V_{HIGH} set to 900mV. Slow slew rate.	-	6	26	N/A	
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential. 50% duty cycle input.	49	49.9	51	45 to 55	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 7. RS2CB19008A 100Ω CLK AC/DC Characteristics - Source-Terminated 100MHz PCIe Apps [1]

Symbol	Parameter	Condition	MIN	TYP	MAX	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1050	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-150	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	710	815	915	-	mV
V_{LOW}	Voltage Low [3]		-35	20	75	-	

V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 800mV, scope averaging off.	285	410	500	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		-25	35	105	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.	2.1	3	3.7	2 to 4	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.	1.6	2.6	3.4	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Fast slew rate.	-	4	16	20	%
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Slow slew rate.	-	3.5	15.5	20	%
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	802	907	1012	-	mV
V_{LOW}	Voltage Low [3]		-38	21	80	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 900mV, scope averaging off.	320	450	540	300 to 600	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		-35	40	115	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, Fast slew rate, scope averaging on.	2.1	3.0	3.9	2 to 4	V/ns
		V_{HIGH} set to 900mV, Slow slew rate, scope averaging on.	1.6	2.8	3.4	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Fast slew rate.	-	5	19.7	20	%
$T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Slow slew rate.	-	4.9	19.5	20	%
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	48	50	52	45 to 55	%

1. Standard high impedance load with C_L= 2pF. For more information, see Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant **x86** processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 8. RS2CB19008A 85Ω CLK AC/DC Characteristics - Non-PCIe, Source-Terminated Loads [1]

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VOH	Output High Voltage [2]	VHIGH = 800mV, Fast Slew Rate, 25MHz, 156.25MHz, 312.5MHz.	630	800	1003	mV
VOL	Output Low Voltage [2]		-150	15	160	
VCROSS	Crossing Voltage (abs) [3]		230	395	570	
ΔVCROSS	Crossing Voltage (var) [3][4][5]		-	50	140	
tR	Rise Time [2] VT = 20% to 80% of swing		135	480	780	ps
tF	Fall Time [2] VT = 20% to 80% of swing		155	425	748	ps
VOH	Output High Voltage [2]	VHIGH = 900mV, Fast Slew Rate, 25MHz, 156.25MHz, 312.5MHz.	700	890	1100	mV
VOL	Output Low Voltage [2]		-155	30	195	
VCROSS	Crossing Voltage (abs) [3]		260	430	640	
ΔVCROSS	Crossing Voltage (var) [3][4][5]		-	40	165	
tR	Rise Time [2] VT = 20% to 80% of swing		160	500	870	ps
tF	Fall Time [2] VT = 20% to 80% of swing		150	430	765	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, VT = 0V.	47	50	52	%

1. Standard high impedance load with CL = 2pF. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 9. RS2CB19008A 85Ω CLK AC/DC Characteristics - Non-PCIe, Double-Terminated Loads [1]

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 25MHz, 156.25MHz, 312.5MHz (amplitude is reduced by ~50% due to double termination).	370	430	475	mV
V_{OL}	Output Low Voltage [2]		-30	11	60	
V_{CROSS}	Crossing Voltage (abs) [3]		150	215	245	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	8	40	
t_R	Rise Time [2] V_T = 20% to 80% of swing		205	320	570	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		120	300	450	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz (amplitude is reduced by ~50% due to double termination).	385	490	555	mV
V_{OL}	Output Low Voltage [2]		-30	12	60	
V_{CROSS}	Crossing Voltage (abs) [3]		170	220	265	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	8	45	
t_R	Rise Time [2] V_T = 20% to 80% of swing		215	330	610	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		140	310	400	ps

t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	49	50	51	%

1. Both Tx and Rx are terminated (double-terminated) with CL = 2pF. This reduces amplitude by 50%. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.
7.

Table 10. RS2CB19008A 100Ω CLK AC/DC Characteristics - Non-PCIe Apps, Source-Terminated Loads [1]

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	700	795	910	mV
V_{OL}	Output Low Voltage [2]		-70	30	120	
V_{CROSS}	Crossing Voltage (abs) [3]		252	375	495	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		0	35	135	
t_R	Rise Time [2] VT = 20% to 80% of swing		205	320	590	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		145	315	585	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	750	885	1020	mV
V_{OL}	Output Low Voltage [2]		-80	20	145	
V_{CROSS}	Crossing Voltage (abs) [3]		260	400	545	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		0	45	145	
t_R	Rise Time [2] VT = 20% to 80% of swing		200	390	610	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		120	325	595	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48	50	52	%

1. Standard high impedance load with CL= 2pF. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 11. RS2CB19008A 100Ω CLK AC/DC Characteristics–Non-PCIe Apps, Double-Terminated Loads [1]

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{OH}	Output High Voltage [2]	VHIGH = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz)	360	395	430	mV
V_{OL}	Output Low Voltage [2]		-25	8	45	
V_{CROSS}	Crossing Voltage (abs) [3]		150	185	215	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-12	10	30	
t_R	Rise Time [2] VT = 20% to 80% of swing		150	310	557	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		110	260	380	ps
V_{OH}	Output High Voltage [2]	VHIGH = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	380	480	560	mV
V_{OL}	Output Low Voltage [2]		-30	10	50	
V_{CROSS}	Crossing Voltage (abs) [3]		165	220	280	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-18	10	30	
t_R	Rise Time [2] VT = 20% to 80% of swing		170	320	610	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		130	305	400	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, VT = 0V.	48	50	52	%

1. Both Tx and Rx are terminated (double-terminated) with C_L= 2pF. This reduces amplitude by 50%. For more information, see Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

2.5.4 CLKIN AC/DC Characteristics

Table 12. CLKIN AC/DC Characteristic

Symbol	Parameter	Condition	MIN [1]	TYP	MAX	Unit
V_{CROSS}	Input Crossover Voltage	-	100	-	1400	mV
V_{SWING}	Input Swing	Differential value.	200	-	-	mV
dv/dt	Input Slew Rate	Measured differentially. [2]	0.6	-	-	V/ns

1. For values required for performance, see the Phase Jitter tables.
2. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

2.5.5 Output-to-Output and Input-to-Output Skew

Table 13. RS2CB19008A Output-to-Output and Input-to-Output Skew [1]

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{SK}	Output-to-Output Skew [2]	Any two outputs, all outputs at fast slew rate.	-	38	50	ps
		Any two outputs, all outputs at slow slew rate.	-	40	60	ps
	Input-to-Output Delay	Clock in to any output, all outputs at fast slew rate.	1.1	1.2	1.4	ns

t_{PD}	Double-Terminated [3]	Clock in to any output, all outputs at slow slew rate.	1.2	1.4	1.6	ns
t_{PD}	Input-to-Output Delay Source-Terminated [3]	Clock in to any output, all outputs at fast slew rate.	1.2	1.4	1.6	ns
		Clock in to any output, all outputs at slow slew rate.	1.4	1.5	1.8	ns
Δt_{PD}	Input-to-Output Delay Variation [3]	A single device, over temperature *and voltage*.	-	1.4	2	ps/°C

1. For more information, see Test Loads.
2. This parameter is defined in accordance with JEDEC Standard 65.
3. Defined as the time between to output rising edge and the input rising edge that caused it.

2.5.6 I/O Signals

Table 14. I/O Electrical Characteristics

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{IH}	Input High Voltage [1][2]	Single-ended inputs, unless otherwise listed.	2	-	VDD + 0.3	V
V_{IL}	Input Low Voltage [1][2]		-0.3	-	0.8	V
V_{IH}	Input High Voltage	SADR_tri[1:0].	2.4	-	VDD+0.3	V
V_{IM}	Input Mid Voltage		1.2	-	1.8	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
V_{OH}	Output High Voltage [2]	SBI_OUT, IOH = -2mA	2.4	3.2	VDD + 0.3	V
V_{OL}	Output Low Voltage [2]	SBI_OUT, IOL = 2mA	-	0.1	0.4	V
I_{IH}	Input Leakage Current High, V_{IN} = VDD	CLKIN	-	-	87	µA
		CLKINb	-	-	87	
		Single-ended inputs, unless otherwise listed.	25	-	35	
		PWRGD_PWRDNb	-1	-	5	
		SADR_tri[1:0]	25	-	35	
I_{IL}	Input Leakage Current Low, V_{IN} = 0V	CLKIN	-12	-	-6	µA
		CLKINb	-3	-	3	
		Single-ended inputs, unless otherwise listed.	-3	-	3	
		PWRGD_PWRDNb	-35	-	-20	
		SADR_tri[1:0]	-35	-	-20	
Rp	PD_CLKIN	Value of internal pull-down resistor to ground (CLKIN)	-	53	-	kΩ
	PU_CLKINb	Value of internal pull-up resistor to 0.5V (CLKINb).	-	57	-	
	Pull-up/Pull-down Resistor	Single-ended inputs.	-	125	-	
Zo	Output Impedance	SBI_OUT pin.	-	50	-	Ω
		CLK outputs, RS2CB19008A (single-ended value).	-	41	-	Ω
		CLK outputs, RS2CB19008A -100 (single-ended value).	-	48	-	Ω

1. For SCLK and SDATA, see the SMBus Electrical Characteristics table.
2. These values are compliant with JESD8C.01.

2.5.7 Power Supply Current

Table 15. Power Supply Current

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
I_{DDCLK}	V_{DDCLK} Operating Current	85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. VDD=3.3V	-	80	88	mA
		85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.VDD=3.3V	-	93	103	
		85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.VDD=3.3V	-	105	115	
		85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.VDD=3.3V	-	122	130	
I_{DDCLK_PD}	V_{DDCLK} Power-down Current	PWRGD_PWRDNb = 0.VDD=3.3V		1	3	mA
I_{DDR}	V_{DDR} Operating Current	85Ω impedance, fast slew rate, at 100MHz. PWRGD_PWRDNb = 1.VDD=3.3V	-	29	35	mA
		85Ω impedance, fast slew rate, at maximum output frequency. PWRGD_PWRDNb = 1.VDD=3.3V	-	36	40	mA
I_{DDR_PD}	V_{DDR} Power-down Current	PWRGD_PWRDNb = 0 VDD=3.3V	-	3.8	5	mA
I_{DDCLK}	V_{DDCLK} Operating Current	85Ω impedance, fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1. VDD=1.8V	-	65	70	mA
		85Ω impedance, fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.VDD=1.8V	-	78	83	
		85Ω impedance, fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.VDD=1.8V	-	80	85	
		85Ω impedance, fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.VDD=1.8V	-	88	93	
I_{DDCLK_PD}	V_{DDCLK} Power-down Current	PWRGD_PWRDNb = 0.VDD=1.8V		1	3	mA
I_{DDR}	V_{DDR} Operating Current	85Ω impedance, fast slew rate, at 100MHz. PWRGD_PWRDNb = 1.VDD=1.8V	-	24	26	mA
		85Ω impedance, fast slew rate, at maximum output frequency. PWRGD_PWRDNb = 1.VDD=1.8V	-	28	31	mA
I_{DDR_PD}	V_{DDR} Power-down Current	PWRGD_PWRDNb = 0 VDD=1.8V	-	3.8	5	mA

2.5.8 SMBus Electrical Characteristics

Table 16. SMBus DC Electrical Characteristics [1]

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{IH}	High-level Input Voltage for SMBCLK and SMBDAT	-	0.8 VDD	-	-	V
V_{IL}	Low-level Input Voltage for SMBCLK and SMBDAT	-	-	-	0.3 VDD	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	-	0.05 VDD	-	-	
V_{OL}	Low-level Output Voltage for SMBCLK and SMBDAT	I_{OL} = 4mA	-	0.28	0.4	
I_{IN}	Input Leakage Current per Pin	-	[2]	-	[2]	µA
C_B	Capacitive Load for Each Bus Line	-	-	-	400	pF

1. V_{OH} is governed by the V_{PUP}, the voltage rail to which the pull-up resistors are connected.
2. For more information, see I/O Electrical Characteristics.

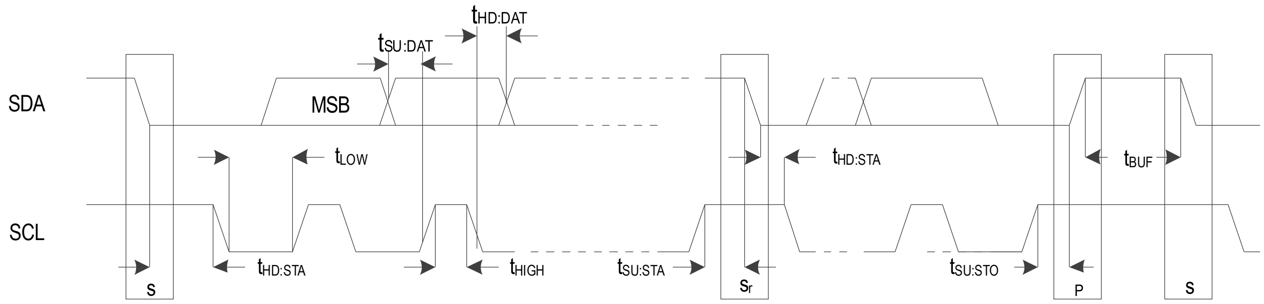


Figure 3. SMBus Slave Timing Diagram

Table 17. SMBus AC Electrical Characteristics

Symbol	Parameter	Condition	100kHz Class		400kHz Class		Unit
			MIN	MAX	MIN	MAX	
f_{SMB}	SMBus Operating Frequency	[1]	10	100	10	400	kHz
t_{BUF}	Bus free time between STOP and START Condition	-	4.7	-	1.3	-	µs
$t_{HD:STA}$	Hold Time after (REPEATED) START Condition	[2]	4	-	0.6	-	µs
$t_{SU:STA}$	REPEATED START Condition Setup Time	-	4.7	-	0.6	-	µs
$t_{SU:STO}$	STOP Condition Setup Time	-	4	-	0.6	-	µs
$t_{HD:DAT}$	Data Hold Time	[3]	300	-	300	-	ns
$t_{SU:DAT}$	Data Setup Time	-	250	-	100	-	ns
$t_{TIMEOUT}$	Detect SCL_SCLK Low Timeout	[4]	25	35	25	35	ms
$t_{TIMEOUT}$	Detect SDA_nCS Low Timeout	[5]	25	35	25	35	ms
t_{LOW}	Clock Low Period	-	4.7	-	1.3	-	µs
t_{HIGH}	Clock High Period	[6]	4	50	0.6	50	µs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time - Slave	[7]	N/A		N/A		ms
$t_{LOW:MEXT}$	Cumulative Clock Low Extend Time - Master	[8]	N/A		N/A		ms
t_F	Clock/Data Fall Time	[9]	-	300	-	300	ns
t_R	Clock/Data Rise Time	[9]	-	1000	-	300	ns
t_{SPIKE}	Noise Spike Suppression Time	[10]	-	–	0	50	ns

1. Power must be applied and PWRGD_PWRDNb must be a 1 for the SMBus to be active.
2. A master should not drive the clock at a frequency below the minimum f_{SMB}. Further, the operating clock frequency should not be reduced below the minimum value of fSMB due to periodic clock extending by slave devices as defined in Section 5.3.3 of System Management

Bus (SMBus) Specification, Version 3.1, dated 19 Mar 2018. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW:\ SEXT}$ and $t_{LOW:\ MEXT}$ limits. For example, if the SMBCLK is high for $t_{HIGH,MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB,MIN} – t_{HIGH,MAX}$. This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100 µs in a non-periodic way.

3. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the V_{IH},MIN of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
4. Slave devices may have caused other slave devices to hold SDA low. This is the maximum time that a device can hold SMBDAT low after the master raises SMBCLK after the last bit of a transaction. A slave device may detect how long SDA is held low and release SDA after the time out period.
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT,MAX}$ or longer.
6. The device has the option of detecting a timeout if the SMBDATA pin is also low for this time.
7. $t_{HIGH,MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.
8. tLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a slave device or another master will also extend the clock causing the combined clock low time to be greater than tLOW:MEXT on a given byte. This parameter is measured with a full speed slave device as the sole target of the master.
9. The rise and fall time measurement limits are defined as follows:
   Rise Time Limits: ($V_{IL:MAX}$ - 0.15 V) to ($V_{IH:MIN}$ + 0.15 V)
   Fall Time Limits: ($V_{IH:MIN}$ + 0.15 V) to ($V_{IL:MAX}$ - 0.15 V)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

2.5.9 Side-Band Interface

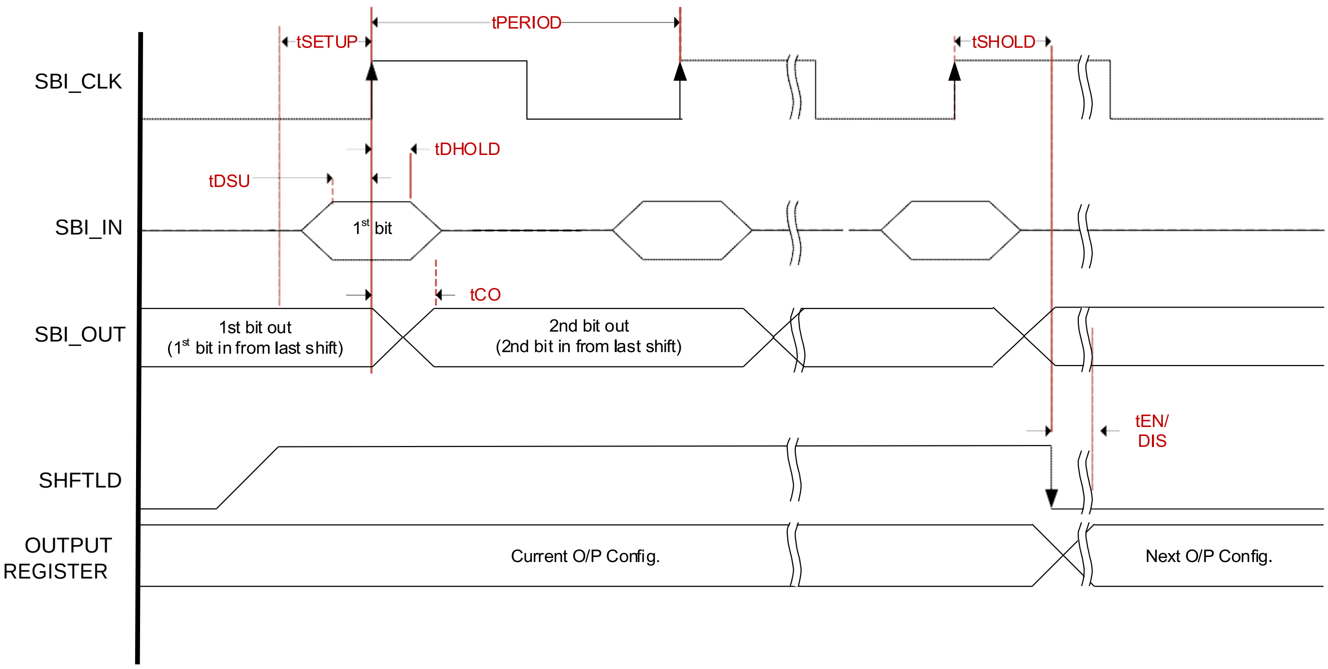


Figure 4. Side-Band Interface Timing

Figure 4 is the timing diagram and Table 18 provides the electrical characteristics for the Side-Band Interface. The SBI supports clock rates up to 25MHz.

Table 18. Electrical Characteristics – Side-Band Interface

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{PERIOD}	Clock Period	Clock period.	40	-	-	ns
t_{SETUP}	SHFT Setup Time to Clock	SHFT_LDB high to SBI_CLK rising edge.	10	-	-	ns
t_{DSU}	SBI_IN Setup Time	SBI_IN setup to SBI_CLK rising edge.	5	-	-	ns
t_{DHOLD}	SBI_IN Hold Time	SBI_IN hold after SBI_CLK rising edge.	2	-	-	ns
t_{CO}	SBI_CLK to SBI_OUT	SBI_CLK rising edge to SBI_OUT valid.	2	-	-	ns
t_{SHOLD}	SHFT Hold Time	SHFT_LDB hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LDB falling edge)	10	-	-	ns
$t_{EN/DIS}$	Enable/Disable Time	Delay from SHFT_LDB falling edge to next output configuration taking effect.[1]	4	-	12	clocks
t_{SLEW}	Slew Rate	SBI_CLK (between 20% and 80%).[2]	0.7	-	6	V/ns

3. Test Loads

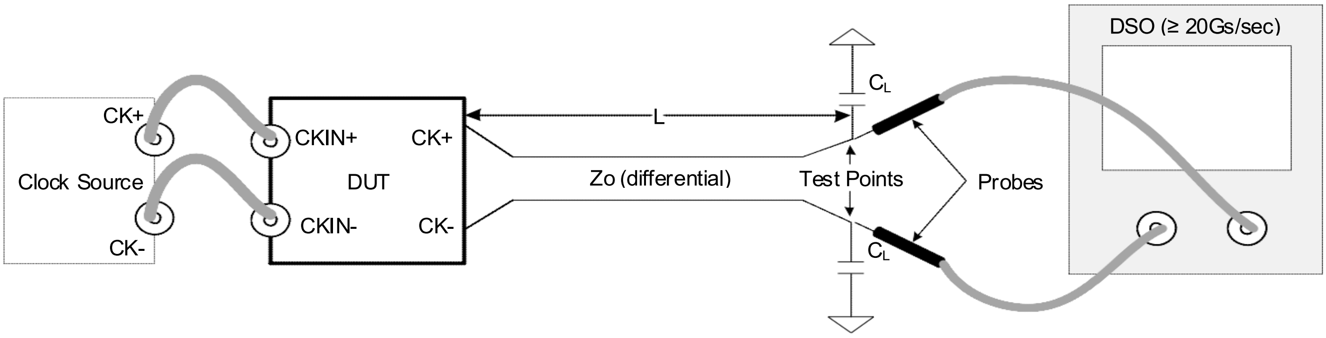


Figure 5. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

Table 19. Parameters for AC/DC Test Load (Standard PCIe Source-Terminated)

Device	Clock Source	Rs (ohms)	Zo (ohms)	L (cm)	C_L (pF)
RS2CB19008A	SMA100B	Internal	85	25.4	2
RS2CB19008A-100	SMA100B	Internal	100	25.4	2

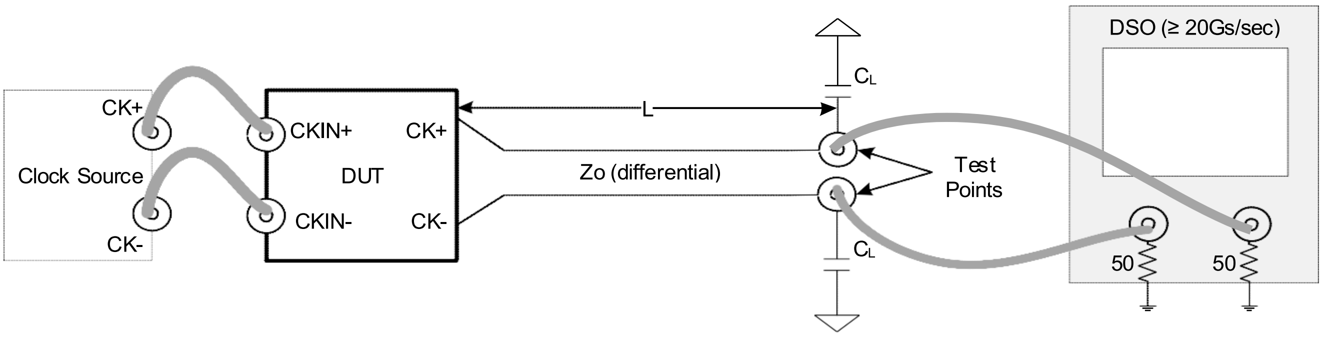


Figure 6. AC/DC Test Load for Differential Outputs (Double-Terminated)

Table 20. Parameters for AC/DC Test Load (Double-Terminated)

Device	Clock Source	Rs (ohms)	Zo (ohms)	L (cm)	C_L (pF)
RS2CB19008A	SMA100B	Internal	85	25.4	2
RS2CB19008A-100	SMA100B	Internal	100	25.4	2

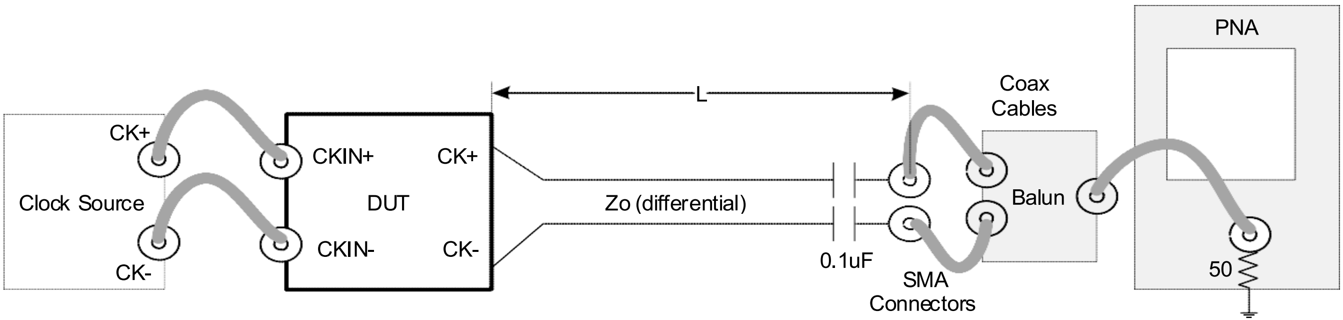


Figure 7. Test Load for PCIe Phase Jitter Measurements

Table 21. Parameters for PCIe Gen5 Jitter Measurement

Device	Clock Source	Rs (ohms)	Zo (ohms)	L (cm) [1]	C_L (pF)
RS2CB19008A	SMA100B	Internal	85	25.4	2
RS2CB19008A-100	SMA100B	Internal	100	25.4	2

1. PCIe Gen6 specifies L = 0cm for 32 and 64 GT/s. L = 25.4cm is more conservative.

4. SMBus Interface

4.1 Write Sequence

- Controller (host) sends a start bit
- Controller (host) sends the write address
- RS2CB19008A clock will **acknowledge**
- Controller (host) sends the beginning byte Location= N
- RS2CB19008A clock will **acknowledge**
- Controller (host) sends the byte count = X
- RS2CB19008A clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- RS2CB19008A clock will **acknowledge** each byte one at a time
- Controller (host) sends a stop bit

Index Block Write Operation

Controller (Host)			**RS2CB19008A (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stop bit		

4.2 Read Sequence

- Controller (host) will send a start bit
- Controller (host) sends the write address
- RS2CB19008A clock will **acknowledge**
- Controller (host) sends the beginning byte Location= N
- RS2CB19008A clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- RS2CB19008A clock will **acknowledge**
- RS2CB19008A clock will send the data byte count = X
- RS2CB19008A clock sends **Byte N+X-1**
- RS2CB19008A clock sends **Byte L through Byte X (if X(H) was written to Byte 7)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**RS2CB19008A (Slave/Receiver)**
T	start bit		
Slave Address			
WR	Write		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat start		
Slave Address			
RD	Read		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not		
P	stop bit		

4.3 SMBus Bit Types

Bit Description	Definition
RO	Read-only
RW	Read-write
RW1C	Read/Write '1' to clear
RESERVED	Undefined do not write

4.4 Write Lock Functionality

WRITE_LOCK	WRITE_LOCK RW1C	SMBus Write Protect
0	0	No
0	1	Yes
1	0	Yes
1	1	Yes

4.5 SMBus Address Decode

Address Selection		Binary Value								Hex Value
SADR_tri1	SADR_tri0	7	6	5	4	3	2	1	Rd/Wrt	
0	0	1	1	0	1	1	0	0	0	D8
	M	1	1	0	1	1	0	1	0	DA
	1	1	1	0	1	1	1	1	0	DE
M	0	1	1	0	0	0	0	1	0	C2
	M	1	1	0	0	0	1	0	0	C4
	1	1	1	0	0	0	1	1	0	C6
1	0	1	1	0	0	1	0	1	0	CA
	M	1	1	0	0	1	1	0	0	CC
	1	1	1	0	0	1	1	1	0	CE

2.6 RS2CB19008A SMBus Registers

Table 22. RS2CB19008A SMBus Registers

Byte	Register	Name	Bit	Type	Default	Description	Definition
0	OUTPUT_ENABLE_2	*RESERVED*	[7]	RW	0		0 = output is disabled (low/low) 1 = output is enabled
		RESERVED	[6]	RW	0		
		RESERVED	[5]	RW	0		
		RESERVED	[4]	RW	0		
		RESERVED	[3]	RW	0		
		RESERVED	[2:0]	RW	1		
1	OUTPUT_ENABLE_0	CLK7_EN	[7]	RW	1	Output Enable for CLK7	0 = output is disabled (low/low) 1 = output is enabled
		CLK6_EN	[6]	RW	1	Output Enable for CLK6	
		CLK5_EN	[5]	RW	1	Output Enable for CLK5	
		RESERVED	[4]	RW	0		
		RESERVED	[3]	RW	0		
		RESERVED	[2]	RW	0		
		RESERVED	[1]	RW	0		
		RESERVED	[0]	RW	0		
2	OUTPUT_ENABLE_1	*RESERVED*	[7]	RW	0		0 = output is disabled (low/low) 1 = output is enabled
		RESERVED	[6]	RW	0		
		CLK13_EN	[5]	RW	1	Output Enable for CLK13	
		CLK12_EN	[4]	RW	1	Output Enable for CLK12	
		CLK11_EN	[3]	RW	1	Output Enable for CLK11	
		CLK10_EN	[2]	RW	1	Output Enable for CLK10	
		RESERVED	[1]	RW	0		
		CLK8_EN	[0]	RW	1	Output Enable for CLK8	
3	OEb_PIN_READBACK	RB_OEb_12	[7]	RO	1'bX	Status of OEb12	0 = pin low 1 = pin high
		RB_OEb_11	[6]	RO	1'bX	Status of OEb11	
		RB_OEb_10	[5]	RO	1'bX	Status of OEb10	
		RESERVED	[4]	RO	1'bX		
		RB_OEb_8	[3]	RO	1'bX	Status of OEb8	
		RB_OEb_7	[2]	RO	1'bX	Status of OEb7	
		RB_OEb_6	[1]	RO	1'bX	Status of OEb6	
		RB_OEb_5	[0]	RO	1'bX	Status of OEb5	
4	SBEN_RDB_A CP_CONFIG	RESERVED	[7:5]	RW	1'b111		-
		ACP_ENABLE	[4]	RW	1	Enable Automatic Clock Parking to low/low when LOS event is detected	0 = disable ACP 1 = enable ACP
		RESERVED	[3:1]	RW	1'b110		-
		RB_SBI_ENQ	[0]	RO	1'bX	Status of SBI_ENQ	0 = pin low 1 = pin high

Table 22. RS2CB19008A SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
5	VENDOR_REVISION_ID	RID	[7:4]	RO	0x2	REVISION ID, A rev is 0000	-
		VID	[3:0]	RO	0x1	VENDOR ID	-
6	DEVICE_ID	DEVICE_ID	[7:0]	RO	0xC9	Device ID	-
7	BYTE_COUNT	RESERVED	[7:5]	RW	0x0	RESERVED	-
		BC	[4:0]	RW	0x7	Writing to this register configures how many bytes will be read back in a block read.	-
8	SBI_MASK_0	MASK7	[7]	RW	0	Masks off Side-band Disable for CLK7	0 = SBI may disable the output 1 = SBI cannot disable the output
		MASK6	[6]	RW	0	Masks off Side-band Disable for CLK6	
		MASK5	[5]	RW	0	Masks off Side-band Disable for CLK5	
		RESERVED	[4]	RW	0		
		RESERVED	[3]	RW	0		
		RESERVED	[2]	RW	0		
		RESERVED	[1]	RW	0		
		RESERVED	[0]	RW	0		
9	SBI_MASK_1	*RESERVED*	[7]	RW	0		0 = SBI may disable the output 1 = SBI cannot disable the output
		RESERVED	[6]	RW	0		
		MASK13	[5]	RW	0	Masks off Side-band Disable for CLK13	
		MASK12	[4]	RW	0	Masks off Side-band Disable for CLK12	
		MASK11	[3]	RW	0	Masks off Side-band Disable for CLK11	
		MASK10	[2]	RW	0	Masks off Side-band Disable for CLK10	
		RESERVED	[1]	RW	0		
		MASK8	[0]	RW	0	Masks off Side-band Disable for CLK8	

Table 22. RS2CB19008A SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
10	SBI_MASK_2	*RESERVED*	[7:4]	RW	0		-
		RESERVED	[3]	RW	0		0 = SBI may disable the output 1 = SBI cannot disable the output
		RESERVED	[2]	RW	0		
		RESERVED	[1]	RW	0		
		RESERVED	[0]	RW	0		
11	OUTPUT_SLEW_RATE_0	CLK7_SLEWRATE	[7]	RW	1	CLK7 Slewrate Control	0 = low slew rate 1 = high slew rate
		CLK6_SLEWRATE	[6]	RW	1	CLK6 Slewrate Control	
		CLK5_SLEWRATE	[5]	RW	1	CLK5 Slewrate Control	
		RESERVED	[4]	RW	1		
		RESERVED	[3]	RW	1		
		RESERVED	[2]	RW	1		
		RESERVED	[1]	RW	1		
		RESERVED	[0]	RW	1		
12	OUTPUT_SLEW_RATE_1	*RESERVED*	[7]	RW	1		0 = low slew rate 1 = high slew rate
		RESERVED	[6]	RW	1		
		CLK13_SLEWRATE	[5]	RW	1	CLK13 Slewrate Control	
		CLK12_SLEWRATE	[4]	RW	1	CLK12 Slewrate Control	
		CLK11_SLEWRATE	[3]	RW	1	CLK11 Slewrate Control	
		CLK10_SLEWRATE	[2]	RW	1	CLK10 Slewrate Control	
		RESERVED	[1]	RW	1		
		CLK8_SLEWRATE	[0]	RW	1	CLK8 Slewrate Control	
13	OUTPUT_SLEW_RATE_2	RESERVED	[7:4]	RW	0b111	RESERVED	0 = low slew rate 1 = high slew rate
		RESERVED	[3]	RW	1		
		RESERVED	[2]	RW	1		
		RESERVED	[1]	RW	1		
		RESERVED	[0]	RW	1		
14 - 19	RESERVED	-	-	-	-	RESERVED	-
20	LPHCSL_AMP_CTRL	AMP	[7:4]	RW	0x7	Global Differential output Control 0.625V~1V 25mV/step Default = 0.8V	-
		RESERVED	[3:0]	RW	0x7	RESERVED	-

Table 22. RS2CB19008A SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
21	PD_RESTORE_LOSb	AC_IN	[7]	RW	0	Enable receiver bias when CLKIN is AC coupled,	0 = DC coupled input 1 = AC coupled input
		Rx_TERM	[6]	RW	0	Enable termination resistors on CLKIN	0 = input termination R is disabled 1 = input termination R is enabled
		RESERVED	[5:4]	-	1'b11	-	-
		PD_RESTOREb	[3]	RW	1	Save Configuration in Power Down	0 = Config Cleared 1 = Config Saved
		SDATA_TIMEOUT_EN	[2]	RW	1	Enable SMB SDATA time out monitoring	0 = disable SDATA time out 1 = enable SDATA time out
		RESERVED	[1]	RO	1'bX	-	-
		LOSb_RB	[0]	RO	1'bX	real time read back of loss detect block output	0 = LOS event detected 1 = NO LOS event detected.
22–32	RESERVED	*RESERVED*	[7:0]	RW	0xXX	RESERVED	-
33	SBI_READBACK_0 [1]	SBI_CLK7	[7]	RO	1'bX	Readback of Side-band Disable for CLK7	0 = bit low 1 = bit high
		SBI_CLK6	[6]	RO	1'bX	Readback of Side-band Disable for CLK6	
		SBI_CLK5	[5]	RO	1'bX	Readback of Side-band Disable for CLK5	
		RESERVED	[4]	RO	1'bX		
		RESERVED	[3]	RO	1'bX		
		RESERVED	[2]	RO	1'bX		
		RESERVED	[1]	RO	1'bX		
		RESERVED	[0]	RO	1'bX		

Table 22. RS2CB19008A SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
34	SBI_READBACK_1 [1]	*RESERVED*	[7]	RO	1'bX		0 = bit low 1 = bit high
		RESERVED	[6]	RO	1'bX		
		SBI_CLK13	[5]	RO	1'bX	Readback of Side-band Disable for CLK13	
		SBI_CLK12	[4]	RO	1'bX	Readback of Side-band Disable for CLK12	
		SBI_CLK11	[3]	RO	1'bX	Readback of Side-band Disable for CLK11	
		SBI_CLK10	[2]	RO	1'bX	Readback of Side-band Disable for CLK10	
		RESERVED	[1]	RO	1'bX		
		SBI_CLK8	[0]	RO	1'bX	Readback of Side-band Disable for CLK8	
35	SBI_READBACK_2 [1]	*RESERVED*	[7:4]	RO	1'bXXX		0 = bit low 1 = bit high
		RESERVED	[3]	RO	1'bX		
		RESERVED	[2]	RO	1'bX		
		RESERVED	[1]	RO	1'bX		
		RESERVED	[0]	RO	1'bX		
36-37	RESERVED	*RESERVED*	[7:0]	RW	0xXX		
38	WRITE_LOCK_NCLEAR	*RESERVED*	[7:1]	RW	0x0		-
		WRITE_LOCK	[0]	RW	0	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by cycling power.	0 = SMBus not locked for writing by this bit. See WRITE_LOCK_RW1C bit. 1 = SMBus locked for writing
39	WRITE_LOCK_CLEAR_LOS_EVENT	*RESERVED*	[7:2]	RW1C	1'b111000	-	-
		LOS_EVT	[1]	RW1C	0	LOS Event Status When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it.	0 = No LOS event detected 1 = LOS event detected.
		WRITE_LOCK_RW1C	[0]	RW1C	0	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to it.	0 = SMBus not locked for writing by this bit. See WRITE_LOCK bit. 1 = SMBus locked for writing

1. Register only valid when the Side-Band Interface is enabled (SBI_ENQ = 1).

5. Applications Information

5.1 Inputs, Outputs, and Output Control

5.1.1 Recommendations for Unused Inputs and Outputs

5.1.1.1 Unused Differential CLKIN Inputs

For RS2CB19008A multiplexers that use only one input clock, the unused input can be left open. It is recommended that no trace be attached to unused CLKIN pins.

5.1.1.2 Unused Control Inputs

The control pins have internal pull-up or internal pull-down resistors and do not require external resistors. They can be left floating if the default pin state is the desired state. If external resistors are needed to change the pin state or are desired for design robustness, 10kohm is the recommended value.

5.1.1.3 Unused Differential CLK Outputs

All unused CLK outputs can be left floating. RSM recommends that no trace be attached to unused CLK outputs. While not required (but is highly recommended), the best design practice is to disable unused CLK outputs.

5.1.1.4 Unused SMBus Clock and Data Pins

If the SMBus interface is not used, the clock and data pins must be pulled high with an external resistor. If the interface may be used for debug, separate resistors should be used. 10kohm is the recommended value.

5.1.2 Differential CLKIN Configurations

The RS2CB19008A clock input supports four configurations:

- Direct connection to HCSL-level inputs
- Direct connection to LVDS-level inputs with *external* termination resistor
- Internal self-bias circuit for applications that *externally* AC-couple the input clock
  - This feature is enabled by the **AC_IN** bit.
- Internal pull-down resistors (Rp) to terminate the clock input at the receiver.
  - This feature is enabled by the **Rx_TERM** bit.

Devices with multiple input clocks have individual AC_IN and Rx_TERM configuration bits for each input. The internal input clock terminations prevent reflections and are useful for non-PCIe applications, where the frequency and transmission line length vary from the 100MHz PCIe standard.

Figure 8 through Figure 11 illustrate the above items.

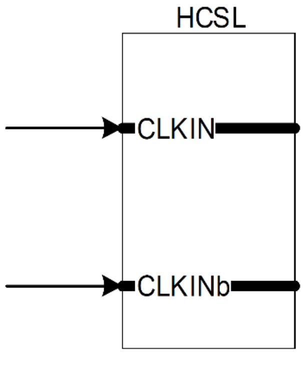


Figure 8. HCSL Input Levels (PCI-e Standard)

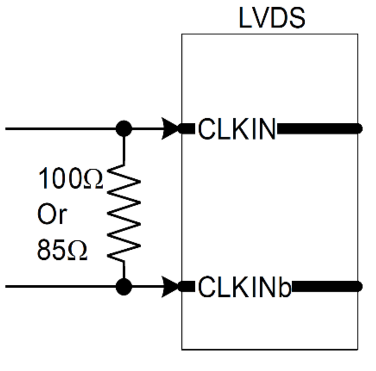


Figure 9. LVDS Input Levels

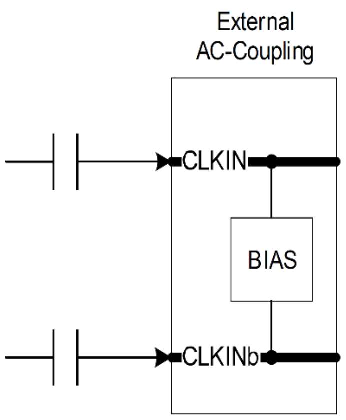


Figure 10. External AC-Coupling

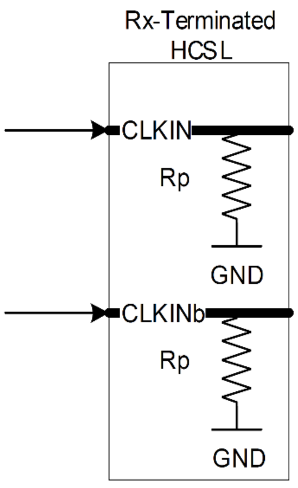


Figure 11. Receiver Termination

5.1.3 Differential CLK Output Configurations

5.1.3.1 Direct-Coupled HCSL Loads

The RS2CB19008A LP-HCSL clock outputs have internal source terminations and directly drive industry-standard HCSL-level inputs with no external components. They support both 85ohm and 100ohm differential impedances. The clock outputs can also drive receiver-terminated HCSL loads. The combination of source termination and receiver termination results in a double-terminated load. When double-terminated, the clock output swing will be half of the source-terminated values.

5.1.3.2 AC-Coupled non-HCSL Loads

The RS2CB19008A clock output can directly drive AC-coupling capacitors without any termination components. The clock input side of the AC-coupling capacitor may require an input-dependent bias network (BN). For examples of terminating the RS2CB19008A clock outputs to other logic families such as LVDS, LVPECL, or CML.

Figure 12 to Figure 14 show the various clock output configurations.

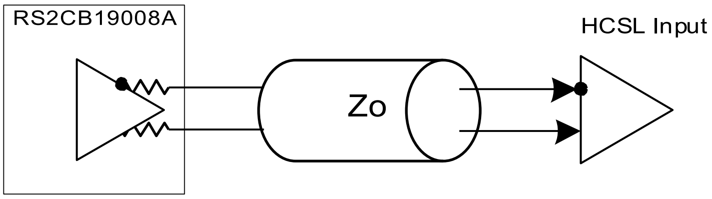


Figure 12. Direct-Coupled Source-Terminated HCSL

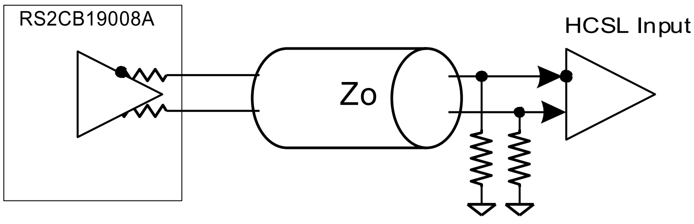
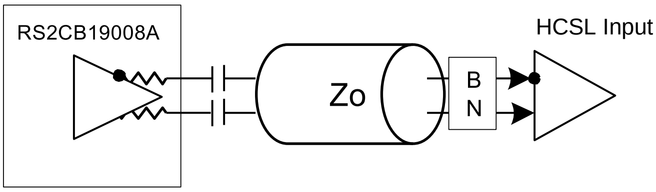


Figure 13. Direct-Coupled Double-Terminated HCSL



BN = Input-dependent bias network

Figure 14. AC-Coupled

5.2 Loss of Signal and Automatic Clock Parking

The RS2CB19008A have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOSb pin (the "b" suffix indicates "bar", or active-low) and sets the LOS_EVT bit in the SMBus register space.

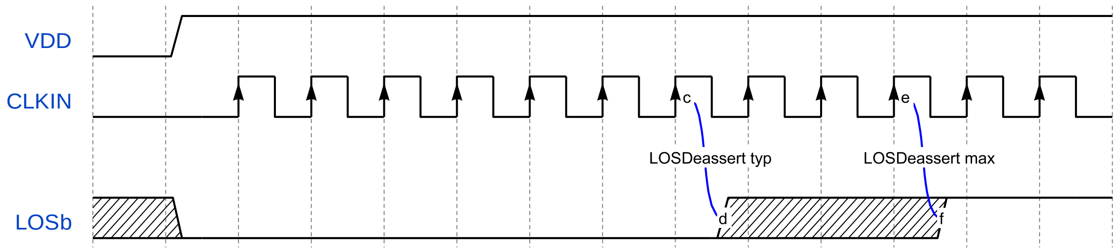


Figure 15. LOSb De-assert Timing RS2CB19008A Devices

Note: The LOSb pin monitors the *selected input clock* in the RS2CB19008A multiplexers.

The following diagram shows the LOSb assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event. For exact timing, see Electrical Characteristics.

5.3 Output Enable Control

The RS2CB19008A provides three mechanisms to enable or disable clock outputs. All three mechanisms start and stop the output clocks in a synchronous, glitch-free manner. A clock output is enabled only when all three mechanisms indicate "enabled." The following sections describe the three mechanisms.

5.3.1 SMBus Output Enable Bits

The RS2CB19008A has a traditional SMBus output enable bit for each output. The power-up default is 1, or enabled. Changing this bit to a 0 disables the output to a low/low state. The transitions between the enable and disable states are glitch-free in both directions.

Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

5.3.2 Output Enable (OEb) Pins

If the OEb pin is low the controlled output is enabled. If the OEb pin is high, the controlled output is disabled to a low/low state. All OEb pins enable and disable the controlled outputs in a glitch-free, synchronous manner.
Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.
The RS2CB19008A each have 7 OEb pins. Some of the pins are muxed with SBI functions.Details are provided in Table 23.

Table 23. RS2CB19008A OEb Mapping

Pin Name	SBI_ENQ Pin	Default Pin Function
OEb12	X	CLK12 OEb
OEb11	X	CLK11 OEb
OEb10_SHFT_LDb	0 (Disabled)	CLK10 OEb
	1 (Enabled)	SHFT_LDb
OEb8	X	CLK8 OEb
OEb7	X	CLK7 OEb
OEb6_SBI_CLK	0 (Disabled)	CLK6 OEb
	1 (Enabled)	SBI_CLK
OEb5_SBI_IN	0 (Disabled)	CLK5 OEb
	1 (Enabled)	SBI_IN

5.3.3 Side-Band Interface (SBI)

SBI function and Connection Topologies refer to RS2CB190xx Series Datasheet.

The RS2CB19008A support two SBI connection topologies: Star and Daisy-chain.

5.3.4 Output Enable/Disable Priority

The RS2CB19008A output enable/disable priority is an “AND” function of all enable methods. This means that the SMBus output enable bit AND the OEb pin (if present/assigned) AND the SBI must indicate that the output is enabled in order for the output to be enabled. A logical representation of the priority logic is shown in Figure 16.

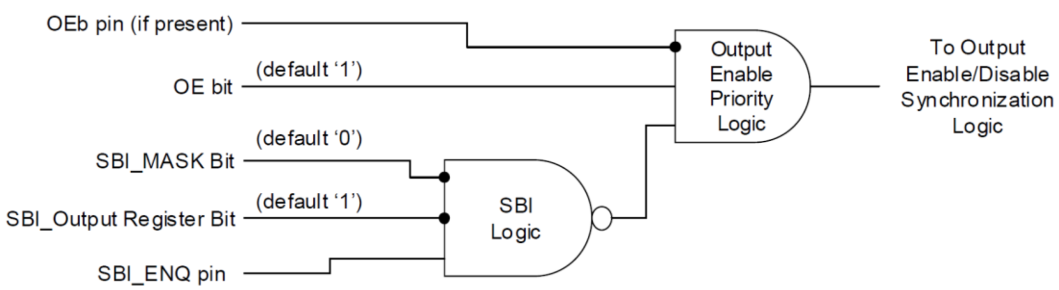
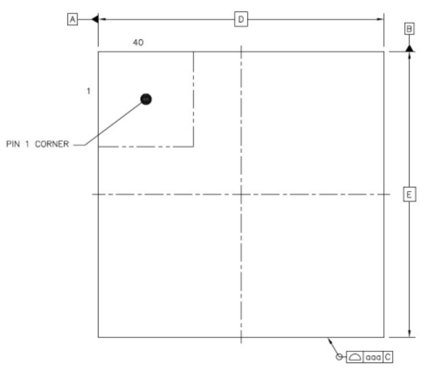


Figure 16. Output Enable/Disable Priority (Logical)

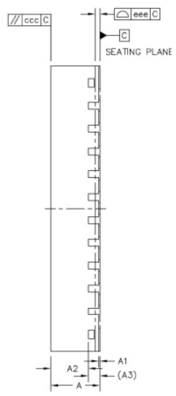
6. Package Information

The package outline drawings are located at the end of this document and are accessible from the website. The package information is the most current data available and is subject to change without revision of this document.

TQFN 5x5X0.85-40L

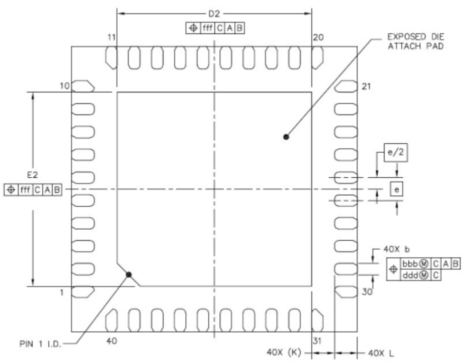


Top View



Side View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K	0.4 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
		ddd	0.05		
EXPOSED PAD OFFSET		fff	0.1		



Bottom View

Note:
1.All dimensions are in mm.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-220

TQFN 5x5x0.85mm(ZLA40) POD Rev.0

Raystar Microelectronics Technology Inc

7. Revision History

Revision	Description	Date
V0.9	Preliminary release	2024/11/13
V1.0	Initial release	2024/11/15
V1.1	Modify Pin18 CLK to CLK6	2024/12/09