Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I^2C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I^2C-bus and SMBus compatible
- Less than 1.5 ns propagation delay
- Allows voltage level translation between:
  - 1.0 V VREF1 and 1.8 V～5 V V_{REF2}
  - 1.2 V VREF1 and 1.8 V～5 V V_{REF2}
  - 1.5 V VREF1 and 2.5 V～5 V V_{REF2}
  - 1.8 V VREF1 and 3.3 V～5 V V_{REF2}
  - 2.5 V VREF1 and 3.3 V～5 V V_{REF2}
  - 3.3 V VREF1 and 5 V V_{REF2}
- Bidirectional voltage translation with no direction pin
- Low 3.5 ohm ON-state connection between input and output ports provides less signal distortion
- 5 V tolerant I^2C-bus I/O ports to support mixed-mode signal operation
- Lock-up free operation for isolation when EN= LOW
- Flow through pin out for ease of printed-circuit board trace routing
- ESD protection exceeds 4000V HBM
- Temperature: -40°C to +85°C

Description

The RS7LS4551 is a dual bidirectional I^2C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.3 V (V_{REF1}) and 1.8 V to 5.5 V(V_{REF2}).

The RS7LS4551 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The RS7LS4551 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The RS7LS4551 only isolates both sides when the device is disabled and provides voltage level translation when active.

The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Block Diagram

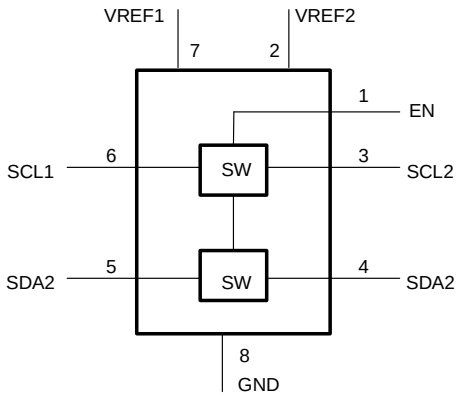


Figure 1: Block Diagram

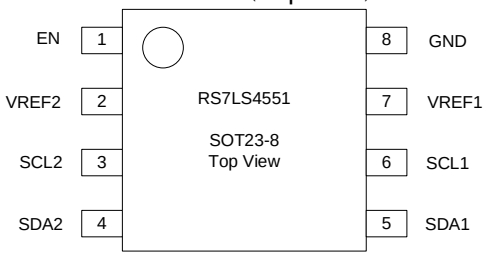
Ordering Information

Ordering Code	Package	Package Description
RS7LS4551ZEE	TDFN	8-pin, 2.0x3.0 mm
RS7LS4551TE	SOT	8-Pin, SOT23

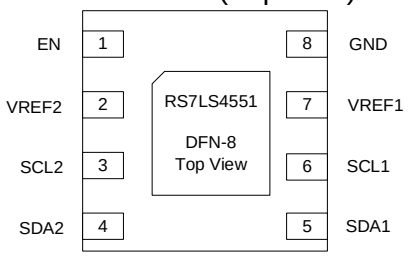
Notes:
[1] E = Pb-free and Green

Pin Configuration

SOT23-8（Top view）



TDFN-8 (Top view)



Pin Name	Pin NO. SOT23	Pin NO. DFN-8	Description
EN	1	1	Output enables (active High).
VREF1	7	7	low-voltage side reference supply voltage for SCL1 and SDA1
SCL1	6	6	serial clock, low-voltage side;
SDA1	5	5	serial data, low-voltage side;
SDA2	4	4	serial data, high-voltage side;
SCL2	3	3	serial clock, high-voltage side;
VREF2	2	2	high-voltage side reference supply voltage for SCL2 and SDA2
GND	8	8	GND

Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
Tstore	Storage Temperature	−65	-	+150	°C
VREF1	DC reference voltage range	-0.3	-	6.0	V
VREF2	DC reference bias voltage range	-0.3	-	6.0	V
VIO	Input/output voltage range	-0.3	-	6.0	V
Ich	Continuous channel current	-	-	128	mA
IIK	Input clamp current (V_I<0V)	-0.3	-	-50	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
$V_{I/O}$	Voltage on an input/output pin	0	-	5.5	V
V_{REF1}	Reference voltage1	0	-	5.5	V
V_{REF2}	Reference bias voltage 2	0	-	5.5	V
$V_{I(EN)}$	Input voltage on pin EN	0	-	5.5	V
$I_{(pass)}$	Pass switch current	-	-	64	ns/V
T_A	Ambient temperature	-40	-	85	°C

DC Electrical Characteristics

T_A = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions (1)		MIN	TYP	MAX	Unit
Input and output SDAn and SCLn							
VIK	input clamping voltage	II = -18mA; VI(EN) = 0 V		-	-	-1.2	V
IIH	HIGH-level input current	VI = 5 V; VI(EN) = 0 V		-	-	5	µA
Ci(EN)	input capacitance on pin EN	VI = 3 V or 0 V		-	11	-	pF
Cio(off)	Off-state input/output capacitance (SCLn, SDAn)	VO = 3 V or 0 V; VI(EN) = 0 V		-	4	-	pF
Cio(on)	on-state input/output capacitance (SCLn, SDAn)	VO = 3 V or 0 V; VI(EN) = 3 V		-	10.5	-	pF
Ron	ON-state resistance (2) (SCLn, SDAn)	VI = 0V; IO =64mA	VI(EN) = 4.5 V	-	3.5	5.5	Ω
			VI(EN) = 3 V	-	4.7	7	Ω
			VI(EN) = 2.3 V	-	6.3	9.5	Ω
			VI(EN) = 1.5 V	-	8.5	13	Ω
		VI = 2.4V; IO=15mA	VI(EN) = 4.5 V	1	6	15	Ω

Notes:
1. All typical values are at T_A = 25 °C.
2. Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

Dynamic characteristics

T_A = -40 °C to +85 °C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	CL = 50 pF		CL = 30 pF		CL = 15 pF		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
Dynamic characteristics (translating down)									
VI(EN) = 3.3 V; VIH = 3.3 V; VIL = 0 V; VM = 1.15 V									
tPLH	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
tPHL	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.2	0	1	0	0.5	ns
VI(EN) = 2.5 V; VIH = 2.5 V; VIL = 0 V; VM = 0.75 V									
tPLH	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1	0	0.7	0	0.5	ns
tPHL	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.3	0	1	0	0.6	ns
Dynamic characteristics (translating up)									
VI(EN) = 3.3 V; VIH = 2.3 V; VIL = 0 V; VT = 3.3 V; VM = 1.15 V;									
tPLH	LOW-to-HIGH propagation delay	from (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
tPHL	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.4	0	1.1	0	0.7	ns
VI(EN) = 2.5 V; VIH = 1.5 V; VIL = 0 V; VT = 2.5 V; VM = 0.75 V;									
tPLH	LOW-to-HIGH propagation delay	from (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
tPHL	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.3	0	1.3	0	0.8	ns

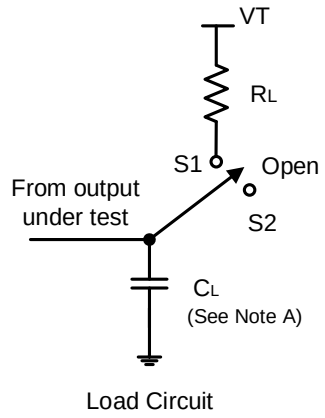


Figure.2 Load Circuit for Outputs

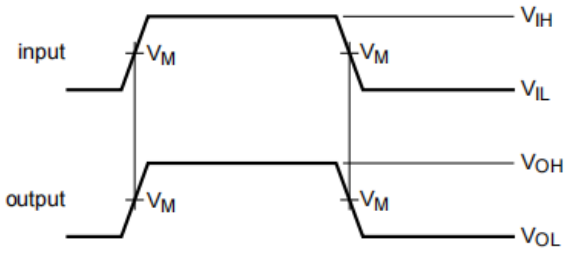


Figure3. Parameter Measurement information

Notes: A. C_L includes probe and jig capacitance.
B. All input pluses are supplied by generators having the following characteristics: PRR≤10Mhz, Zo=50Ω，t_r≤2ns，t_f≤2ns.
C. The outputs are measured one at a time, with one transition per measurement.

Functional Description

The RS7LS4551 can also be used to run two buses, one at 400kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The RS7LS4551 has a standard open-collector configuration of the I^2C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I^2C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical.

Application Information

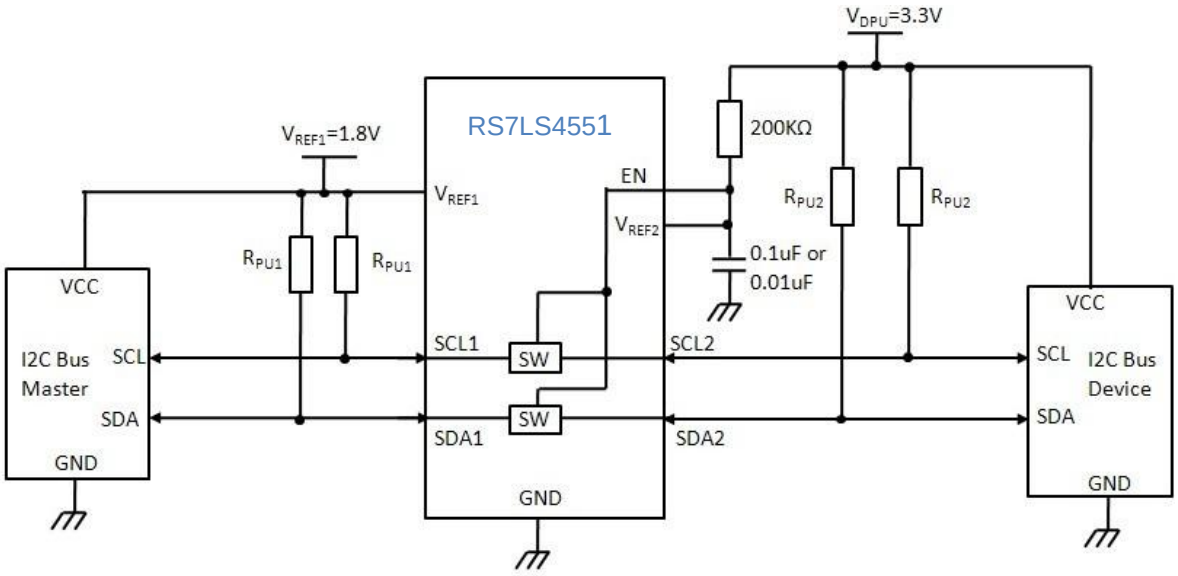


Figure.4 Typical Application Circuit (Switch Always Enabled)

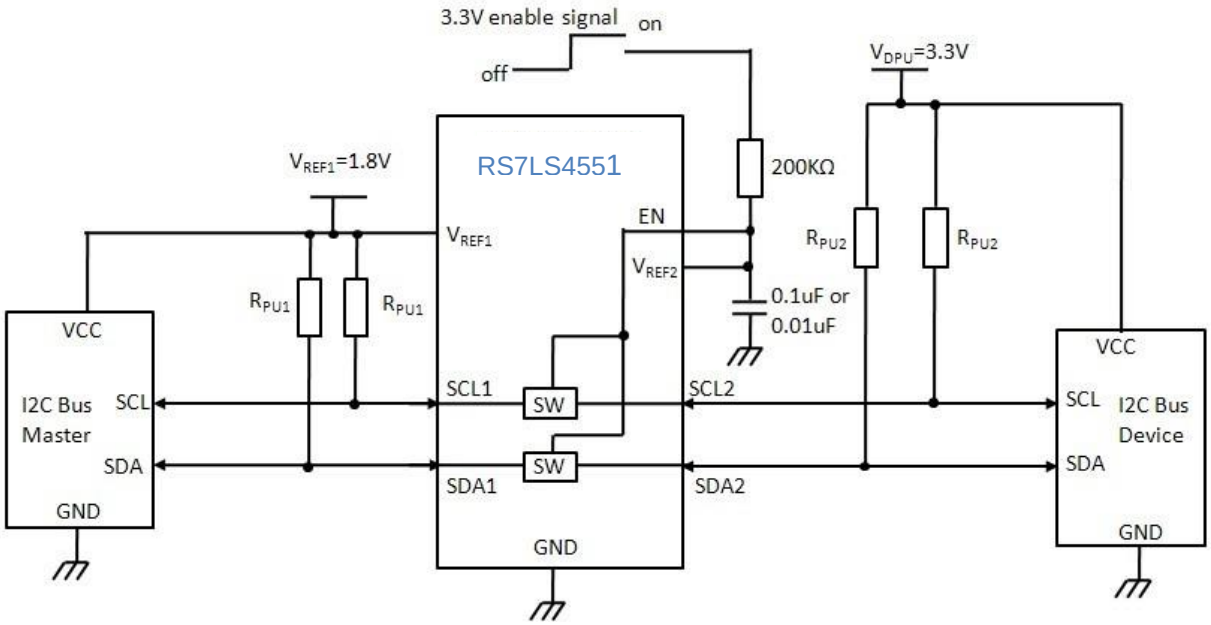


Figure5. Typical Application Circuit (Switch Enabled Control)

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to high-side VDPU through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended.

The I2C bus controller output can be totem pole or open-drain (pull-up resistors may be required) and the I2C-bus device output can be totem pole or open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to

V_{DPU}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

pull-up resistor value

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sinks current
- The V_{OL} of driver
- The V_{IL} of the driver
- Frequency of operation

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(max) = \frac{1}{tLow(min) + tHigh(min) + tr(actual) + tf(actual)}$$

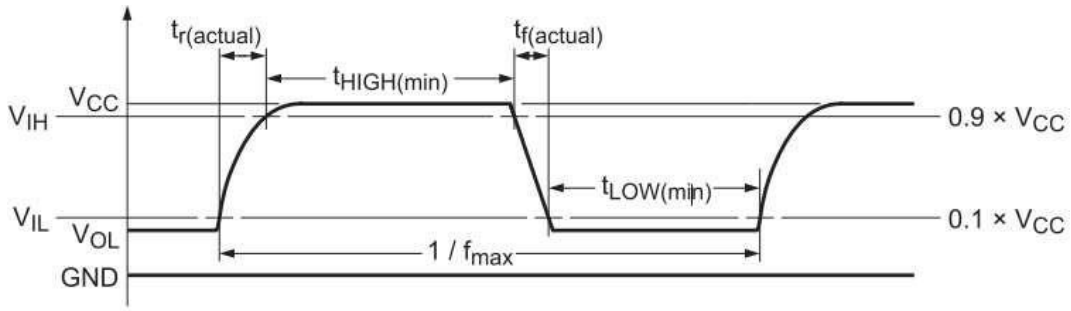


Figure 6. An example waveform for maximum frequency

The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (C_L) and the pull-up resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus. Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

A description of the fall time applied to either An or Bn output going from HIGH to LOW is as follows. Whichever side is asserted first, the B-side down must discharge to the VCC(A) voltage. The time is determined by the pull-up resistor, pull-down driver strength and the capacitance. As the level moves below the VCC(A) voltage, the channel resistance drops so that both A and B sides equal. The capacitance on both sides is connected to form the total capacitance and the pull-up resistors on both sides combine to the parallel equivalent resistance. The Ron of the device is small compared to the pull-up resistor values, so its effect on the pull-up resistance can be neglected and the fall is determined by the driver pulling the combined capacitance and pull-up resistor currents. An estimation of the actual fall time seen by the device is equal to the time it takes for the B-side to fall to the VCC(A) voltage and the time it takes for both sides to fall from the VCC(A) voltage to the VIL level.

A description of the rise time applied to either An or Bn output going from LOW to HIGH is as follows. When the

signal level is LOW, the Ron is at its minimum, so the A and B sides are essentially one node. They will rise together with an RC time constant that is the sum of all the capacitance from both sides and the parallel of the resistance from both sides. As the signal approaches the VCC(A) voltage, the channel resistance goes up and the waveforms separate, with the B side finishing its rise with the RC time constant of the B side. The rise to VCC(A) is essentially the same for both sides.

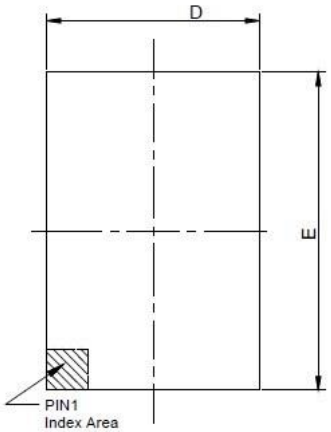
Layout guidelines

To make full use of the performance of RS7LS4551, the guidelines below should be followed:

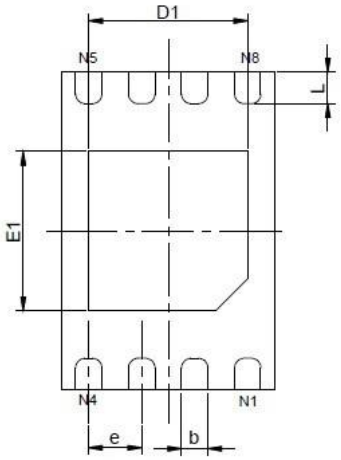
1. C_{VCCA} and C_{VCCB} should be placed on the top layer as close as possible to the V_{CCA} and V_{CCB} pin.
2. The trace of signals should be short enough to avoid any reflection when transmitted

Packaging Mechanical:

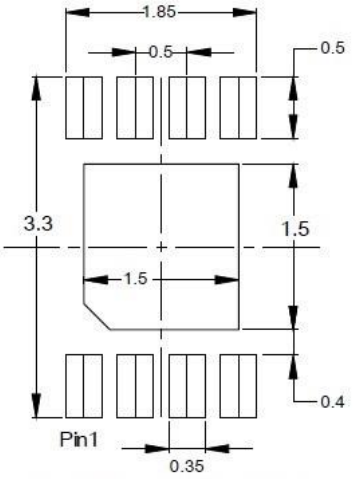
DFN 2x3-8L



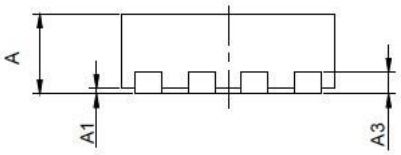
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-229
3.Dimensions exclude burrs, mold flash or protrusions.

TDFN2X3-8L (ZE08) POD Rev.0
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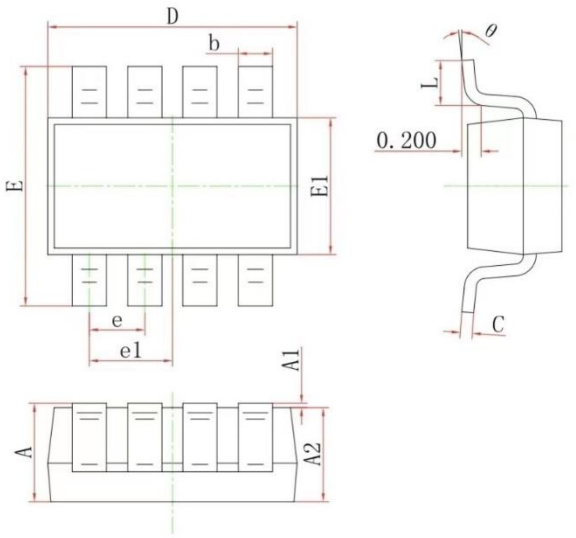
SOT23-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.650BSC.		0.026BSC.	
e1	0.975BSC.		0.038BSC.	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MO-178

SOT23-8L POD Rev.0
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Revision History

Revision	Description	Date
0.1	Revise Pin Description	2023/4/12
0.2	Revise some wrong definition	2023/4/21
1.0	1. Modify max rating 2. Modify functional description 3. Modify DC and Electrical Characteristics spec 4. Modify Dynamic characteristics spec.	2024/5/22