RS5AP6011, RS5AP6012, RS5AP6014

Low-power and Low-Voltage Rail to Rail Operational Amplifier

Features

- Supply Voltage: 2.1V to 5.5V
- Low Supply Current: 900μA per channel
- Rail to Rail Input and Output
- Bandwidth: 10MHz
- Slew Rate: 8V/μs
- Excellent EMI Suppress Performance
- Offset Voltage: ±3mV Maximum
- Offset Voltage Temperature Drift: 2μV/°C
- Low Noise: 27nV/√Hz at 1kHz
- High Output Capability: 70mA
- −40°C to 125°C Operation Temperature Range

Applications

- Smoke detectors
- HVAC: heating, ventilating, and air conditioning
- Motor control: AC induction
- Refrigerators
- Wearable devices
- Laptop computers
- Washing machines
- Sensor signal conditioning
- Power modules
- Barcode scanners
- Active Filters
- Low-side current sensing

Description

The RS5AP601X family of single-, dual-, and quad-channel operational amplifiers is specifically designed for general-purpose applications. Featuring rail-to-rail input and output (RRIO) swings, low quiescent current (900μA, typical), wide bandwidth (10MHz), and low noise (27nV/√Hz at 1kHz), this family is attractive for a variety of applications that require a good balance between cost and performance, such as consumer electronics, smoke detectors, and white goods. The low-input-bias current (±1.0pA, typical) enables the RS5AP601X to be used in applications with megaohm source impedances.

The robust design of the RS5AP601X provides ease-of- use to the circuit designer: unity-gain stability with capacitive loads of up to 100pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4kV HBM).

The devices are optimized for operation at voltages as low as 2.1V (±1.05V) and up to 5.5V (±2.75V), and are specified over the extended temperature range of –40°C to +125°C.

The single-channel RS5AP6011 is available in SOT23-5 and SC70-5 packages. The dual-channel RS5AP6012 is available in SOP-8, MSOP-8, and DFN2X2-8 packages, and the quad-channel RS5AP6014 is offered in a TSSOP-14 and SOP-14 package.

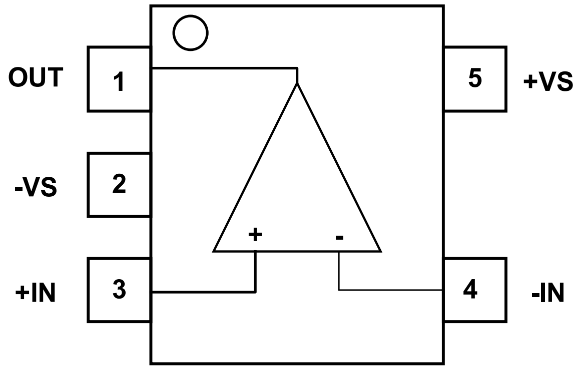
Device Information

Part Number	Package	Description
RS5AP6011TAE	SOT23-5	3mmx2.9mm
RS5AP6011UCE	SC70-5	2mmx1.25mm
RS5AP6012WE	SOP-8	6mmx4.9mm
RS5AP6012UE	MSOP-8	5.15mmx3.2mm
RS5AP6012ZAE	DFN2X2-8	2mmx2mm
RS5AP6014WE	SOP-14	8.65mmx6mm
RS5AP6014LE	TSSOP-14	6.4mmx5mm

Notes：
E = Pb-free and Green

Pin Configuration and Functions

5 Pin Functions: RS5AP6011

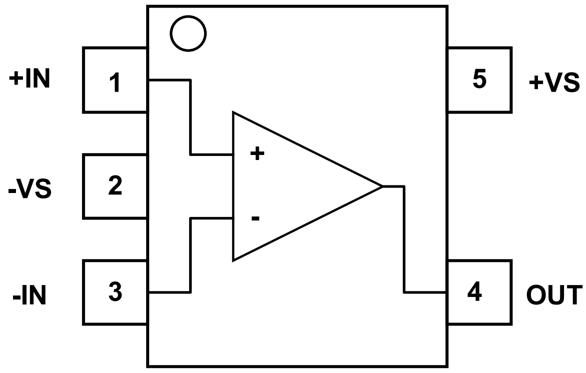


RS5AP6011
SOT-23-5, Top View

Table 1. Pin Functions: RS5AP6011

PINS		I/O	Description
NAME	No.		
OUT	1	O	Output
-VS	2	–	Negative Supply Voltage
IN+	3	I	Non-Inverting Input
IN-	4	I	Inverting Input
+VS	5	–	Positive Supply Voltage

5 Pin Functions: RS5AP6011U

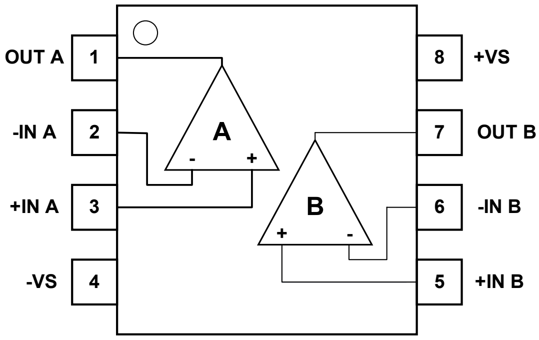


RS5AP6011U
SC70-5, Top View

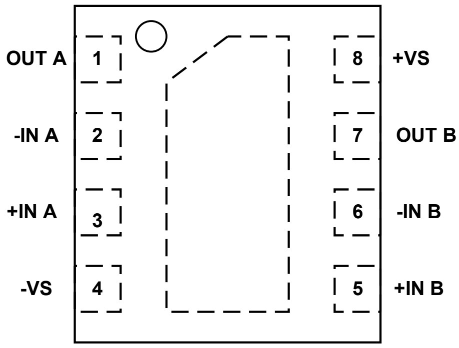
Table 2. Pin Functions: RS5AP6011U

PINS		I/O	Description
NAME	No.		
IN+	1	I	Non-Inverting Input
-VS	2	–	Negative Supply Voltage
IN-	3	I	Inverting Input
OUT	4	O	Output
+VS	5	–	Positive Supply Voltage

8 Pin Functions: RS5AP6012



RS5AP6012
SOP-8/MSOP8 Top View

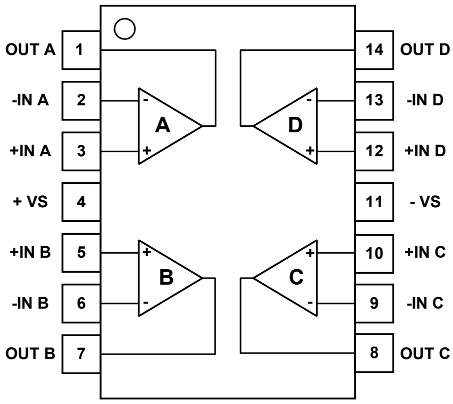


RS5AP6012
DFN2X2-8, Top View

Table 3. Pin Functions: RS5AP6012

PINS		I/O	Description
NAME	NO.		
OUTA	1	O	Output, Channel A
-IN A	2	I	Inverting Input, Channel A
+IN A	3	I	Noninverting Input, Channel A
-VS	4	–	Negative Supply Voltage
+IN B	5	I	Noninverting Input, Channel B
-IN B	6	I	Inverting Input, Channel B
OUT B	7	O	Output, channel B
+VS	8	–	Positive Supply Voltage

14 Pin Functions: RS5AP6014



RS5AP6014
SOP-14/TSSOP-14, Top View

Table 4. Pin Functions: RS5AP6014

PINS		I/O	Description
NAME	NO.		
OUTA	1	O	Output, Channel A
-IN A	2	I	Inverting Input, Channel A
+IN A	3	I	Noninverting Input, Channel A
+VS	4	–	Positive Supply Voltage
+IN B	5	I	Noninverting Input, Channel B
-IN B	6	I	Inverting Input, Channel B
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
- VS	11	–	Negative Supply Voltage
+IN D	12	I	Noninverting input, channel D
-IN D	13	I	Inverting input, channel D
OUT D	14	O	Output, channel D

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Supply Voltage			7	V
Input Voltage		$(V^-) - 0.3$	$(V^+) + 0.3$	V
Input Current: +IN, −IN (2)			±10	mA
Differential Input Voltage		$(V^-) - (V^+)$	$(V^+) - (V^-)$	mV
Output Short-Circuit Duration (3)			Indefinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	250	81	°C/W
SOP-8	158	43	°C/W
MSOP-8	210	45	°C/W
DFN2X2-8	100	60	°C/W
SOP-14	120	36	°C/W
TSSOP-14	180	35	°C/W

Electrical Characteristics

All test conditions: V_S = 5 V, R_L = 10 K, V_{CM} = V_{DD}/2, T_A = +27°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_S	Supply Voltage Range		2.1		5.5	V
I_Q	Quiescent Current per Amplifier			900		μA
PSRR	Power Supply Rejection Ratio			90		dB
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V to 3V		0.5		mV
V_{OS} TC	Input Offset Voltage Drift	T_A = −40°C to 125°C		2		μV/°C
I_B	Input Bias Current	T_A = 25°C		1		pA
		T_A = 85°C		50		pA
I_{OS}	Input Offset Current			1		pA
C_{IN}	Input Capacitance	Differential Mode		8		pF
		Common Mode		6.5		pF
Av	Open-loop Voltage Gain	R_{LOAD} = 10kΩ		110		dB
V_{CMR}	Common-mode Input Voltage Range		(V-) –0.1		(V+) +0.1	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3V		100		dB
Xtalk	Channel Separation	f = 1kHz, R_L = 2kΩ		110		dB
Output Characteristics						
V_{OH}, V_{OL}	Maximum Output Voltage Swing	R_{LOAD} = 10kΩ		5		mV
I_{SC}	Output Short-Circuit Current			70		mA
AC Specifications						
GBW	Gain-Bandwidth Product			10		MHz
SR	Slew Rate	A_V = 1, V_{OUT} =1.5V to 3.5V, R_{LOAD} = 10kΩ		8		V/μs
t_S	Settling Time, 0.1%	A_V = 1, 2 V Step, C_{LOAD} = 10pF, R_{LOAD} = 10kΩ		2.7		μs
	Settling Time, 0.01%			4.8		μs
PM	Phase Margin	R_{LOAD} = 10kΩ		70		°
GM	Gain Margin	R_{LOAD} = 10kΩ		15		dB
Noise Performance						
E_N	Input Voltage Noise	f = 0.1Hz to 10Hz		8		μV_{PP}
e_N	Input Voltage Noise Density	f = 1kHz		27		$nV\sqrt{HZ}$
i_N	Input Current Noise	f = 1kHz		2		$fA\sqrt{HZ}$
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, A_V = 1, R_L = 2kΩ, V_{OUT} = 1Vp-p		0.003		%

Typical Performance Characteristics

V_S = 5 V, V_{CM} = 2.5 V, R_L = 10K, unless otherwise specified.

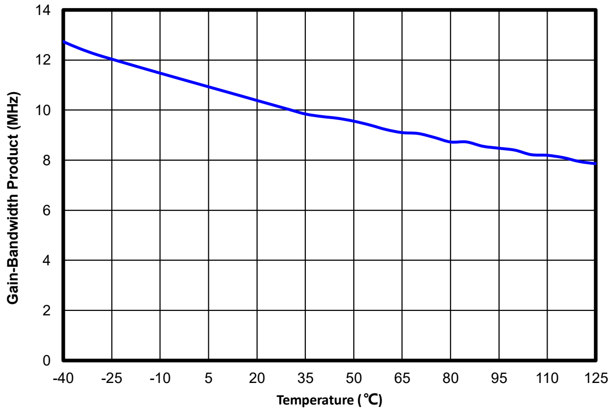


Figure 1. Unity Gain Bandwidth vs. Temperature

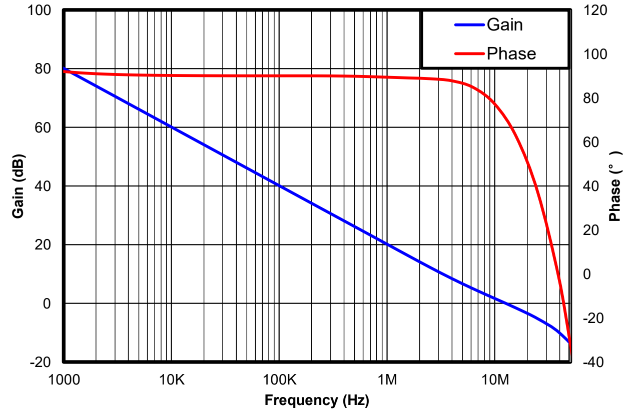


Figure 2. Open-Loop Gain and Phase

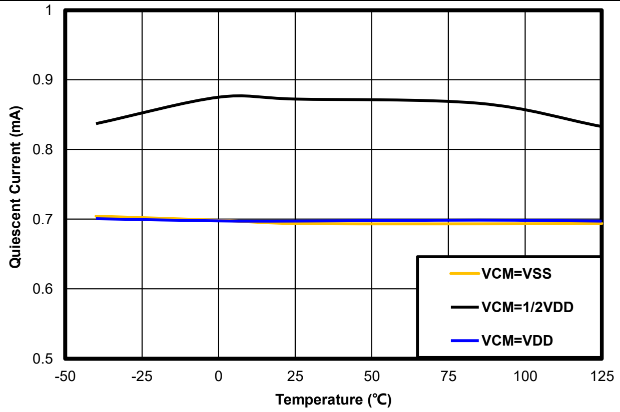


Figure 3. Supply Current vs. Temperature

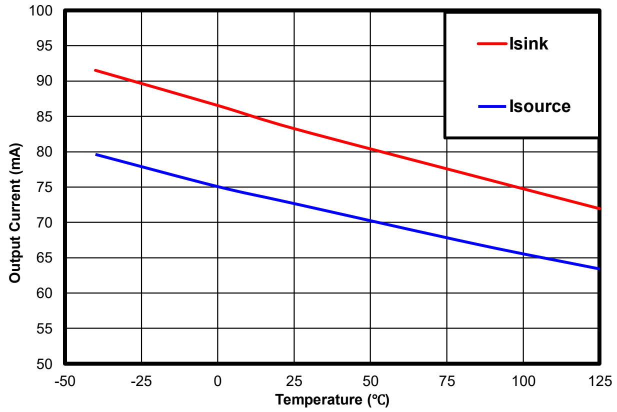


Figure 4. Short Circuit Current vs. Temperature

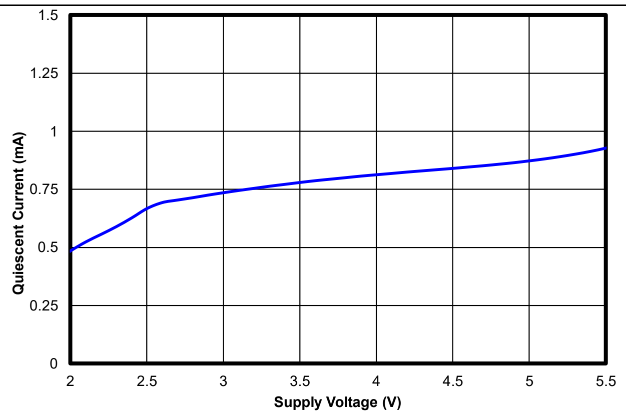


Figure 5. Quiescent Current vs. Supply Voltage

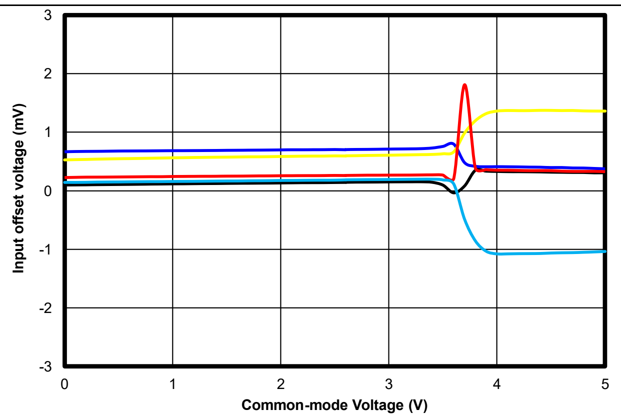


Figure 6. Offset Voltage vs. Common-Mode Voltage

Typical Performance Characteristics (Continued)

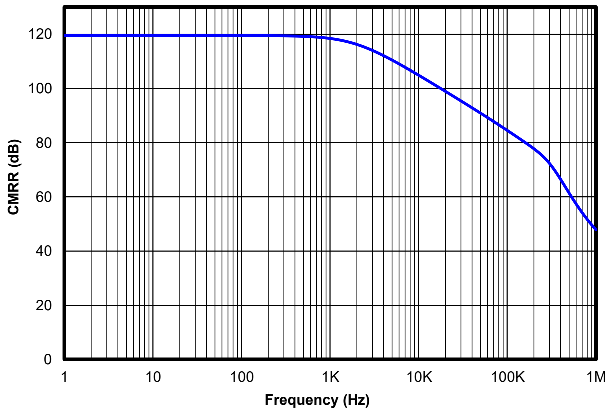


Figure 7. CMRR vs. Frequency

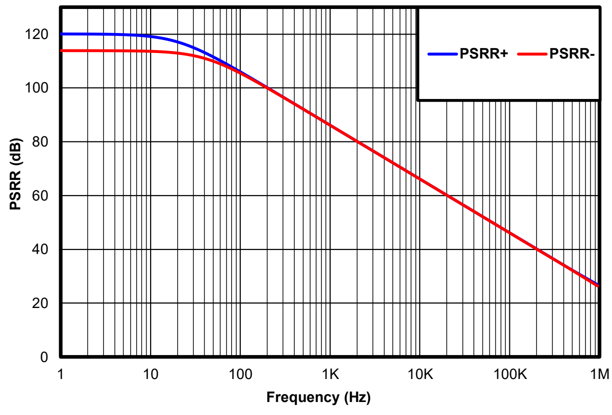


Figure 8. PSRR vs. Frequency

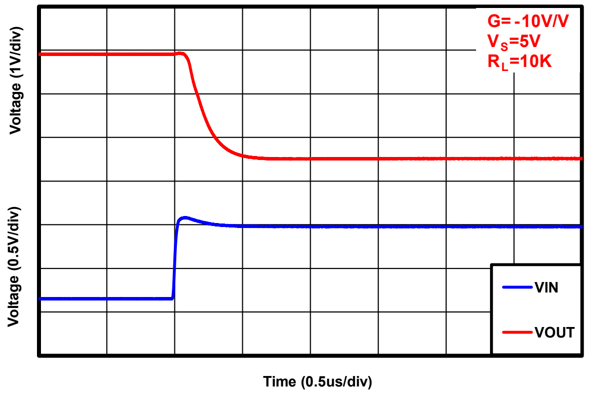


Figure 9. Positive Over-Voltage Recovery

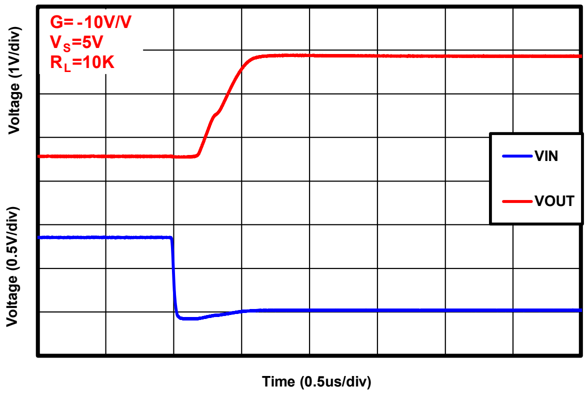


Figure 10. Negative Over-Voltage Recovery

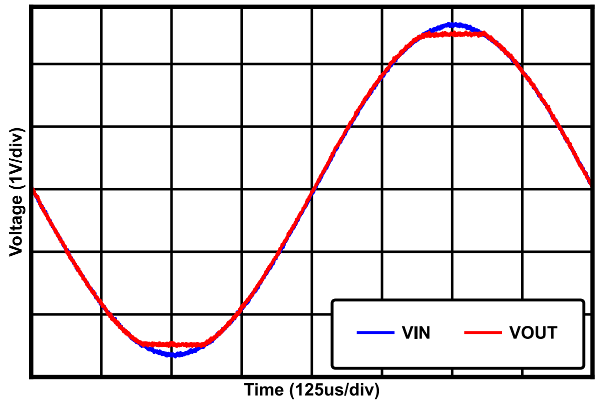


Figure 11. No Phase Reversal

Application Information

Low Supply Voltage and Low Power Consumption

The RS5AP601X family of operational amplifiers operates efficiently within a supply voltage range of 2.1 V to 5.5 V, drawing a quiescent current of only 900 µA per amplifier. This combination of low supply voltage and low current consumption makes these amplifiers ideal for portable applications that require high capacitive load driving capability and stable wide bandwidth performance. Optimized for wide bandwidth, low-power applications, the RS5AP601X family offers an industry-leading gain bandwidth product (GBWP) to power ratio. They maintain unity gain stability across all capacitive loads, ensuring reliable performance. When the load capacitance increases, the non-dominant pole in the open-loop frequency shifts to a lower frequency, reducing the phase and gain margin. Higher gain configurations tend to perform better in capacitive load driving than lower gain configurations due to a lower closed-loop bandwidth, which results in a higher phase margin.

Ground Sensing and Rail to Rail Output

The RS5AP601X family boasts excellent output drive capabilities, delivering over 70 mA of output current. Its rail-to-rail output topology allows the output voltage to swing within 10 mV of either supply rail. With input terminals that can extend 200 mV beyond both supply rails, these op-amps enable true ground sensing, enhancing their versatility in various applications. The maximum output current capability is dependent on the supply voltage; as the supply voltage increases, so does the output current capacity. To prevent thermal damage, the junction temperature of the IC must be kept below 150°C during continuous short-circuit conditions. The output stage features reverse-biased ESD diodes connected to each supply, and care should be taken to ensure the output voltage does not exceed 0.5 V beyond either supply rail to avoid undesirable current flow through these diodes.

Driving Large Capacitive Load

Larger load capacitance decreases the overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in output step response. The unity-gain buffer (G = +1 V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the RS5AP601X OPA family (e.g., > 200 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 12) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.

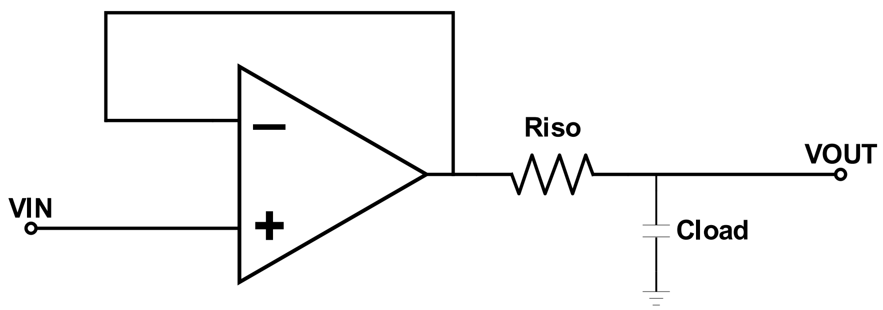
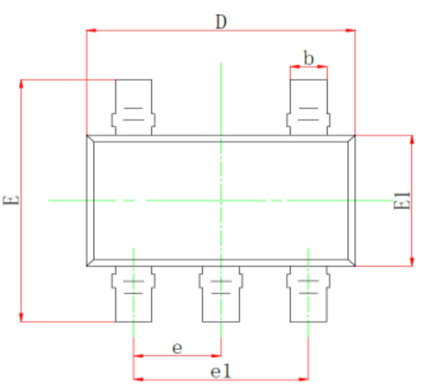


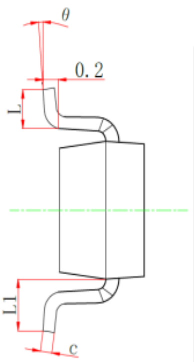
Figure 12. Drive Large Capacitive Load

Package Information

SOT23-5

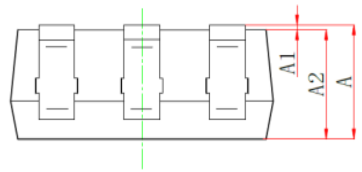


TOP VIEW
[顶视图]



SIDE VIEW
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC.)		0.037(BSC.)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°



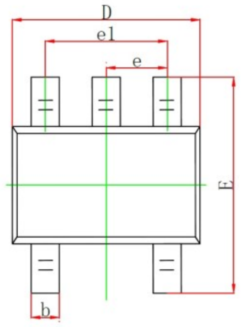
BOTTOM VIEW
[背视图]

Note:
1. All dimensions are in mm. Angels in degrees.
2. Refer Jedec MO-187
3. Dimensions exclude burrs, mold flash or protrusions.

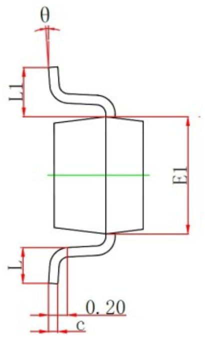
SOT23-5L POD Rev.0

Raystar Microelectronics Technology Inc.

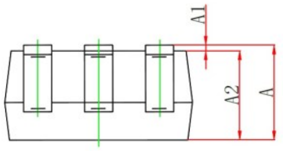
SC70-5



TOP VIEW
[顶视图]



SIDE VIEW
[侧视图]



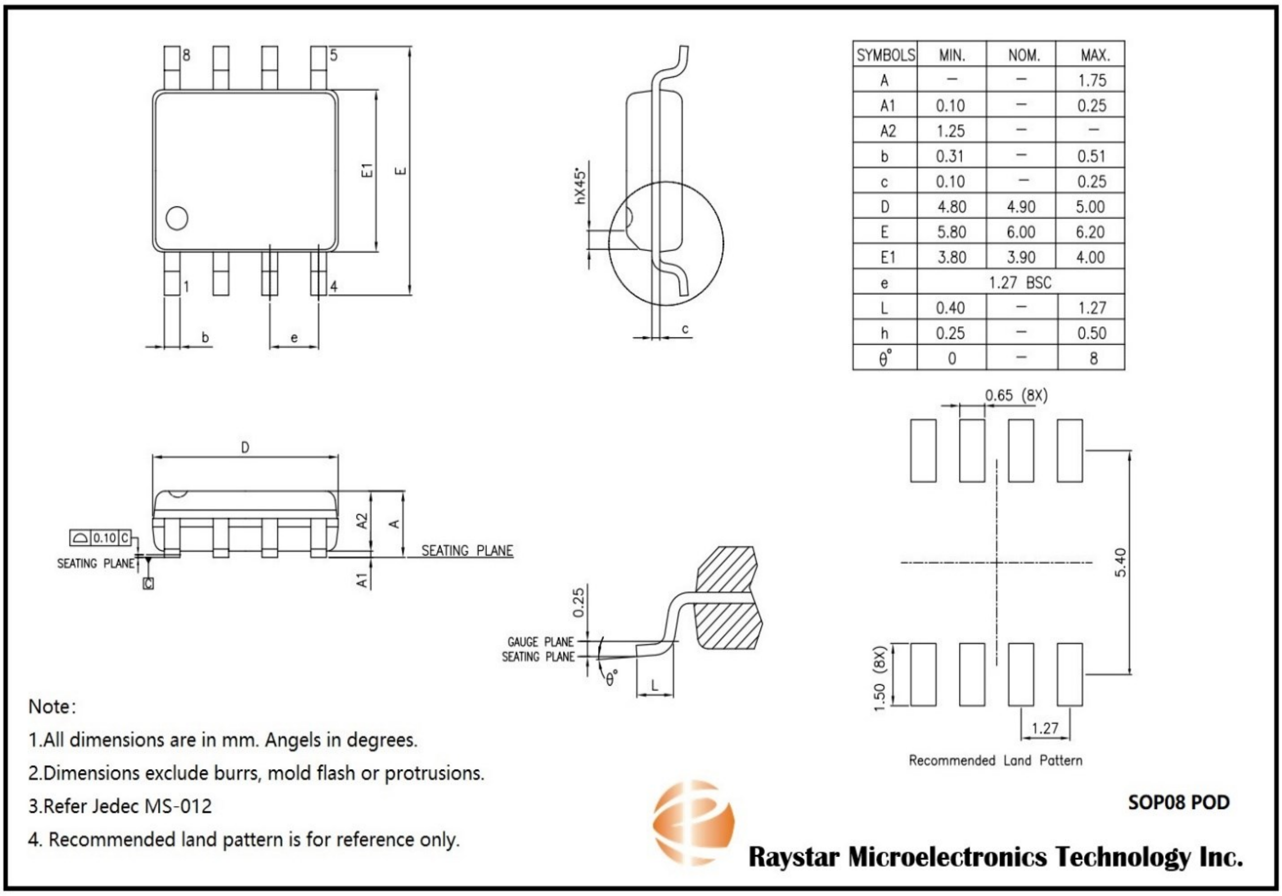
SIDE VIEW
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525 REF.		0.021 REF.	
θ	0°	8°	0°	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-178
3.Dimensions exclude burrs, mold flash or protrusions.

SC70-5L (C05) POD Rev.0
Raystar Microelectronics Technology Inc.

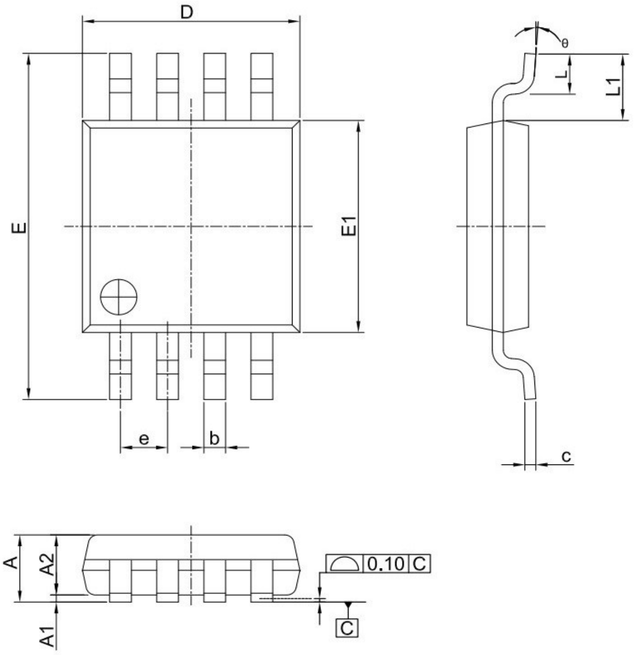
SOP-8



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	—	1.27
h	0.25	—	0.50
θ°	0	—	8

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

MSOP-8

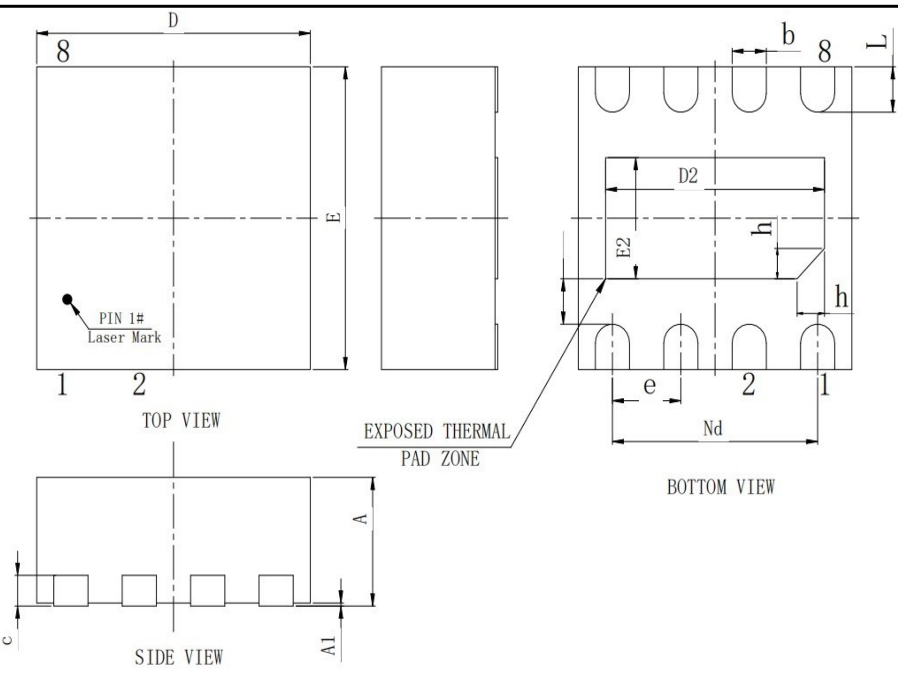


PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-187
3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08 POD Rev.0
Raystar Microelectronics Technology Inc.

DFN2X2-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	1.95	2.00	2.05
D2	1.55	1.60	1.65
Nd	1.50BSC		
e	0.50BSC		
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
L	0.25	0.30	0.35
K	0.25	0.30	0.35
h	0.20REF		

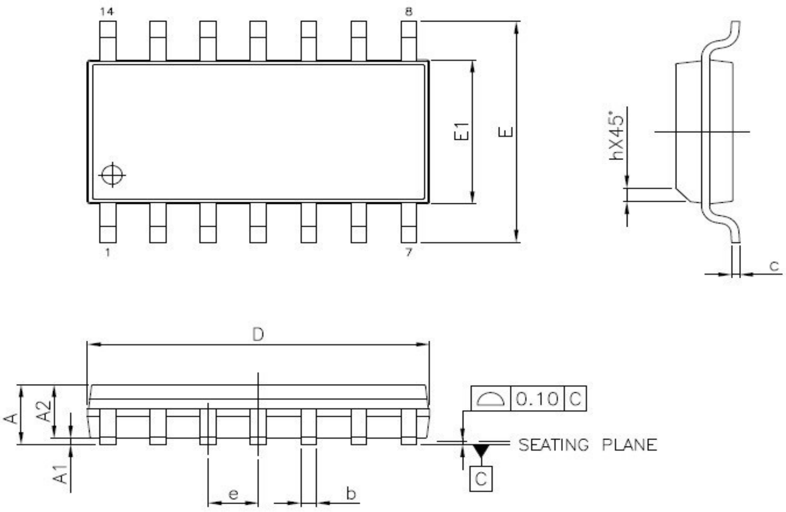
Notes:

1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-229
3. Dimensions exclude burrs, mold flash or protrusions.

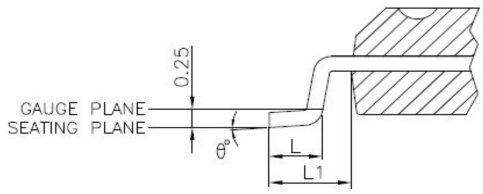
DFN 2X2X0.75-8L(ZA08) POD Rev. A

Raystar Microelectronics Technology Inc.

SOP-14



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e		1.27 BSC	
L	0.40	—	1.27
L1		1.04 REF	
h	0.25	—	0.50
θ°	0	—	8



Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

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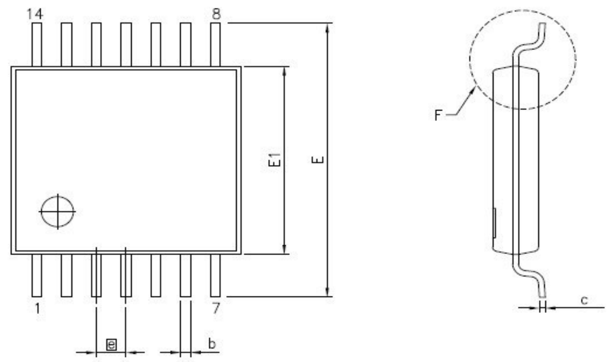
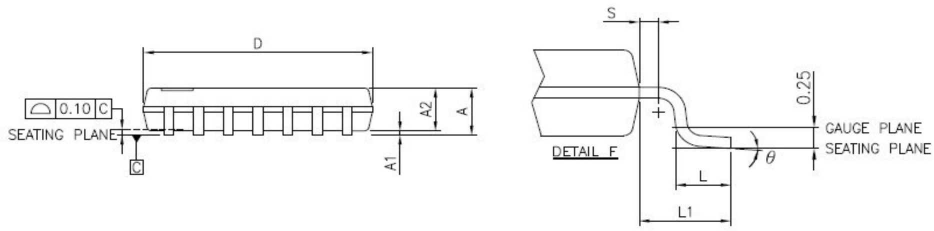


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°



Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MO-153F

4. Recommended land pattern is for reference only.

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Revision History

Revision	Description	Date
V1.0	Initial Release	2024/09/20
V1.1	Added SC70-5 package	2024/11/11