Features

- High-Performance 1:10 Clock Driver
- 12kHz to 20MHz additive phase jitter: 25fs RMS at 125MHz
- Operates up to 200 MHz @ 3.3V
- Pin-to-Pin Skew < 100 ps @ 3.3V
- Output Enable Glitch Suppression outputs
- Distributes One Clock Input to Two Banks of Five Outputs
- 25Ω On-Chip Series Damping Resistors
- -40 to +105°C, 2.3~3.6 V operation
- 4.4 x 7.8mm 24-Pin TSSOP

Applications

- General-Purpose Applications
- Networking
- Telecom system

Description

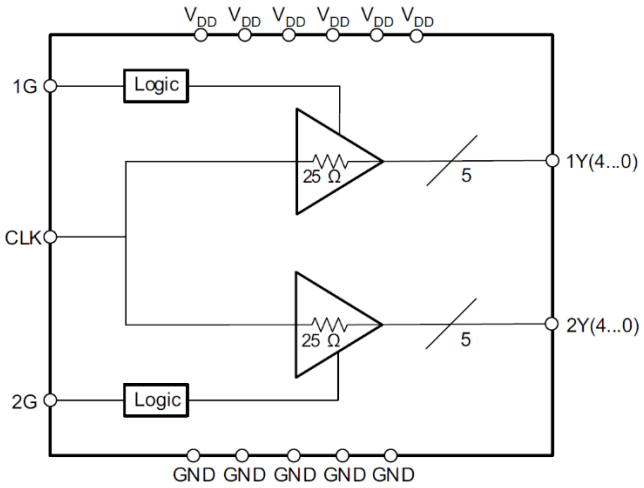
The RS2CB2310 device is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5V and 3.3V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

Ordering Information

Part Number	Package	Description
RS2CB2310LE	TSSOP24	4.4mm × 7.8 mm

Notes:
[1] E = Pb-free and Green

Block Diagram



Pin Configuration

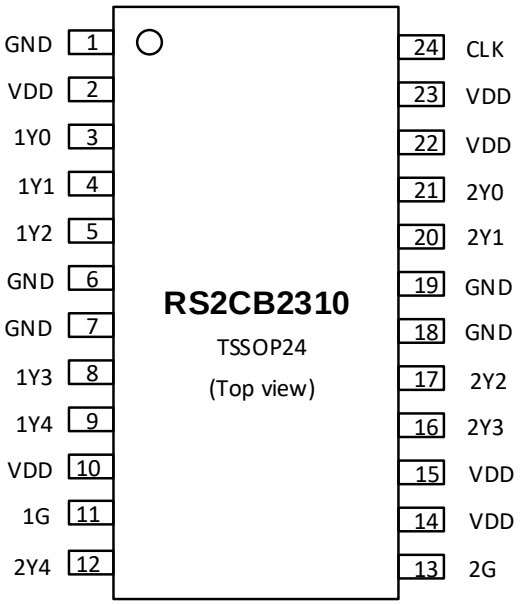


Figure 1. Pin Assignments for 24-Pin TSSOP Package – Top View

Pin Description

Table 1. Pin Descriptions

Pin Name	Number	Type	Description
VDD	2, 10, 14, 15, 22, 23	Power	DC power supply, 2.3 V ~ 3.6 V.
GND	1, 6, 7, 18, 19	GND	Ground
1G	11	I, SE, PD	Output enable control for 2Y[0:4] outputs. 1 = enable output, 0 = disable output.
2G	13	I, SE, PD	Output enable control for 2Y[0:4] outputs. 1 = enable output, 0 = disable output.
CLK	24	I, SE	Single-ended input.
1Y[0:4]	3, 4, 5, 8, 9	O, SE	Bank1,five single-ended outputs. 3.3V/2.5V LVCMOS reference levels.
2Y[0:4]	21, 20, 17, 16, 12	O, SE	Bank2,five single-ended outputs. 3.3V/2.5V LVCMOS reference levels.

Table 2. Signal Types

Term	Description
I	Input
O	Output
PD	Pull-down
PU	Pull-up
SE	Single-ended
Power	Power
GND	Ground

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CB2310 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Supply Voltage	V_{DD}		-0.5		4.6	V	
Input High Voltage	V_{IH}				V_{DD} +0.5	V	2
Input Low Voltage	V_{IL}		-0.5			V	1
Output High Voltage	V_{OH}				V_{DD} +0.5	V	2
Output Low Voltage	V_{OL}		-0.5			V	1
Input clamp current	I_{IK}	$V_I < 0$ or $V_I > V_{DD}$			±50	mA	
Output clamp current	I_{OK}	$V_O < 0$ or $V_O > V_{DD}$			±50	mA	
Continuous total output current	I_O	V_O = 0 to V_{DD}			±50	mA	
Storage Temperature	T_S		-65		150	°C	
Junction Temperature	T_J	Maximum operating junction temperature.			125	°C	
Input ESD Protection	ESD	Human Body Model.			2000	V	
		Charged-device Model			1000	V	

1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Supply Voltage	V_{DD}		2.3	2.5		V	
				3.3	3.6		
Input High Voltage	V_{IH}	V_{DD} = 3 V to 3.6 V	2			V	
		V_{DD} = 2.3 V to 2.7 V	1.7				
Input Low Voltage	V_{IL}	V_{DD} = 3 V to 3.6 V			0.8	V	
		V_{DD} = 2.3 V to 2.7 V			0.7		
Output High Current	I_{OH}	V_{DD} = 3 V to 3.6 V			12	mA	
		V_{DD} = 2.3 V to 2.7 V			6		
Output Low Current	I_{OL}	V_{DD} = 3 V to 3.6 V			12	mA	
		V_{DD} = 2.3 V to 2.7 V			6		
Operating Temperature	T_A		-40		85	°C	

1. The unused input must be held high or low to prevent them from floating.

Electrical Characteristics

TA = TAMB. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 6. DC Characteristics

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units	Notes
Input Voltage	V_{IK}	V_{DD} = 3 V	I_I = –18 mA			-1.2	V	1
Input Current	I_I	V_I = 0 to V_{DD}				±5	µA	
Static Device Current	I_{DD}	CLK = 0 V or V_{DD} ,I_O = 0 mA	-40°C to 85°C			90	µA	
			≤105°C			100	µA	
Input Capacitance	C_I	V_{DD} = 2.3 V to 3.6 V	V_{DD} = 2.3 V to 3.6 V		2.5		pF	
Output Capacitance	C_O	V_{DD} = 2.3 V to 3.6 V	V_I = 0 to V_{DD}		2.8		pF	
V_{DD} = 3.3 V ±0.33 V								
Output High Voltage	V_{OH}	V_{DD} = min to max	I_{OH} = -100µA	V_{DD}-0.2			V	
		V_{DD} = 3 V	I_{OH} = -12mA	2.1				
			I_{OH} = -6mA	2.4				
Output Low Voltage	V_{OL}	V_{DD} = min to max	I_{OL} = -100µA			0.2	V	
		V_{DD} = 3 V	I_{OL} = 12mA			0.8		
			I_{OL} = 6mA			0.55		
Output High Current	I_{OH}	V_{DD} = 3 V	V_O = 1 V	-28			mA	
		V_{DD} = 3.3 V	V_O = 1.65 V		-36			
		V_{DD} = 3.6V	V_O = 3.135 V			-14		
Output Low Current	I_{OL}	V_{DD} = 3 V	V_O = 1.95 V	28			mA	
		V_{DD} = 3.3 V	V_O = 1.65 V		36			
		V_{DD} = 3.6V	V_O = 0.4 V			14		

1. All typical values are at respective nominal V_{DD}.

Table 6. DC Characteristics (continued)

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units	Notes
V_{DD} = 2.5 V ±0.25 V								
Output High Voltage	V_{OH}	V_{DD} = min to max	I_{OH} = -100µA	V_{DD}-0.2			V	
		V_{DD} = 2.3 V	I_{OH} = -6mA	1.8				
Output Low Voltage	V_{OL}	V_{DD} = min to max	I_{OH} = 100µA			0.2	V	
		V_{DD} = 2.3 V	I_{OH} = 6mA			0.55		
Output High Current	I_{OH}	V_{DD} = 2.3 V	V_o = 1 V	-17			mA	
		V_{DD} = 2.5 V	V_o = 1.25 V		-25			
		V_{DD} = 2.7V	V_o = 2.375 V			-10		
Output Low Current	I_{OL}	V_{DD} = 2.3 V	V_o = 1.2 V	17			mA	
		V_{DD} = 2.5 V	V_o = 1.25 V		25			
		V_{DD} = 2.7V	V_o = 0.3 V			10		

Table 7. AC Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Clock Frequency	f_{clk}	V_{DD} = 3V to 3.6V	0		200	MHz	
		V_{DD} = 2.3V to 2.7V	0		170		
V_{DD} = 3.3 V ±0.33 V							
CLK to Yn	t_{PLH}	f = 0 MHz to 200 MHz For circuit load, see Figure 3.	1.3		2.8	ns	
	t_{PHL}						
Output skew (Ym to Yn) (see Figure 5)	$t_{sk(o)}$				100	ps	1
Pulse Skew (see Figure 6)	$t_{sk(p)}$				250		
Part-to-Part skew	$t_{sk(pp)}$				500		
Rise Time (see Figure 4)	t_r	V_O = 0.4V to 2V	0.7		2.5	V/ns	
Fall Time (see Figure 4)	t_f	V_O = 2V to 0.4V	0.7		2.5		
Enable setup time, G_high before CLK	$t_{su(en)}$		0.1			ns	
Disable setup time, G_low before CLK	$t_{su(dis)}$		0.1				
Enable hold time, G_high after CLK	$t_{h(en)}$		0.4				
Disable hold time, G_low after CLK	$t_{h(dis)}$		0.4				

1. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

Table 7. AC Characteristics (continued)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
V_{DD} = 2.5 V ±0.25 V							
CLK to Yn	t_{PLH}	f = 0 MHz to 170 MHz For circuit load, see Figure 3.	1.5		3.5	ns	
	t_{PHL}						
Output Skew (Ym to Yn) (see Figure 5)	$t_{sk(o)}$				170	ps	1
Pulse Skew (see Figure 6)	$t_{sk(p)}$				400		
Part-to-Part Skew	$t_{sk(pp)}$				600		
Rise Time (see Figure 4)	t_r	V_o = 0.4V to 1.7V	0.5		1.8	V/ns	
Fall Time (see Figure 4)	t_f	V_o = 1.7V to 0.4V	0.5		1.8		
Enable setup time, G_high before CLK	$t_{su(en)}$		0.1			ns	
Disable setup time, G_low before CLK	$t_{su(dis)}$		0.1				
Enable hold time, G_high after CLK	$t_{h(en)}$		0.4				
Disable hold time, G_low after CLK	$t_{h(dis)}$		0.4				

1. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

Table 8. Jitter Characteristics

Characterized using RS2CB2310 Performance EVM when VDD= 3.3 V. Outputs not under test are terminated to 50 Ω.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Additive phase jitter	t_{jitter}	12 kHz to 5 MHz, f_{out} = 50 MHz		55		fs rms	
		12 kHz to 20 MHz, f_{out} = 125 MHz		25			

Typical Characteristics

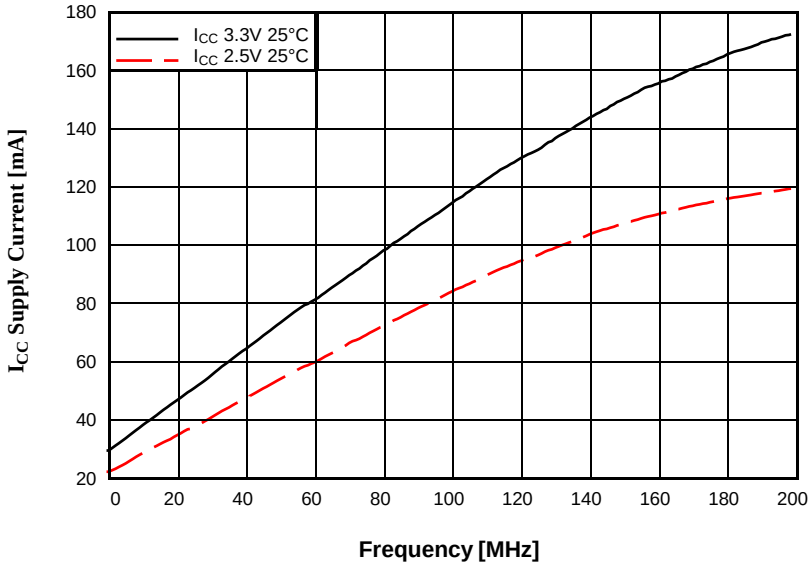
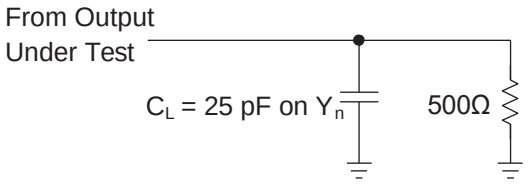


Figure 2. Supply Current vs Frequency

Test Information



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.

Figure 3. Test Load Circuit

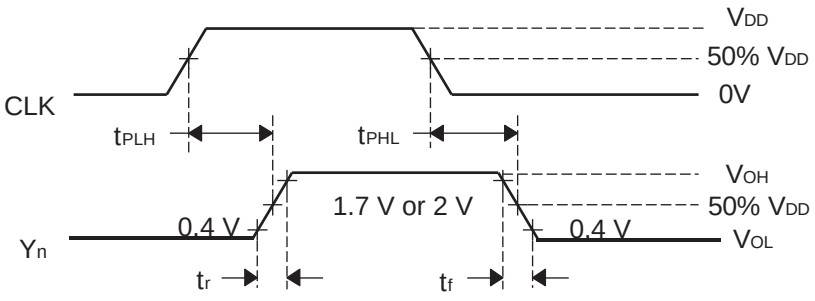


Figure 4. Voltage Waveforms Propagation Delay Times

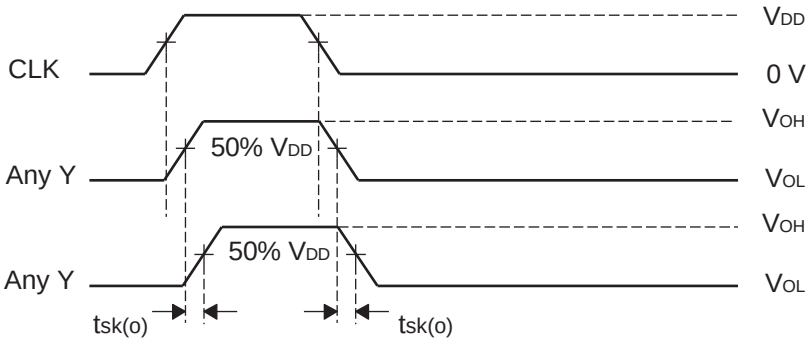
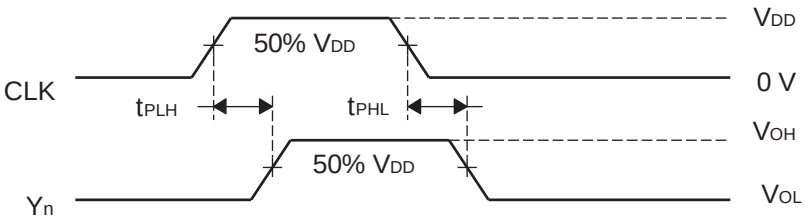


Figure 5. Output Skew



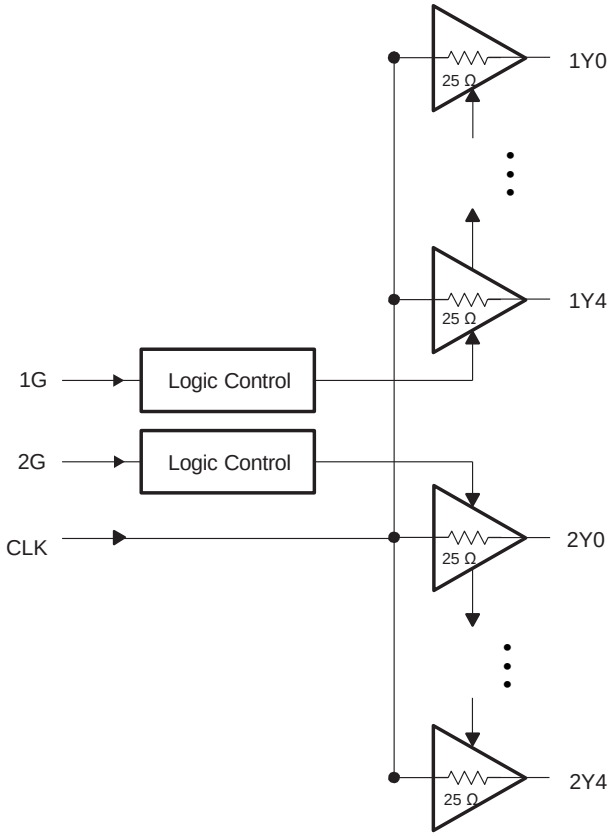
NOTE: $t_{sk(p)} = | t_{PLH} - t_{PHL} |$

Figure 6. Pulse Skew

Detailed Description

The RS2CB2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5V and 3.3V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

Functional Block Diagram

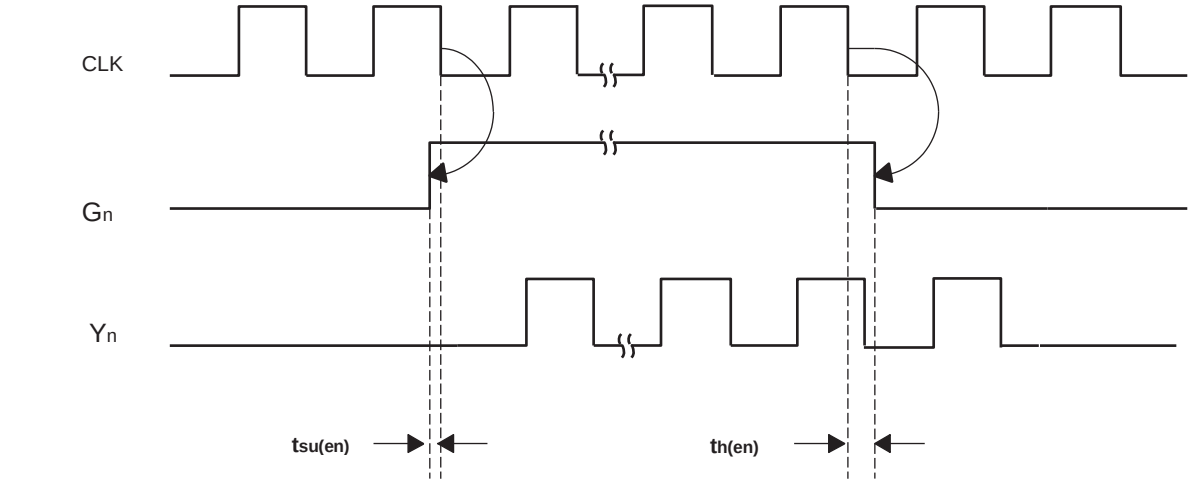


Feature Description

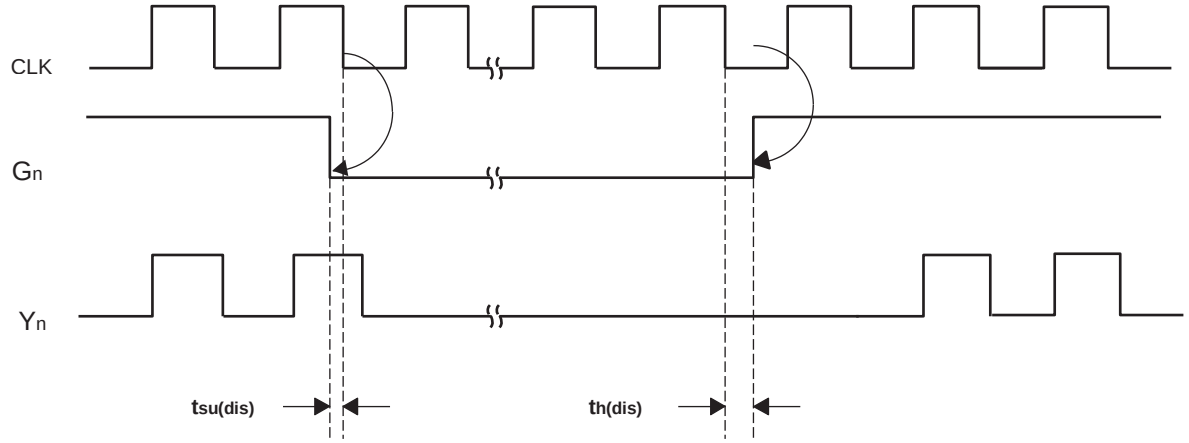
Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 7).

The G input must fulfill the timing requirements (tsu, th) according to the Switching Characteristics table for predictable operation.



a) Enable Mode



b) Disable Mode

Figure 7. Enable and Disable Mode Relative to CLK

Device Functional Modes

Table 9 lists the functional modes for the RS2CB2310.

Table 9. Function Table

INPUT			OUTPUT	
1G	**2G**	**CLK**	**1Y[0:4]**	**2Y[0:4]**
L	L	↓	L	L
H	L	↓	CLK(1)	L
L	H	↓	L	CLK(1)
H	H	↓	CLK(1)	CLK(1)

(1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Application Information

The RS2CB2310 is a LVCMOS buffer solution that can operate up to 200 MHz. Low output skew as well as the ability for glitchless output enable and disable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application. The following design is typical applications.

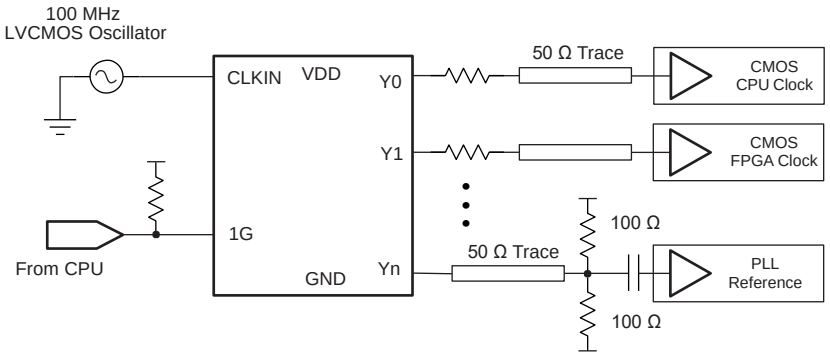


Figure 8. Example System Configuration

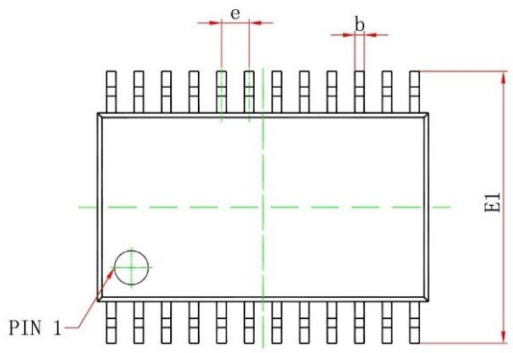
NOTE:Refer to *Electrical Characteristics* table to determine the appropriate series resistance needed for matching the output impedance of the RS2CB2310 to that of the characteristic impedance of the transmission line.

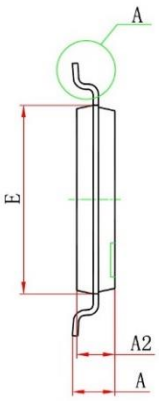
The RS2CB2310 shown in Figure 8 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.
The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

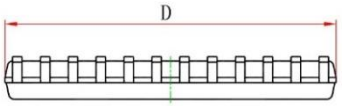
- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the RS2CB2310 to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the RS2CB2310.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC-coupling can be used when common-mode voltage is mismatched.

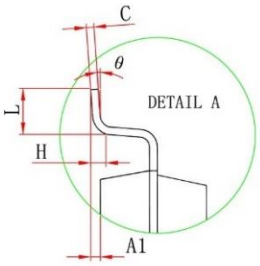
Package Information

TSSOP_24-Pin









Symbol	Dimensions In Millimeters	
	Min	**Max**
D	7.700	7.900
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A		1.200
A2	0.800	1.000
A1	0.050	0.150
e	0.65 (BSC)	
L	0.500	0.700
H	0.25(TYP)	
θ	1°	7°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012

TSSOP24 POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary release	2024/05/23
1.0	Initial release	2024/10/11