## Features

- 3.3V Supply Voltage
- Crystal/CMOS Input: 25 MHz
- Four Differential Low-Power HCSL Outputs with On-Chip Termination
- Default ZOUT = 85Ω
- Two reference LVCMOS Outputs
- Programmable Slew Rate and Output Amplitude for Each Differential Output
- Selectable 0%, -0.3%, or -0.5% Spread on Differential Outputs
- Differential Output-to-Output Skew <50ps
- Very-Low phase Jitter for Differential Outputs
  < 0.3ps RMS, SSC off
  < 1.5ps RMS, SSC on
- LOS (Loss-Of-Signal) indication Clock input
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device
- Available in TQFN-32L package
- -40 to +85°C temperature operation

## Applications

- Cloud/High-performance Computing
- nVME Storage
- In-Vehicle Networking
- Automotive infotainment

## Description

The RS2CG286 is a 4 differential LP-HCSL Outputs and 2 LVCMOS outputs, very-low-power PCIe Gen1/ Gen2/Gen3/Gen4/Gen5 clock generator.

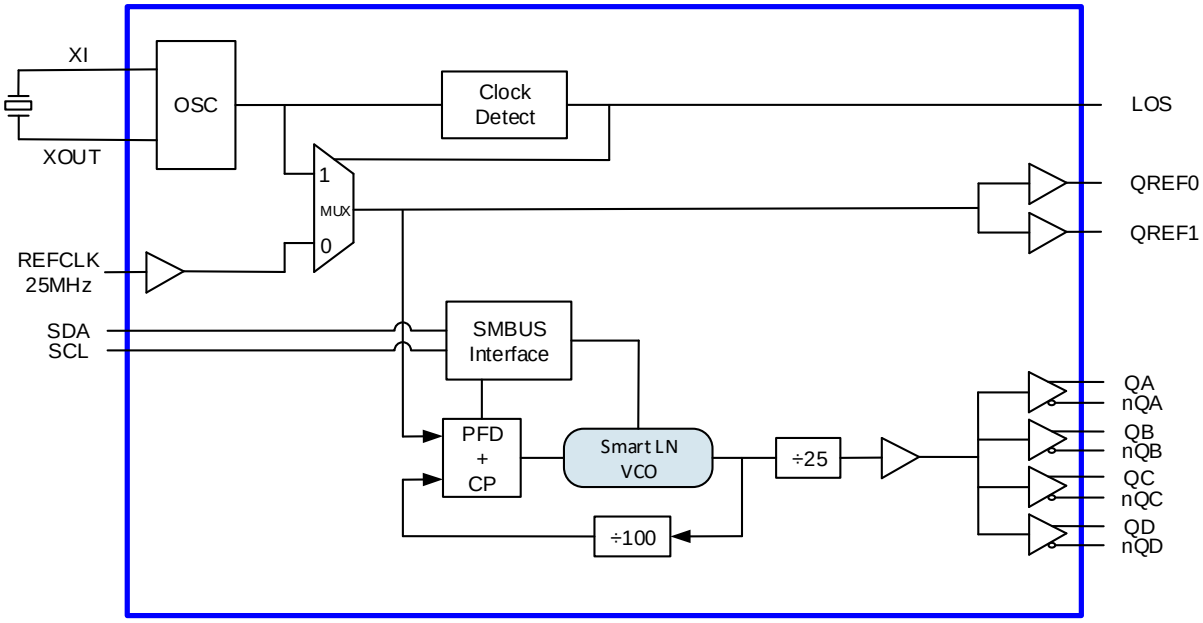
It uses a 25MHz crystal or CMOS reference as an input to generate the 100MHz low-power differential LP-HCSL outputs with on-chip terminations and the 25MHz LVCMOS buffered reference Single-ended outputs that are provided to serve as a low-noise reference for other circuitry.

It uses RSM's proprietary PLL design to achieve very-low jitter that meets PCIe Gen1~Gen5 requirements. It also provides various options, such as different slew rate and amplitude through SMBus, so users can easily configure the device to get the optimized performance. The device also supports selectable spread spectrum options to reduce EMI for various applications.

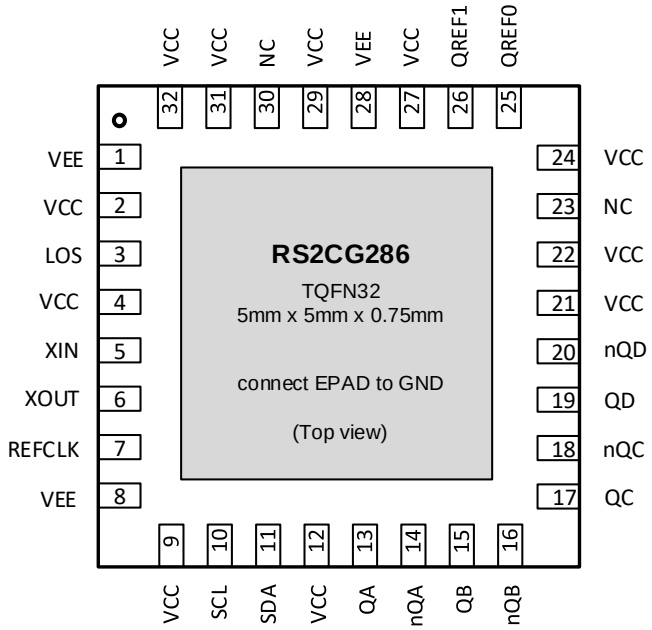
## Order information

| Part Number | Package | Description |
|---|---|---|
| RS2CG286ZHE | ZH | TQFN_32L_5mmx5mm |

## Functional Block Diagram




## Pin Configuration



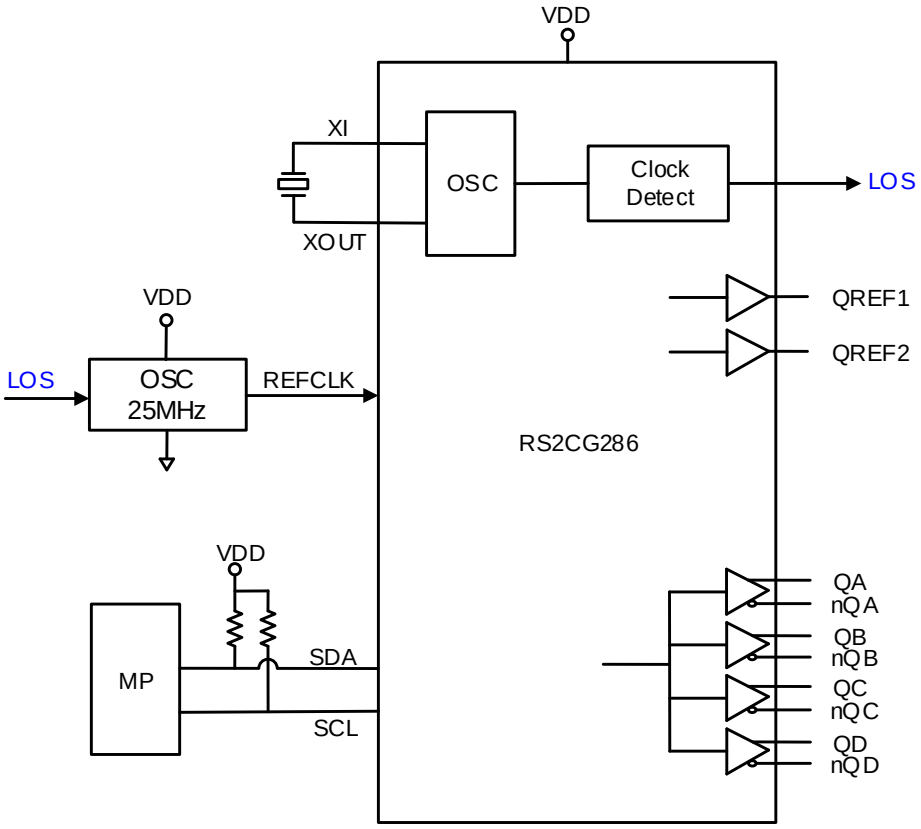
## Pin Descriptions

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1, 8, 28 | VEE | Power | Negative supply pins (GND). |
| 2,4,9, 12,21,22,24,27,29,31,32 | VCC | Power | Pins 2, 24, 27 – Power supply for the 25MHz LVCMOS outputs<br>Pin 4 –Power supply for the crystal oscillator<br>Pin 9,12,21,22 –Power supply for the LP-HCSL differential outputs<br>Pins 29 –Power supply for the divider<br>Pin 31,32 –Power supply for the PLL |
| 3 | LOS | Output | Output indicating Loss of Input Signal. This pin is a TTL output. A high output on this pin indicates a loss of signal on XTAL input clock. |
| 25,26 | QREF0, QREF1 | Output | Single-ended outputs. 3.3V LVCMOS/LVTTL reference levels. |
| 5 | XIN | Input | Parallel resonant crystal interface. XTAL_IN is the input. |
| 6 | XOUT | Output | Parallel resonant crystal interface. XTAL_OUT is the output, |
| 7 | REFCLK | Input | Single-ended LVCMOS/LVTTL reference clock input. |
| 10,11 | SCL, SDA | I/O | SMBus communication interface |
| 23,30 | NC | NC | No connect. |
| 13,14 | QA, nQA | Output | ±0.8V Differential LP-HCSL interface levels |
| 15,16 | QB, nQB | Output | ±0.8V Differential LP-HCSL interface levels |
| 17,18 | QC, nQC | Output | ±0.8V Differential LP-HCSL interface levels |
| 19,20 | QD, nQD | Output | ±0.8V Differential LP-HCSL interface levels |

## Pin Characteristics

| Symbol | Parameter | | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | Crystal Not Included | | 2 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | QREF [0:1] | $V_{CC}$ = 3.6V | | 6 | | pF |
| $R_{PU}$ | Input Pullup Resistor | | | | 51 | | kΩ |
| $R_{PD}$ | Input Pulldown Resistor | | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | QREF [0:1] | | | 33 | | Ω |

## Typical Application Circuit




**Notes:**

1. The LOS signal can be used to enable or disable the external OSC.

## Absolute Maximum Ratings

| Symbol | Parameter | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| VDD | Supply Voltage to Ground Potential | -0.5 | - | 4.6 | V |
| $V_{IO}$ | Input / Output Voltage | -0.5 | - | VDD+0.5 | V |
| $V_{IH}$ | SMBUS Input High Voltage | | | 3.6 | V |
| $T_J$ | Junction Temperature | | | 125 | °C |
| $T_{store}$ | Storage Temperature | −65 | - | +150 | °C |
| ESD | ESD HBM protection (input) | | | 4000 | V |

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

| Symbol | Parameter | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| VDD | Power Supply Voltage | 3.0 | | 3.6 | V |
| $V_{IH}$ | Input Voltage on REFCLK, SCL, SDA | | | 3.6 | V |
| $T_A$ | Ambient air temperature | -40 | | +85 | °C |

## DC Electrical Characteristics

**Table 3. Power Supply DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 85°C.**

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| VCC | Power Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| ICC | Power Supply Current | No Load | | | 200 | mA |

**Table 4. LVCMOS DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 85°C.**

| Symbol | Parameter | | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| IIH | Input High Current | REFCLK | VCC = VIN = 3.6V | | | 150 | µA |
| IIL | Input Low Current | REFCLK | VCC = 3.6V, VIN = 0V | -5 | | | µA |
| VOH | Output High Voltage; | | VCC = 3.3V ± 0.3V | 2.3 | | | V |
| VOL | Output Low Voltage; | | VCC = 3.3V ± 0.3V | | | 0.8 | V |

**Table 5. LP-HCSL DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 85°C.**

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| VOH | Output High Voltage; | | 660 | | 850 | mV |
| VOL | Output Low Voltage; | | -150 | | 150 | mV |
| Vomax | Output Maximum Voltage; | | | 820 | 1150 | mV |
| Vomin | Output Minimum Voltage; | | -300 | -42 | | mV |
| Voc | Output Cross Voltage; | | 250 | 380 | 550 | mV |

**Table 6. Crystal Characteristics**

| Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

## AC Electrical Characteristics

**Table 7. LP-HCSL AC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 85°C.**

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | | | 25 | | MHz |
| $f_{OUT}$ | Output Frequency | LP-HCSL | | 100 | | MHz |
| $T_{jc-c}$ | Cycle to cycle Jitter | | | 20 | 60 | ps |
| tsk(o) | Output Skew; NOTE 2, 3 | Measured on the Rising Edge | | | 50 | ps |
| $t_R$ / $t_F$ | Slew rate | +/-150mV window | | 3 | | V/ns |
| ODC | Output Duty Cycle | | 45 | | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

**Table 8. AC Characteristics for Single Side Band Power Levels (LP-HCSL Outputs),VCC = 3.3V ± 0.3V, VEE = 0V, TA = 25°C.**

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| tjPHASE | Integrated Phase Jitter (RMS) | PCIe Gen 1 | - | 25 | 86 | ps |
| | | PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz | - | 0.9 | 3.0 | ps |
| | | PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz) | - | 1.6 | 3.1 | ps |
| | | PCIe Gen3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | - | 0.5 | 1 | ps |
| | | PCIe Gen3 Separate Reference No Spread (PLL BW of 2-4 or 2-5MHz, CDR=10 MHz) | - | 0.5 | 0.7 | ps |
| | | PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | - | 0.37 | 0.5 | ps |
| | | PCIe Gen 5(7) (PLL BW of 500k to 1.8MHz. CDR = 20MHz) | - | 0.05 | 0.15 | ps |
| tjPH-SRISG2 | Integrated Phase Jitter (RMS), -0.3%Spread | PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz) | - | 0.92 | 2 | ps |
| tjPH-SRISG3 | Integrated Phase Jitter (RMS), -0.3% Spread | PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz, CDR=10MHz) | - | 0.4 | 0.7 | ps |
| tjPH-SRISG2 | Integrated Phase Jitter (RMS), -0.5% Spread | PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz) | - | 1.1 | 2 | ps |
| tjPH-SRISG3 | Integrated Phase Jitter (RMS), -0.5% Spread | PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz, CDR=10MHz) | - | 0.6 | 0.7 | ps |

**Table 9. LVCMOS AC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 85°C.**

| Symbol | Parameter | | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | | | | 25 | | MHz |
| $f_{OUT}$ | Output Frequency | | | | 25 | | MHz |
| tjit | RMS Phase Jitter (Random) | | 25MHz $f_{OUT}$, 25MHz crystal Integration Range: 12kHz – 5MHz | | 0.140 | | ps |
| *t*sk(o) | Output Skew; | QREF [0:1] | Measured on the Rising Edge | | | 50 | ps |
| PSNR | Power Supply Noise Reduction | Pin 40, ($V_{CC}$) | From DC to 6.25MHz | | -80 | | dB |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% to 80% | | 1.0 | 1.5 | ns |
| ODC | Output Duty Cycle | | | 45 | | 55 | % |

**Table 10. AC Characteristics for Single Side Band Power Levels (LVCMOS Outputs), VCC = 3.3V ± 0.3V, VEE = 0V, TA = 25°C.**

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $\varphi_N$(1k) | Single-side band phase noise, 1kHz from Carrier | 25MHz | | -137 | | dBc/Hz |
| $\varphi_N$(10k) | Single-side band phase noise, 10kHz from Carrier | | | -153 | | dBc/Hz |
| φ(100k) | Single-side band phase noise, 100kHz from Carrier | | | -162 | | dBc/Hz |
| $\varphi_N$(1M) | Single-side band phase noise, 1MHz from Carrier | | | -163 | | dBc/Hz |
| $\varphi_N$(5M) | Single-side band phase noise, 5MHz from Carrier | | | -163 | | dBc/Hz |

## SMBus Serial Data Interface

RS2CG286 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below. Read and write block transfers can be stopped after any complete byte transfer.

**Table 11. Address Assignment**

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0/1 |

**Table 12. How to Write**

| 1 bit | 7 bit | 1 bit | 1 bit | 8 bit | 1 bit | 8 bit | 1 bit | 8 bit | 1 bit | | 8 bit | 1 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Add. | W(0) | Ack | Beginning Byte location = N | Ack | Data Byte count=X | Ack | Beginning Data Byte (N) | Ack | …… | Data Byte (N+X- 1) | Ack | Stop bit |

**Table 13. How to Read**

| 1 bit | 7 bit | 1 bit | 1 bit | 8 bit | 1 bit | 1 bit | 7 bit | 1 bit | 1 bit | 8 bit | 1 bit | 8 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Add. | W(0) | Ack | Beginning Byte location = N | Ack | Repeat Start bit | Add. | R(1) | Ack | Data Byte count = X | Ack | Beginning Data Byte (N) | Ack |

| | 8 bit | 1 bit | 1 bit |
|---|---|---|---|
| …….. | Data Byte (N+X-1) | NAck | Stop bit |

**Table 14. Output Enable Control 0**

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 1 |
| Bit 6 | Reserved | | RW | | | 1 |
| Bit 5 | Reserved | | RW | | | 1 |
| Bit 4 | Reserved | | RW | | | 1 |
| Bit 3 | OE_OUTA | | RW | Disable Output | Enable Output | 1 |
| Bit 2 | OE_OUTB | | RW | Disable Output | Enable Output | 1 |
| Bit 1 | OE_OUTC | | RW | Disable Output | Enable Output | 1 |
| Bit 0 | OE_OUTD | | RW | Disable Output | Enable Output | 1 |

**Table 15. Output status Control 1**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | SLEW RATE OF HCSL | HCSL SLEW RATE CONTROL | RW | Slow setting | Fast setting | 0 |
| Bit 6 | STOP1 | HCSL Stop Mode Control | RW | 00= Low / Low<br>01= HIZ / HIZ<br>10= High / Low<br>11= Low / High | | 0 |
| Bit 5 | STOP0 | | | | | 0 |
| Bit 4 | HCSL PD | HCSL PD MODE | RW | Normal | PD | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | REF HIZ | Output REF CMOS HIZ MODE | RW | 0=Normal | 1=REF HIZ | 0 |

**Table 16. Reserved**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 17. Reserved**

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 18. Reserved**

| Byte 4 | Name | | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 19. Reserved**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 20. Reserved**

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 21. Reserved**

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 22. Vendor/Revision Identification Control**

| Byte 8 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | RID3 | Revision ID | R | Rev A = 0000 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | Vendor ID | R | RSM = 0011 | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 1 |
| Bit 0 | VID0 | | R | | | 1 |

**Table 23. Device ID Control**

| Byte 9 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | DID7 | | R | | | 0 |
| Bit 6 | DID6 | | R | | | 0 |
| Bit 5 | DID5 | Device ID | R | | | 0 |
| Bit 4 | DID4 | | R | | | 0 |
| Bit 3 | DID3 | | R | | | 0 |
| Bit 2 | DID2 | | R | | | 1 |
| Bit 1 | DID1 | | R | | | 1 |
| Bit 0 | DID0 | | R | | | 1 |

**Table 24. Byte Count Control**

| Byte 10 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | BC5 | Writing to this register configures how many bytes will be read back | RW | Default value is 8 | | 0 |
| Bit 4 | BC4 | | RW | | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

**Table 25. Reserved**

| Byte 11 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 26. Reserved**

| Byte 12 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 27. Reserved**

| Byte 13 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 28. Reserved**

| Byte 14 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 29. Reserved**

| Byte 15 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 30. Reserved**

| Byte 16 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 31. Reserved**

| Byte 17 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 32. Reserved**

| Byte 18 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | Write not allowed | RW | | | 0 |
| Bit 6 | Reserved | Write not allowed | RW | | | 1 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 33. Reserved**

| Byte 19 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | Reserved | | RW | | | 0 |
| Bit 5 | Reserved | | RW | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

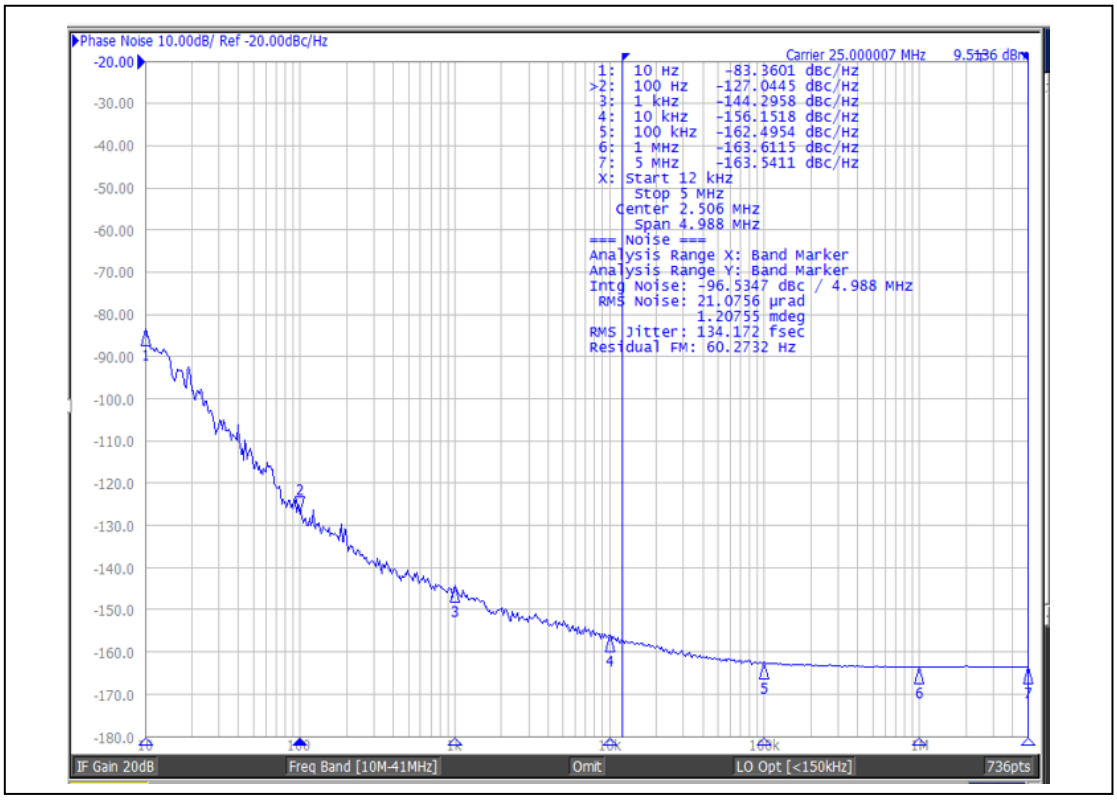
**Table 34. SSC Control**

| Byte 20 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | RW | | | 0 |
| Bit 6 | SSC_DIV6 | SSC clk divider ratio = N*2+1<br>Fssc = Fpfd_FB / (N*2+1) /12<br>B20[1] is RO/RW when B20[7]=0/1 | RW | Divide ratio = decimal value x 2 + 1 | | 1 |
| Bit 5 | SSC_DIV5 | | RW | | | 0 |
| Bit 4 | SSC_DIV4 | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | | RW | | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Table 35. SSC and EFUSE Control**

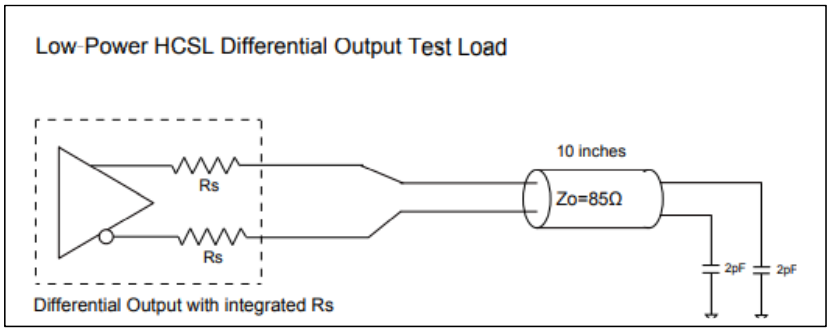
| Byte 21 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | SSC_PD | SSC block power down valid if CG is SSC mode | RW | Normal | Power down | 0 |
| Bit 6 | SSC_EN_SW1 | SSC_EN SW contol | RW | 00 = SSC off<br>01 = -0.3% SS<br>10 = -0.3% SS<br>11 = -0.5% SS | | 0 |
| Bit 5 | SSC_EN_SW0 | | | | | 0 |
| Bit 4 | Reserved | | RW | | | 0 |
| Bit 3 | Reserved | | RW | | | 0 |
| Bit 2 | Reserved | | RW | | | 0 |
| Bit 1 | Reserved | Write not allowed | RW | 00 = ACCESS0 / ACCESS0<br>01 = RE / PEB<br>10 = OUTPUT1 / ACCESS1<br>11 = OUTPUT0 / ADDR0 | | 0 |
| Bit 0 | Reserved | | RW | | | 0 |

**Plots 25MHz LVCMOS Clock (12k to 5MHz)**

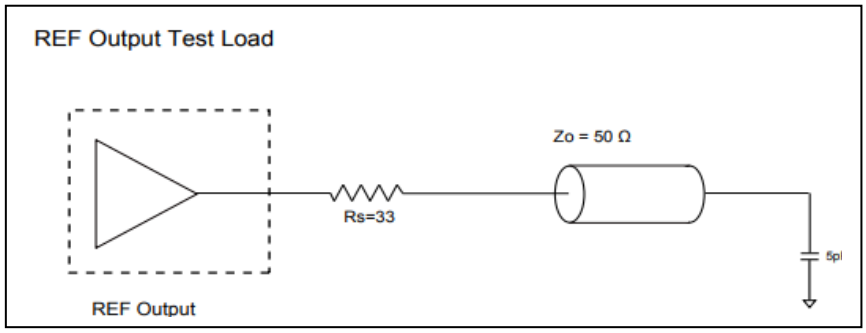


# Typical Test Circuit

### Low-Power HCSL Test Circuit




### CMOS REF Test Circuit




### Differential Output Driving LVDS

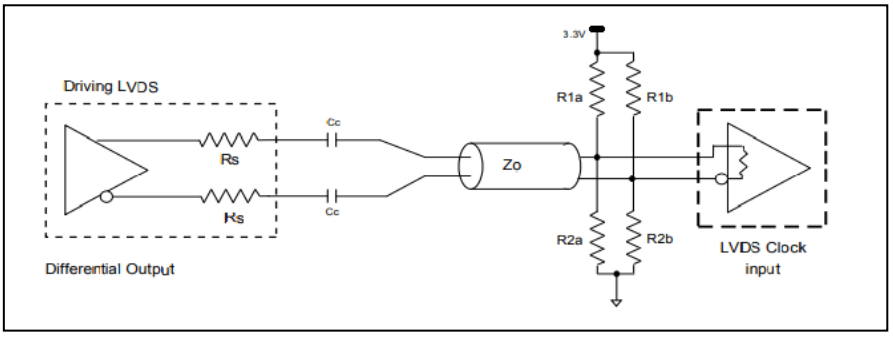


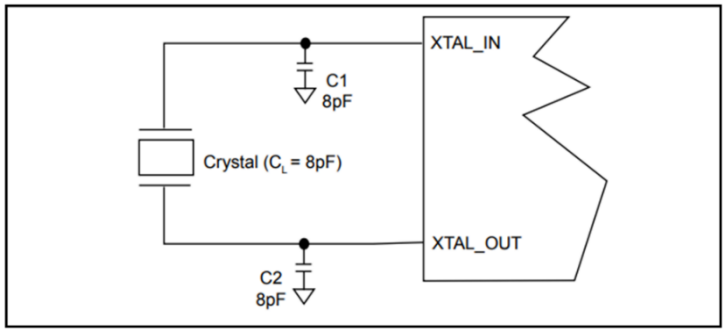

**Table 36. Alternate Differential Output Terminations (Zo = 85Ω).**

| Component | Receiver with Termination | Receiver without Termination | Unit |
|---|---|---|---|
| R1a, R1b | 10,000 | 130 | Ω |
| R2a, R2b | 5600 | 64 | Ω |
| $C_C$ | 0.1 | 0.1 | uF |
| $V_{CM}$ | 1.2 | 1.2 | V |

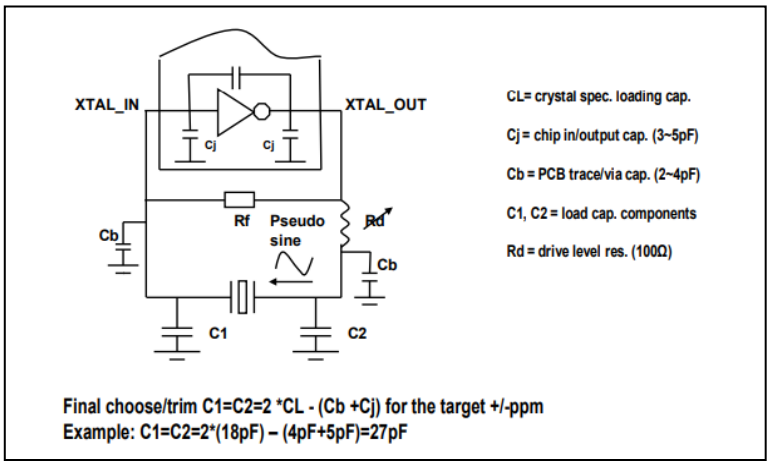
## Crystal Circuit Connection

The following diagram shows RS2CG286 crystal circuit connection with a parallel crystal. For the $C_L$=8pF crystal, it is suggested to use C1=8pF and C2=8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

### Crystal Oscillator Circuit

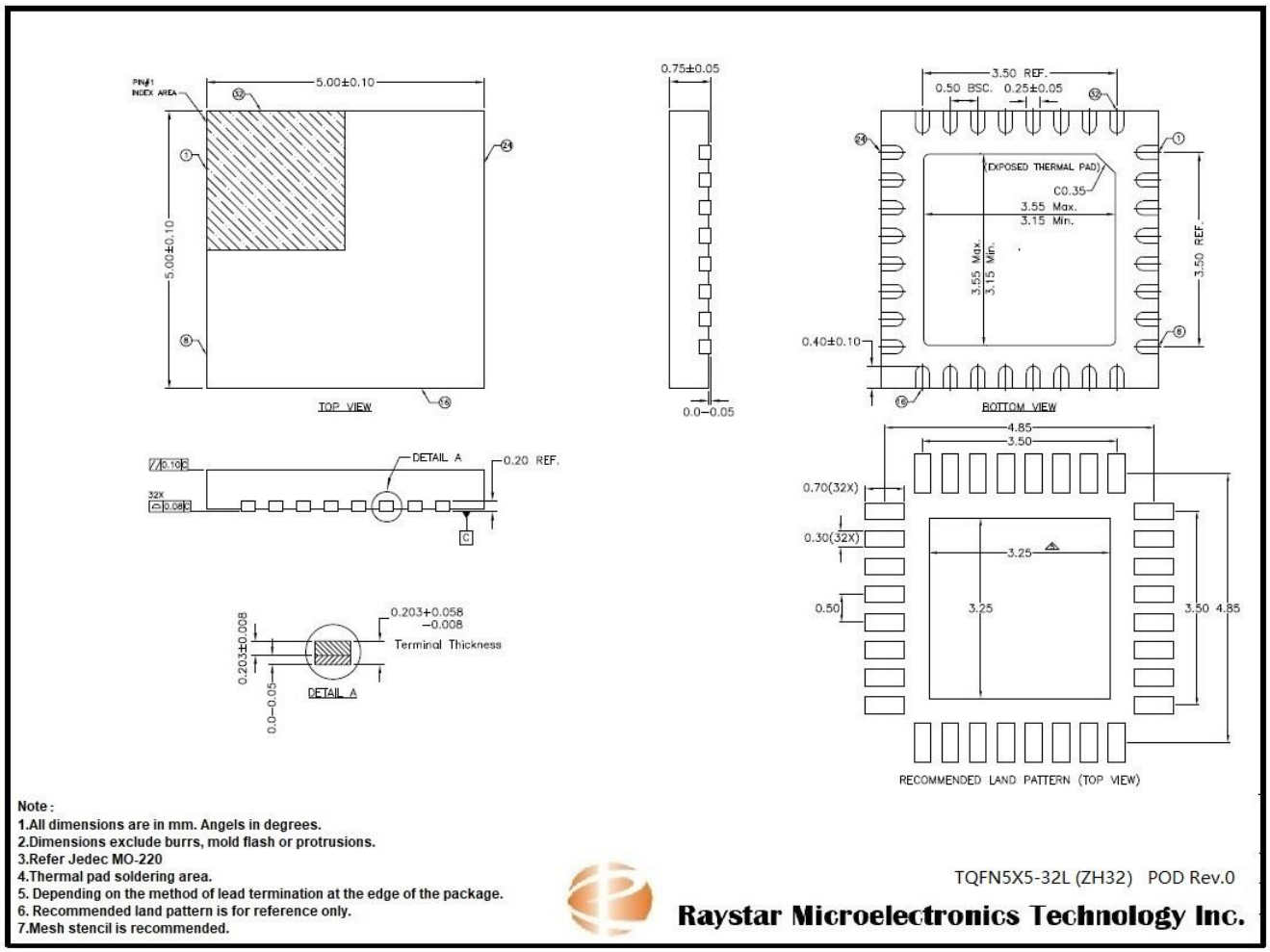



### Crystal Capacitor Calculation



# Package Information

## TQFN-32L (ZH32)




**Note :**
**1.All dimensions are in mm. Angels in degrees.**
**2.Dimensions exclude burrs, mold flash or protrusions.**
**3.Refer Jedec MO-220**
**4.Thermal pad soldering area.**
**5. Depending on the method of lead termination at the edge of the package.**
**6. Recommended land pattern is for reference only.**
**7.Mesh stencil is recommended.**

TQFN5X5-32L (ZH32) POD Rev.0

**Raystar Microelectronics Technology Inc.**

## Revision History

| Revision | Description | Date |
|---|---|---|
| 0.9 | 1.Preliminary. | 2023/9/16 |
| 1.0 | 1.Official Release. | 2024/1/30 |
| 1.1 | 1.Update Pin Configuration.<br>2.Update the Plots.<br>3.Update the LP_HCSL Test Circuit and Oscillator Circuit. | 2024/7/19 |
| 1.2 | 1. Modify the operation temperature range to -40~85℃<br>2. Modify the document No. to RSM-DS-R-0116 | 2024/9/18 |
| | | |