Features

- Fast (400kHz) I2C Interface
- Software Clock Calibration
- RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year Trickle charge capability
- Automatic Power-Fail Detect and Switch Circuitry
- Trickle-Charge Capability
- Low Timekeeping Voltage Down to 1.4V
- Three Operating Voltage Ranges (1.8V, 3V, and 3.3V)
- Oscillator Stop Flag
- Operating Temperature: -40 ~ 85°C

Applications

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)

Description

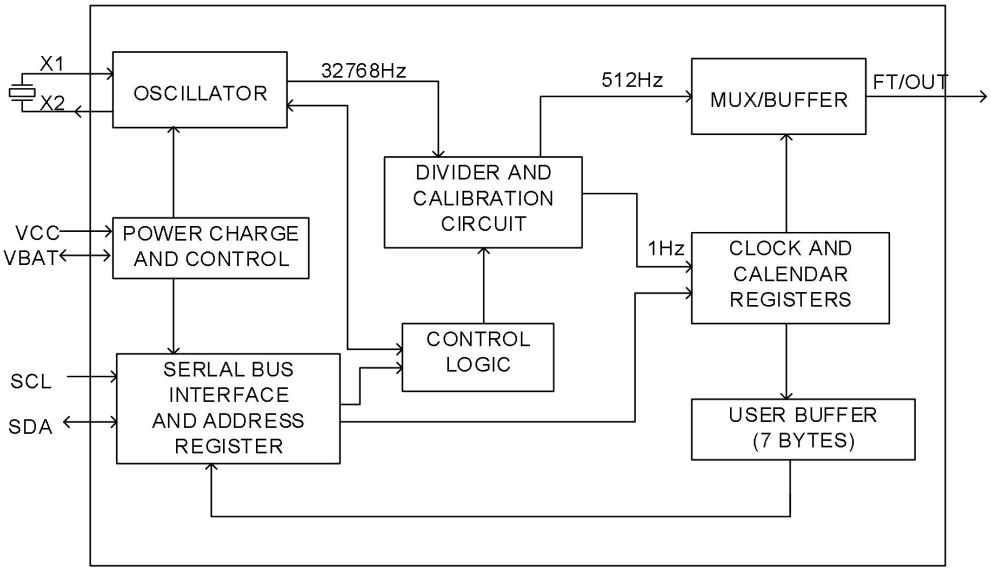
The RS4C1340 is a real-time clock (RTC)/calendar that is pin compatible and functionally equivalent to the ST M41T00, including the software clock calibration. The device additionally provides trickle-charge capability on the VBAT pin, a lower timekeeping voltage, and an oscillator STOP flag. Block access of the register map is identical to the ST device. Two additional registers, which are accessed individually, are required for the trickle charger and flag. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. A built-in power-sense circuit detects power failures and automatically switches to the backup supply. The device is programmed serially through an I2C bidirectional bus.

Ordering Information

Ordering Code	Package	Package Description
RS4C1340-18WE	W	SOP-8
RS4C1340-30WE	W	SOP-8
RS4C1340-33WE	W	SOP-8
RS4C1340-18UE	U	MSOP-8
RS4C1340-30UE	U	MSOP-8
RS4C1340-33UE	U	MSOP-8

Notes:
E = Pb-free and Green

Block Diagram



Pin Configuration

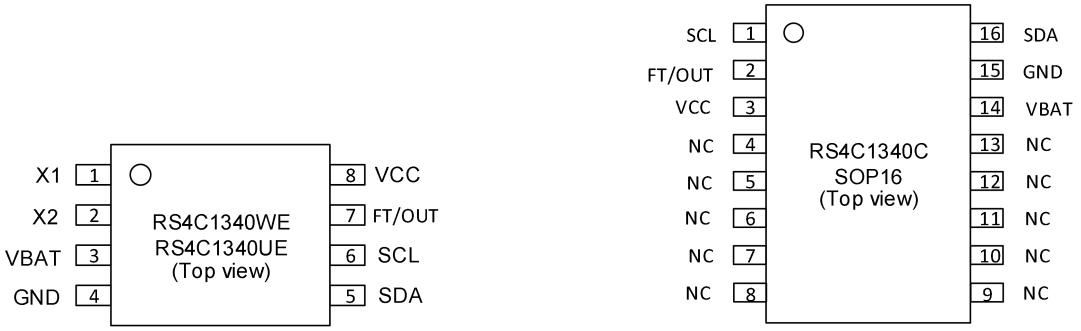


Figure 1. Pin Configuration

Pin Name	Pin No.		Description
	SOP8	SOP16	
X1	1	-	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5pF. X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, X2, is floated if an external oscillator is connected to X1.
X2	2	-	
VBAT	3	14	Connection for a Secondary Power Supply. This pin can be connected to a primary cell such as a lithium coin cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle-charge feature.
GND	4	15	Ground
SDA	5	16	Serial Data Input/Output. SDA is the data input/output for the I 2C serial interface. The SDA pin is open drain and requires an external pullup resistor.
SCL	6	1	Serial Clock Input. SCL is the clock input for the I 2C interface and is used to synchronize data movement on the serial interface.The SCL pin is open drain and requires an external pullup resistor.
FT/OUT	7	2	Frequency Test/Output. This pin is used to output either a 512Hz signal or the value of the OUT bit. When the FT bit is logic 1, the FT/OUT pin toggles at a 512Hz rate. When the FT bit is logic 0, the FT/OUT pin reflects the value of the OUT bit. This open-drain pin requires an external pullup resistor.
V_{CC}	8	3	DC Power for Primary Power Supply.
N.C.	-	4–13	No Connection. Must be connected to ground.

Typical Application Circuit

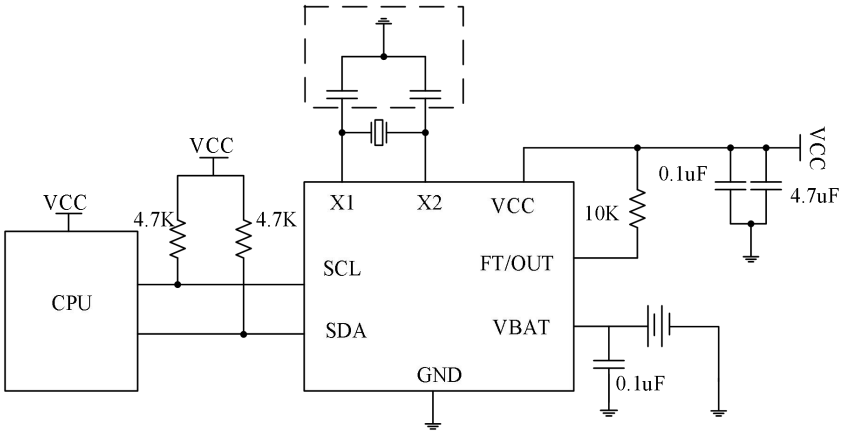


Figure 2. Typical Application Circuit

Notes:

1. FT/OUT open drain,need to add a pull up resistor.
2. It is recommended to add 0.1uF capacitor to VBAT pin.

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature Range	−55	-	+125	°C
Top	Operating Temperature Range	−40	-	+85	°C
V_{CC}	Voltage Range on VCC Pin Relative to Ground	-0.3	-	6.0	V
V_{IO}	Voltage Range on SDA, SCL, and FT/OUT Relative to Ground	-0.3	-	VCC+0.3	V

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(VCC = VCC MIN to VCC MAX, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VCC = 3.3V, TA = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage (Note 8)	V_{CC}	RS4C1340-18	1.71	1.8	1.89	V
		RS4C1340-3	2.7	3	3.3	
		RS4C1340-33	2.97	3.3	5.5	
Input Logic 1 (SDA, SCL)	V_{IH}	(Note 2)	0.7 x VCC	-	VCC + 0.3	V
Input Logic 1 (SDA, SCL)	V_{IL}	(Note 2)	-0.3	-	0.3*VCC	V
Supply Voltage, Pullup (FT/OUT, SDA, SCL), VCC = 0V	V_{PU}	(Note 2)	-	-	5.5	V
Backup Supply Voltage (Note 8)	VBAT	RS4C1340-18	1.4	-	3.7	V
		RS4C1340-3	1.4	-	3.7	
		RS4C1340-33	1.4	-	3.7	
Trickle-Charge Current-Limiting Resistors	R1	(Notes 3, 4)	-	250	-	Ω
	R2	(Notes 5)	-	2000	-	
	R3	(Notes 6)	-	4000	-	
Power-Fail Voltage (Note 8)	V_{PF}	RS4C1340-18	1.51	1.6	1.71	V
		RS4C1340-3	2.45	2.6	2.7	
		RS4C1340-33	2.7	2.88	2.97	
Input Leakage (SCL, CLK)	I_{LI}		-1	-	1	uA
I/O Leakage (SDA, FT/OUT)	I_{LO}		-1	-	1	uA
SDA Logic 0 Output	I_{OLSDA}	VCC > 2V; VOL = 0.4V	-	-	3	mA
		1.7V < VCC < 2V; VOL = 0.2 x VCC	-	-	3	
FT/OUT Logic 0 Output	I_{OLSQW}	VCC > 2V; VOL = 0.4V	-	-	3	mA
		1.7V < VCC < 2V; VOL = 0.2 x VCC	-	-	3	
		1.3V < VCC < 1.7V; VOL = 0.2x VCC	-	-	250	uA
Active Supply Current (Note 7)	I_{CCA}	RS4C1340-18	-	72	150	uA
		RS4C1340-3	-	108	200	
		RS4C1340-33		192	300	
Standby Current (Note 8)	I_{CCS}	RS4C1340-18	-	60	100	uA
		RS4C1340-3	-	81	125	
		RS4C1340-33	-	100	150	
VBACKUP Leakage Current	$I_{BACKUPLKG}$	VBAT = 3.7V	-	-	100	nA

VBAT Current	$I_{BACKUP1}$	OSC ON, FT = 0 (Note 9)	-	800	1150	nA
	$I_{BACKUP2}$	OSC ON, FT = 1 (Note 9)	-	850	1250	
	$I_{BACKUP3}$	OSC ON, FT = 0, VBACKUP = 3.0V, TA = +25°C (Notes 9, 10)	-	800	1000	
VBACKUP Data-Retention Current	$I_{BACKUPDR}$	OSC OFF	-	25	100	nA

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: Measured at VCC = typ, VBACKUP = 0V, register 08h = A5h.
Note 4: The use of 250Ω trickle-charge resistor is not allowed at VCC > 3.63V and shouldn't be enabled
Note 5: Measured at VCC = typ, VBACKUP = 0V, register 08h = A6h.
Note 6: Measured at VCC = typ, VBACKUP = 0V, register 08h = A7h.
Note 7: ICCA—SCL clocking at max frequency = 400kHz.
Note 8: Specified with I2C bus inactive.
Note 9: Measured with a 32.768kHz crystal attached to the X1 and X2 pins.
Note 10: Limits at +25°C are guaranteed by design and not production tested.

Crystal electrical characteristics

Symbol	Parameter*1	MIN	TYP	MAX	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			100	kΩ
C_L	Load capacitance		12.5		pF

Notes:
1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

I2C AC Characteristics

(VCC = VCC MIN to VCC MAX, TA = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode	0		100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			µs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition	Fast mode	0.6			µs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			µs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			µs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			µs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time	Fast mode	0		0.9	µs
		Standard mode	0		0.9	
$t_{SU:DAT}$	Data Setup Time	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
t_F	Fall Time of Both SDA and SCL Signals	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			µs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line	(Note 1)			400	pF
$C_{I/O}$	I/O Capacitance (SCL, SDA)			10		pF
t_{SP}	Pulse Width of Spikes that Must be Suppressed by the Input Filter	Fast mode		30		ns
t_{OSF}	Oscillator Stop Flag (OSF) Delay	(Note 2)		100		ms

Note 1: C_B—total capacitance of one bus line in pF.
Note 2: The parameter tOSF is the period of time the oscillator must be stopped for the OSF flag to be set over the 0V ≤ VCC ≤ VCCMAX and 1.4V ≤ VBAT ≤ 3.7V range.

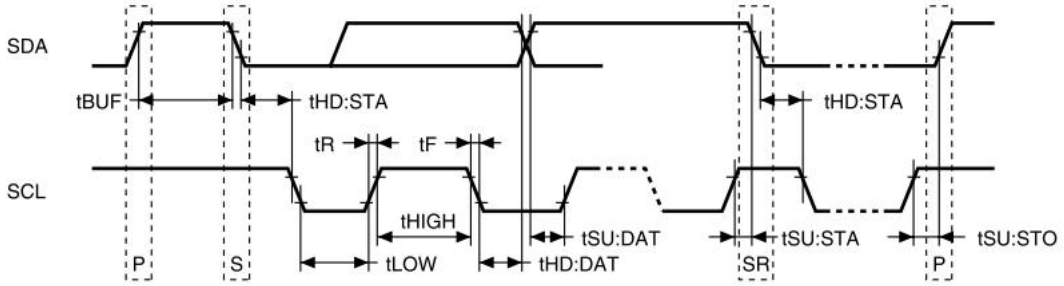


Figure3: Bus timing requirements sequence

Power-Up/Power-Down Characteristics

(TA = -40°C to +85°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
t_{REC}	Recovery at Power-Up*2				2	ms
t_{VCCF}	V_{CC} Fall Time	$V_{PF(MAX)}$ to $V_{PF(MIN)}$	300			µs
t_{VCCR}	V_{CC} Rise Tim	$V_{PF(MIN)}$ to $V_{PF(MAX)}$	0			µs

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

Test Circuits

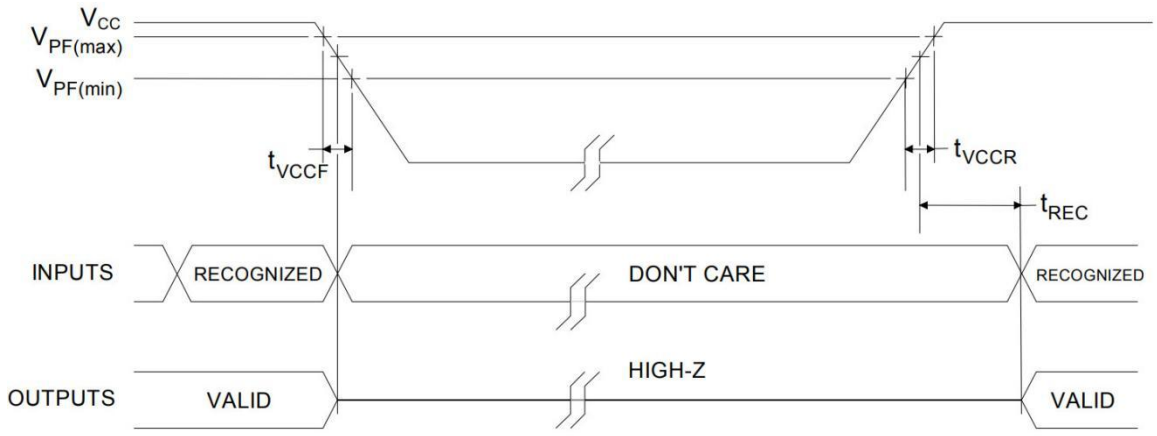


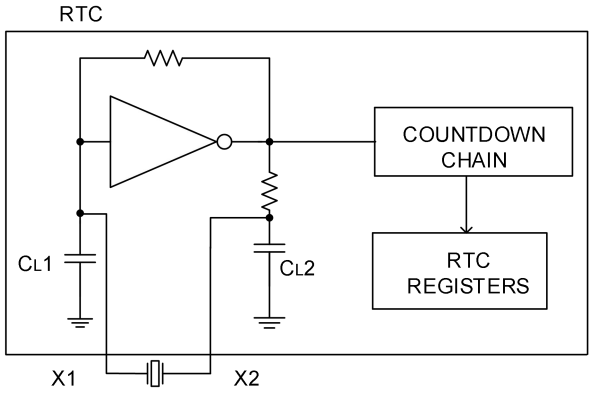
Figure 4: Power-Up/Power-Down Timing

Functional Description

The RS4C1340 is a low-power clock/calendar with a trickle charger. Address and data are transferred serially through a I2C bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The RS4C1340 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply.

Oscillator Circuit

The RS4C1340 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table: Crystal Specifications specifies several crystal parameters for the external crystal. Figure below shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.



Clock Accuracy

The initial clock accuracy depends on the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast.

IIC bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be pulled up via a pull-up resistors.
The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain high.

Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

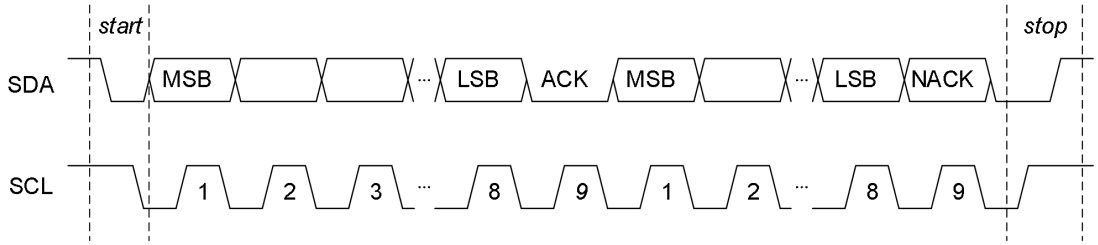


Figure5: Serial bus data transfer sequence

Read mode

In this mode, the master reads the RS4C1340 slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The RS4C1340 slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

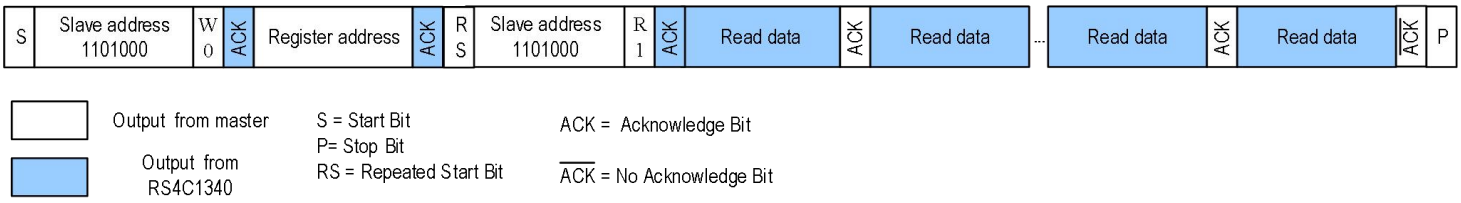


Figure6: Read Mode Sequence

Write mode

In this mode the master transmitter transmits to the RS4C1340 slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The RS4C1340 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

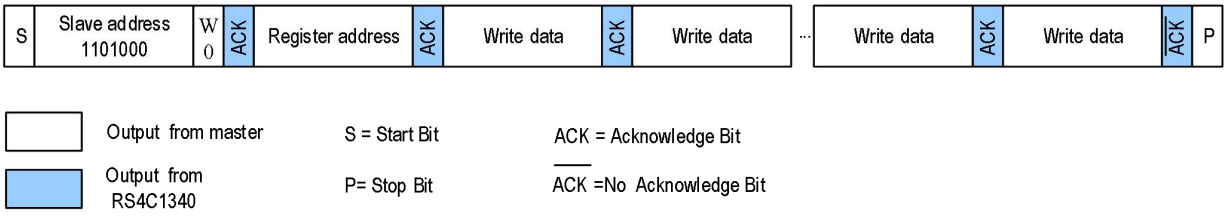


Figure7: Write mode sequence

Application Information

The RS4C1340 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when VCC is greater than VPF. However, when VCC falls below VPF, the internal clock registers are blocked from any access. If VCC is less than VPF, the device power is switched from VCC to VBAT.

Register Configuration

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00H	EOSC	10 seconds			Seconds				Seconds	00-59
01H	X	10 minutes			Minutes				Minutes	00-59
02H	CEB	CB	10 hours		Hours				Century/hours	0-1/00-23
03H	X	X	X	X	X	Day			Day	01-07
04H	X	X	10 dates		Date				Date	01-31
05H	X	X	X	10 M.	Month				Month	01-12
06H	10 years				Years				Year	00-99
07H	OUT	FT	S	Calibration					Control	
08H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUTI	ROUT0	Trickle Charge	
09H	OSF	0	0	0	0	0	0	0	Flag	

The time and calendar information is obtained by reading the appropriate register bytes. Table: RS4C1340 Timekeeper Registers shows the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Seconds register(0x00)

D7(EOSC)	D6	D5	D4	D3	D2	D1	D0
EOSC=1:oscillator stop EOSC=0:oscillator enable	10 seconds			Seconds			

Minutes register(0x01)

D7	D6	D5	D4	D3	D2	D1	D0
X	10 minutes			Minutes			

Century/hours register(0x02)

D7(CEB)	D6(CB)	D5	D4	D3	D2	D1	D0
CEB=1:Century enable CEB=0:Century disable	Set Century enable(CEB=1), CB will be toggled either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state)	10 hours		Hours			

Day register(0x03)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	Day		

Date register(0x04)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	10 dates		Date			

Month register(0x05)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	10M	Month			

Year register(0x06)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Control register(0x07)

D7(OUT)	D6(FT)	D5	D4	D3	D2	D1	D0
Output driver pin When D6(FT)=0 OUT=0 FT/OUT pin outputs low OUT=1 FT/OUT pin outputs high	FREQUENCY TEST bit FT=0 Output 512Hz Disable FT=1 Output 512Hz Enable	Calibration offset value **1**11111=+126.108 ... **1**00010=+8.136 **1**00001=+4.068 000000=0 **0**00001=-2.034 **0**00010=-4.068 ... **0**11111=-64.108					

Trickle Charge Register (0x08)

D7	D6	D5	D4	D3	D2	D1	D0
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUTI	ROUT0

The simplified schematic of Figure: Programmable Trickle Charge shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. The ROUT bits (bits 0, 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Bit values are shown in below table

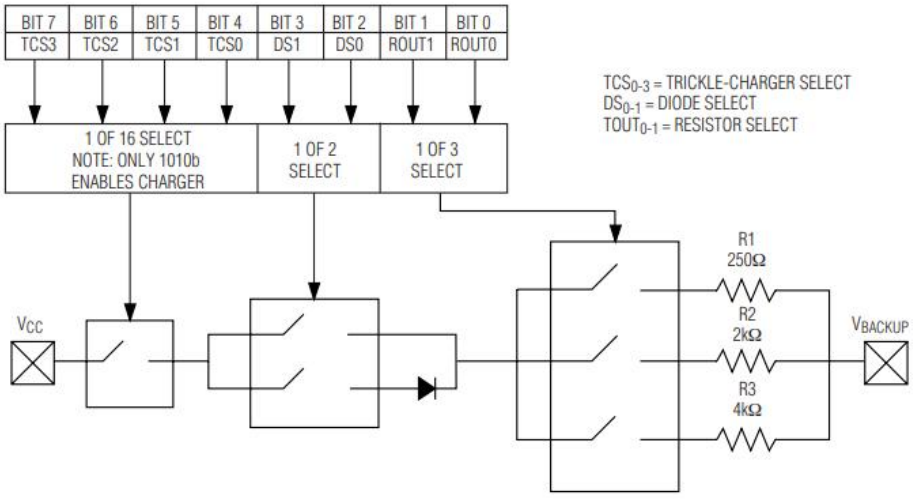
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ωresistor
1	0	1	0	0	1	1	0	No diode, 2kΩresistor
1	0	1	0	1	0	1	0	One diode, 2kΩresistor
1	0	1	0	0	1	1	1	No diode, 4kΩresistor
1	0	1	0	1	0	1	1	One diode, 4kΩresistor
0	0	0	0	0	0	0	0	Power-on reset value

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example:

Assume that a system power supply of 3.3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would, therefore, be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap or battery charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and, therefore, the charge current decreases.



Flag Register (0x09)

D7(OSF)	D6	D5	D4	D3	D2	D1	D0
OSF=1:oscillator has stopped or was stopped for some time period	0	0	0	0	0	0	0

This bit is edge triggered and is set to logic 1 when the internal circuitry senses that the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on both VCC and VBACKUP are insufficient to support oscillation.
3) The EOSC bit is set to 1, disabling the oscillator.
4) External influences on the crystal (e.g., noise, leakage, etc.).

The OSF bit remains at logic 1 until written to logic 0. It can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Preferred initial power-on defaults

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a '1'. All other register bits will initially power on in a random state. After the chip is powered on for the first time, all registers are required to be initialized.

Clock Calibration

The RS4C1340 provides a digital clock calibration feature to allow compensation for crystal and temperature variations.

The calibration circuit adds or subtracts counts from the oscillator divider chain at the divide-by-256 stage. The number of pulses blanked (subtracted for negative calibration) or inserted (added for positive calibration) depends upon the value loaded into the five calibration bits located in the control register. Adding counts speeds the clock up and subtracting counts slows the clock down.

The calibration bits can be set to any value between 0 and 31 in binary form. Bit 5 of the control register, S, is the sign bit. A value of 1 for the S bit indicates positive calibration, while a value of 0 represents negative calibration. Calibration occurs within a 64-minute cycle.

The first 62 minutes in the cycle can, once per minute, have a one-second interval where the calibration is performed. Negative calibration blanks 128 cycles of the 32,768Hz oscillator, slowing the clock down. Positive calibration inserts 256 cycles of the 32,768Hz oscillator, speeding the clock up. If a binary 1 is loaded into the calibration bits, only the first two minutes in the 64- minute cycle are modified. If a binary 6 is loaded, the first 12 minutes are affected, and so on. Therefore, each calibration step either adds 512 or subtracts 256 oscillator cycles for every 125,829,120 actual 32,678Hz oscillator cycles (64 minutes). This equates to +4.068ppm or -2.034ppm of adjustment per calibration step.

If the oscillator runs at exactly 32,768Hz, each of the 31 increments of the calibration bits would represent +10.7 or -5.35 seconds per month, corresponding to +5.5 or -2.75 minutes per month. For example, if using the FT function, a reading of 512.01024Hz would indicate a +20ppm oscillator frequency error, requiring a -10(00 1010) value to be loaded in the S bit and the five calibration bits.

Note: Setting the calibration bits does not affect the frequency test output frequency. Also note that writing to the control register resets the divider chain.

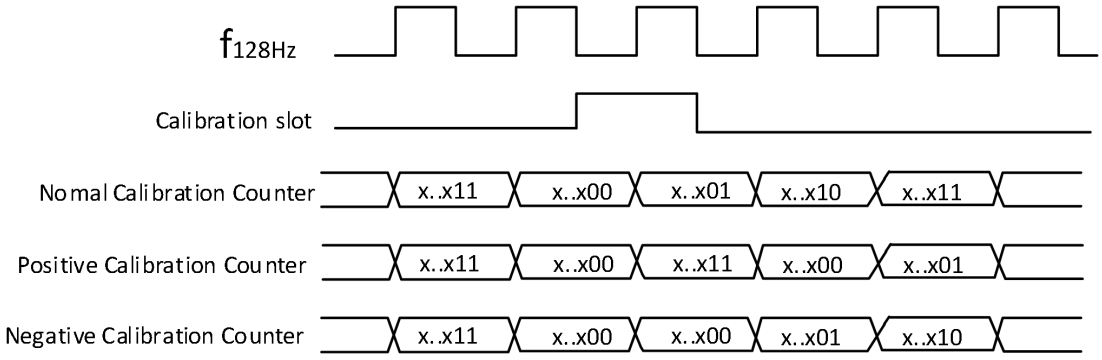
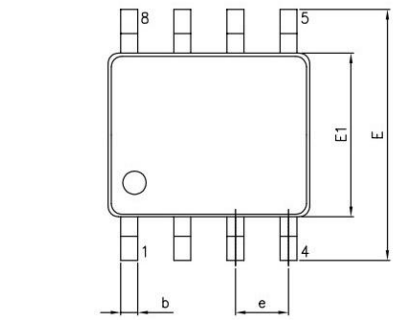
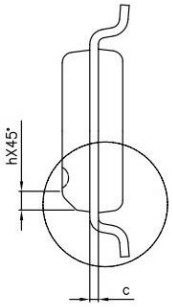


Figure8: Clock Calibration

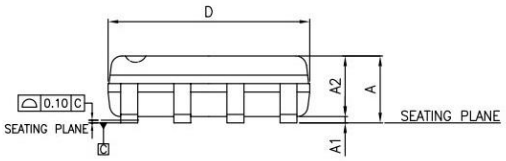
Package Information

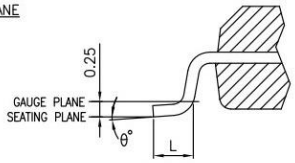
SOP-8 Package

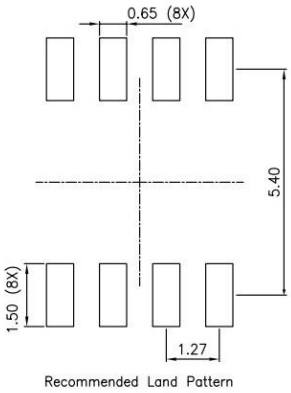




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8







Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

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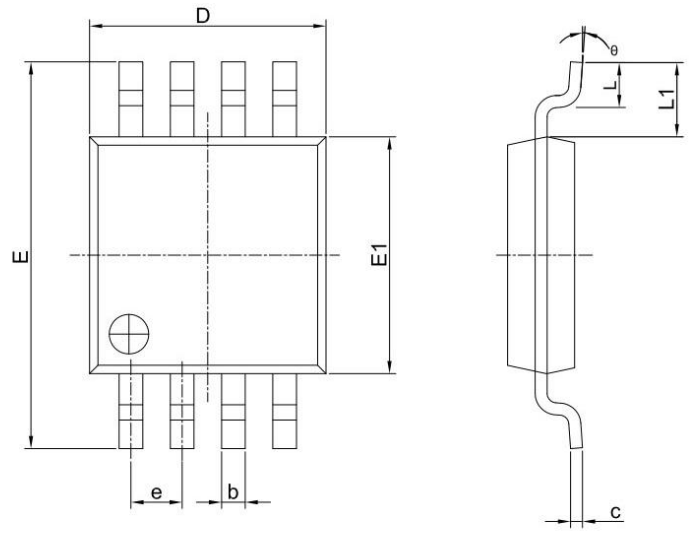
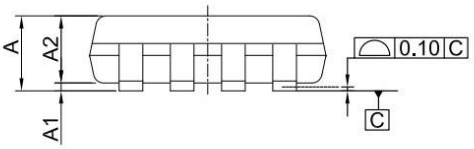
MSOP-8 Package





PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-187
3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary Release	2024/2/18
1.0	Initial Release	2024/3/26