



Features

- PCIe 3.0 compliant
- PCIe 3.0 Phase Jitter -0.45 ps RMS
- LVDS compatible output
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 35ps cycle-to-cycle (typ)
- Spread of -0.5%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)
16-pin TQFN

Block Diagram

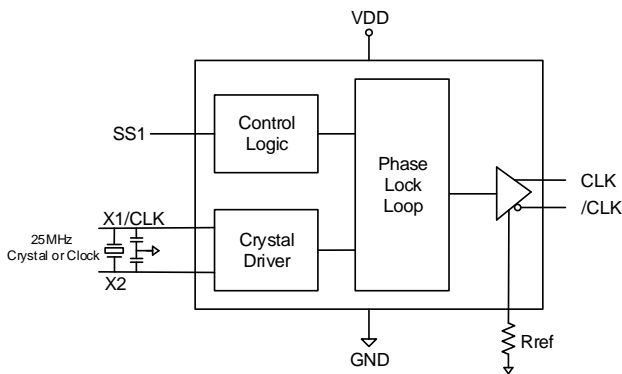


Figure 1 Block Diagram

Description

The RS2CG5701B is a spread spectrum clock generator compliant to PCI Express3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The RS2CG5701B provides one differential (HCSL) or LVDS spread spectrum output. Using Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces one pair of differential outputs (HCSL) at 100MHz. It also provides spread selection of -0.5% and no spread.

Ordering Information

Ordering Code	Package	Description
RS2CG5701BZHE	ZH	TQFN-16L 3X3X0.75

Notes:

[1] E = Pb-free and Green



Pin Configuration

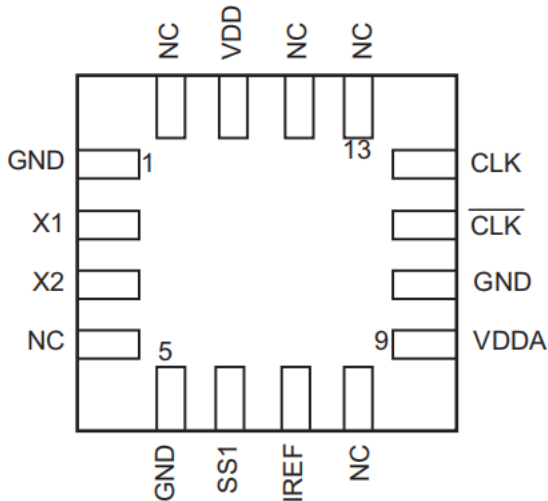


Table 1 Spread Selection Table

SS1	Spread
0	Down -0.5%
1	No Spread

Pin Description

Pin No.	Pin Name	Type	Description
1	GND	Power	Connect to ground
2	X1	Input	Crystal or reference clock in
3	X2	Output	XTAL out. Leave unconnected for clock input.
4	NC	-	No connect
5	GND	Power	Connect to ground
6	SS1	Input	Spread select 1. Internal pull up resistor
7	IREF	Output	475Ω precision resistor attached to this pin is connected to the internal current reference.
8	NC	-	No connect
9	VDDA	Power	Connect to 3.3V source
10	GND	Power	Connect to ground
11	/CLK	Output	HCSL complimentary clock output
12	CLK	Output	HCSL clock output
13	NC	-	No connect
14	NC	-	No connect
15	VDD	Power	Connect to 3.3V source for OSC and core
16	NC	-	No connect



Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
Tstore	Storage Temperature	-65	-	+150	°C
VDD	Supply Voltage to Ground Potential	-0.5	-	5.5	V
VIO	Input / Output Voltage	-0.5	-	VDD+0.5	V
ESD	ESD HBM protection (input)	2000			V

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VDD	Power Supply Voltage	3.0	-	3.6	V
VI	SS1 Control Pin Voltage	-0.3	-	3.6	V
TA	Operating Temperature Range	-40	-	+85	°C



DC Electrical Characteristics

Unless otherwise specified, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $3.0\text{V} \leq V_{DD} \leq 3.6\text{V}$

Symbol	Parameter	Conditions		MIN	TYP	MAX	Unit
VDD	Supply Voltage			3.0	3.3	3.6	V
VIH	Input High Voltage ⁽¹⁾	SS1		0.7*VDD		VDD +0.3	V
VIL	Input Low Voltage ⁽¹⁾	SS1		GND -0.3		0.3*VDD	V
IIL	Input Leakage Current	$0 \leq V_{in} \leq V_{DD}$	Without input pull-up and pull-downs	-5		5	μA
IDD	Operating Supply Current	$R_L = 50\Omega$, $C_L = 2\text{pF}$				95	mA
CIN	Input Capacitance					7	pF
COUT	Output Capacitance					6	pF
LPIN	Pin Inductance					5	nH
ROUT	Output Resistance	CLK Outputs		3.0			k Ω

Note:

1. $R_L = 50\ \text{ohm}$ with $C_L = 2\ \text{pF}$
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point



AC Characteristics

($V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

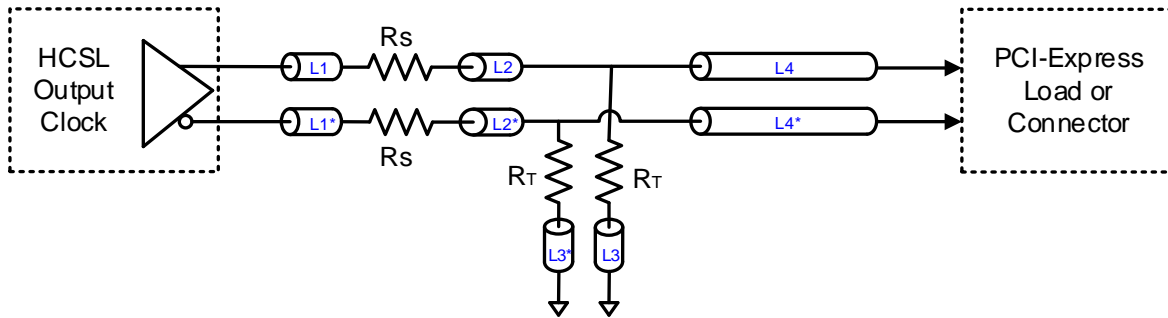
Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
FIN	Input Frequency			25		MHz
FOUT	Output Frequency			100		MHz
VOH	Output High Voltage (1,2)	100 MHz HCSL output @ $V_{DD} = 3.3V$	660	800	900	mV
VOL	Output Low Voltage(1,2)		-150	0	150	mV
VCPA	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
VCN	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
JCC	Jitter, Cycle-to-Cycle(1,3)			35	60	ps
JRMS2.0	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
JRMS3.0	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.75	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.18	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	1	ps
MF	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
tOR	Rise Time(1,2)	From 0.175V to 0.525V	175	332	700	ps
tOF	Fall Time(1,2)	From 0.525V to 0.175V	175	344	700	ps
TSKEW	Skew between outputs	At Crossing Point Voltage			50	ps
TDUTY-CYCLE	Duty Cycle(1,3)		45		55	%
tSTABLE	From power-up to $V_{DD}=3.3V$	From Power-up $V_{DD}=3.3V$		3.0		ms
tSPREAD	Setting period after spread change	Setting period after spread change		3.0		ms

Note:

1. $R_L = 50$ ohm with $C_L = 2$ pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point



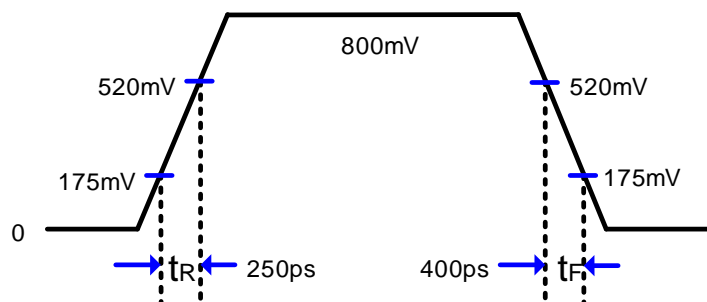
PCIe Device Routing (HCSL)



PCI Express Layout Guidelines

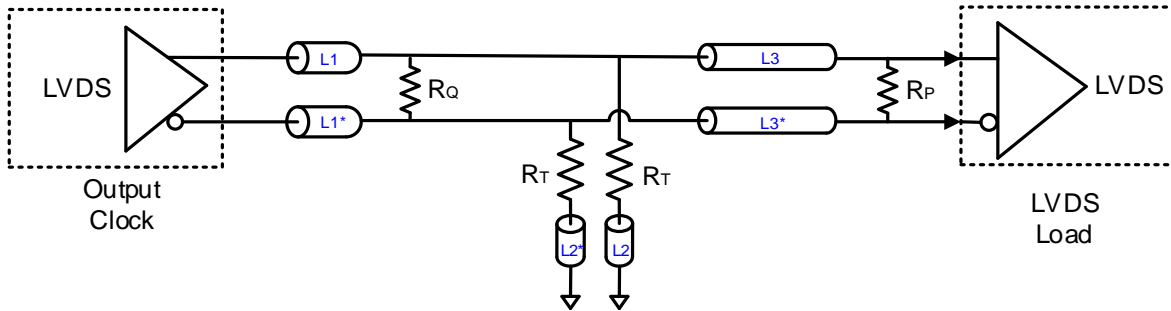
Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	1.8 min to 14.4 max	inch
Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	0.225 min to 12.6 max	inch

Typical HCSL Waveform





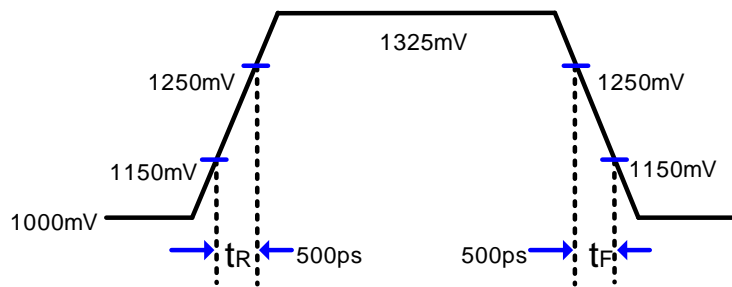
LVDS Device Routing



LVDS Device Routing Guidelines

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
RP	100	Ω
RQ	100	Ω
RT	150	Ω
L3 length, route as 100Ω differential trace(strip-line)	14 max	inch
L3 length, route as 100Ω differential trace.(Micro Strip-line)	12 max	inch

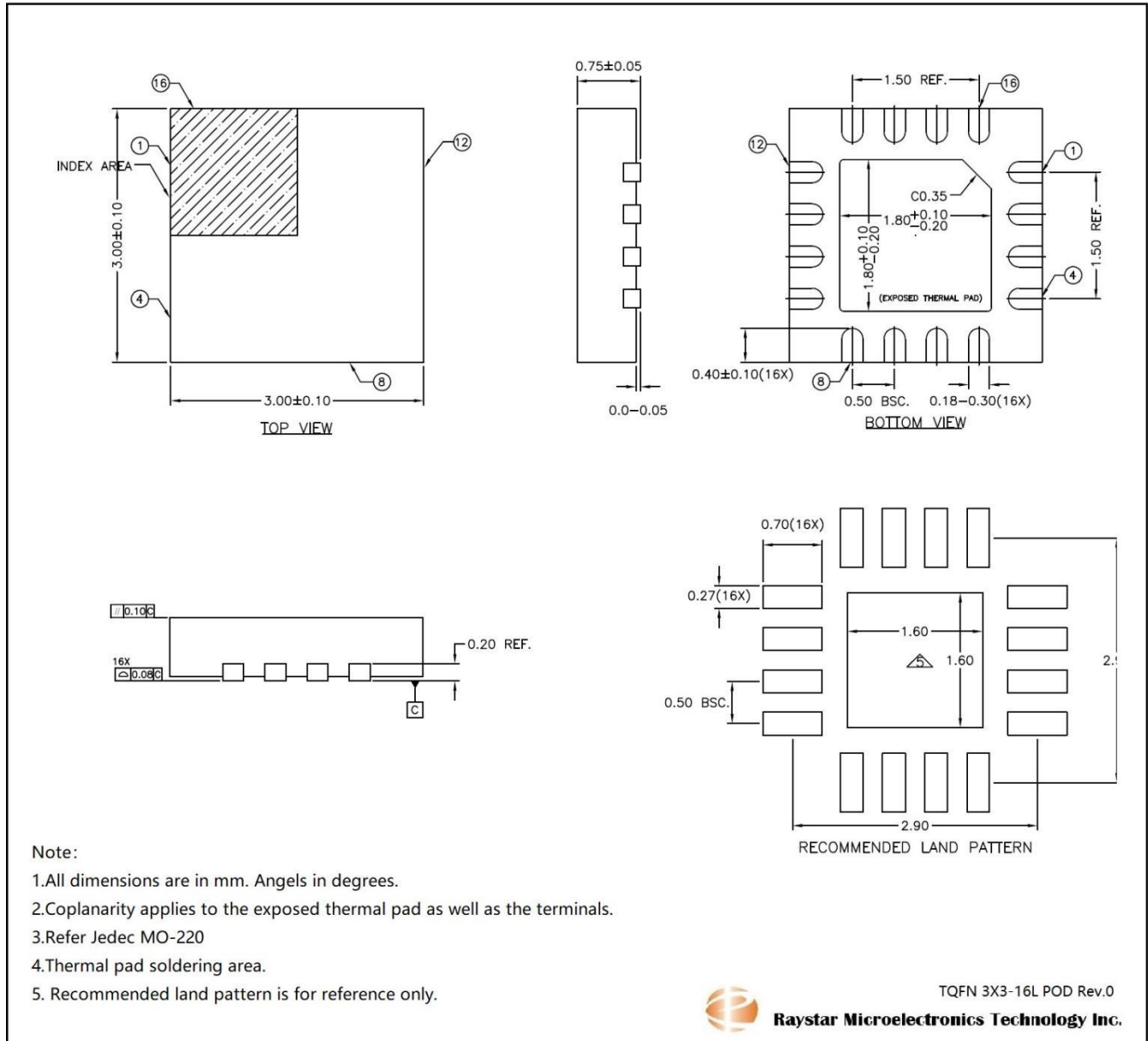
Typical LVDS Waveform





Package Information

TQFN16L





RSM

www.raystar-tek.com

RS2CG5701B

PCIe3.0 Clock Generator with 1 HCSL Outputs

Revision History

Revision	Description	Date
V1.0	Official release	2023/6/15
V1.1	Delete the OE pin description	2024/2/23