Features

- Counters for seconds, minutes, hours, day, date, month, years and century
- 32 kHz crystal oscillator integrating load capacitance (12.5 pF) providing exceptional oscillator stability and high crystal series
- Serial interface supports I2C bus (400 kHz protocol)
- Ultra-low battery supply current of 0.4 µA (typ. at 3 V)
- 2.0 to 5.5 V clock operating voltage
- Automatic switchover and deselect circuitry
- 56 bytes of general purpose RAM
- Software clock calibration to compensate crystal deviation due to temperature
- Automatic leap year compensation
- Grade 1 Temperature Range: -40~125 ºC
- AEC-Q 100 qualified. PPAP capable, and manufactured in IATF 16949 certified facilities.

Description

The RS4C411Q is a low-power serial real-time clock (RTC) with 56 bytes of NVRAM. A built-in 32.768 kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. Addresses and data are transferred serially via a two-line bidirectional bus. The built-in address register is incremented automatically after each write or read data byte.

The RS4C411Q clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium coin cell.

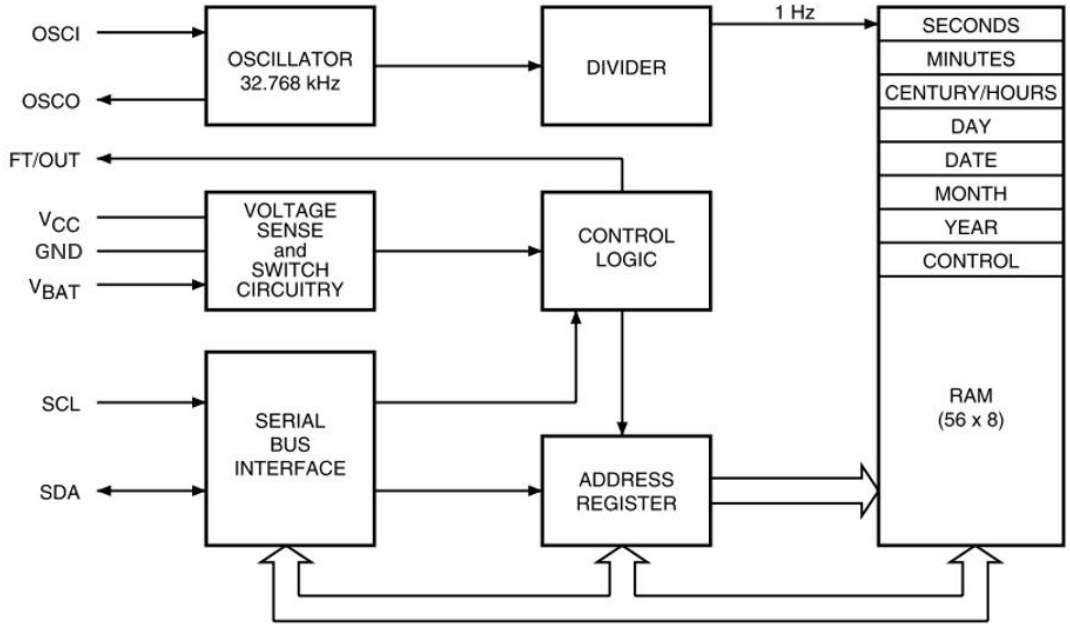
Typical data retention time is in excess of 5 years with a 50 mA/h, 3V lithium cell. The RS4C411Q is supplied in an 8-lead plastic small outline package. RS4C411Q is suitable for automotive applications requiring specific change control.

Ordering Information

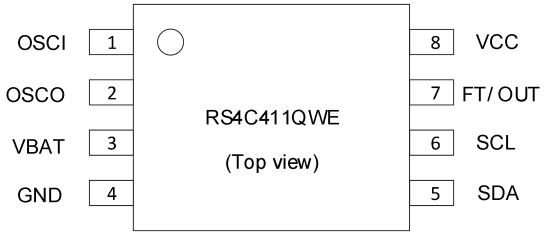
Ordering Code	Package	Package Description
RS4C411QWE	SOP8	pitch 1.27mm

Notes:
[1] E = Pb-free and Green

Figure 1. SOP8/MSO8/DFN8 Block Diagram



Pin Configuration



Pin Name	Pin No.	Type	Description
OSCI	1	Input	Oscillator input
OSCO	2	Output	Oscillator output
VBAT	3	Power	Battery supply voltage
GND	4	GND	Ground
SDA	5	I/O	Serial data address input/output
SCL	6	Input	Serial clock.
FT/OUT	7	Output	Frequency test/output driver (open drain)
VCC	8	Power	Supply voltage
N.C.	-	-	No connection

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	−55	-	+150	°C
V_{CC}	DC Supply Voltage	-0.3	-	6.0	V
V_{IO}	Input / Output Voltage	-0.3	-	6.0	V
IO	Output Current			20	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	2.0	-	5.5	V
V_{IO}	I/O Pin Voltage	GND	-	5.5	V
T_A	Operating Temperature Range	−40	-	125	°C

DC Electrical Characteristics

DC characteristics

Symbol	Parameter	Test Condition*1	MIN	TYP	MAX	Unit
I_{LI}	Input leakage current	0V≤VIN ≤V_{CC}			±1	µA
I_{LO}	Output leakage current	0V ≤VOUT≤V_{CC}			±1	µA
I_{CC}	Supply current	Switch frequency = 400 kHz			150	µA
V_{IL}	Input low voltage		–0.3		0.3*V_{CC}	V
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.4	V
V_{PU}	Pull-up supply voltage (open drain)	FT/OUT			5.5	V
V_{BAT}	Battery supply voltage		2.5*2	3	3.5*3	V
I_{BAT}	Battery supply current	TA = 25°C, V_{CC} = 0 V, oscillator ON, V_{BAT} = 3 V		0.4	1.5	µA

Note:
1. Valid for ambient operating temperature: TA = –40 to 125°C; VCC = 2.0 to 5.5 V (except where noted).
2. After switchover (VSO), VBAT(min) can be 2.0 V for crystal with RS = 40 kΩ.
3. For rechargeable back-up, VBAT(max) may be considered VCC.

Capacitance

Symbol	Parameter*1*2	MIN	MAX	Unit
C_{IN}	Input capacitance (SCL)		7	pF
C_{OUT}	Output capacitance (SDA, FT/OUT)		10	pF

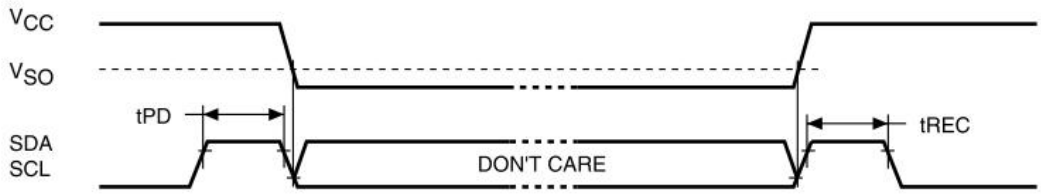
Crystal electrical characteristics

Symbol	Parameter*1*2	MIN	TYP	MAX	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			100	kΩ
C_L	Load capacitance		12.5		pF

Note:
1. These values are externally supplied if using the SOIC8 package.
2. Load capacitors are integrated within the RS4C411Q. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

AC Electrical characteristics

Power down/up mode AC waveforms



Power down/up AC characteristics

Symbol	Parameter*1*2	MIN	MAX	Unit
t_{PD}	SCL and SDA at VIH before power down	0		ns
t_{REC}	SCL and SDA at VIH after power up	10		μs

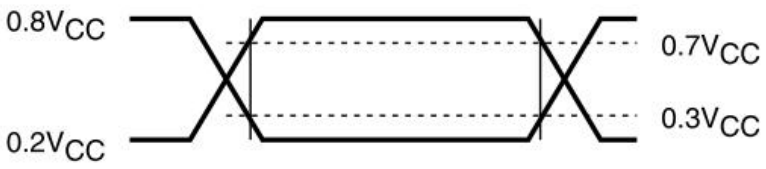
Note
1. Valid for ambient operating temperature: TA = –40 to 125°C; VCC = 2.0 to 5.5 V (except where noted).
2. VCC fall time should not exceed 5 mV/μs.

Power down/up trip points DC characteristics

Symbol	Parameter*1*2	MIN	TYP	MAX*3	Unit
V_{SO}	Battery backup switchover voltage	V_{BAT} – 0.80	V_{BAT} – 0.50	V_{BAT} – 0.30	V

Note
1. Valid for ambient operating temperature: T_A = –40 to +125°C; V_{CC} = 2.0 to 5.5 V (except where noted).
2. All voltages referenced to GND.
3. After VCC is powered up initially, i2C required to read and write once time to activate the oscillator..But when VCC< VSO, the device automatically switches over to the battery mode, at this time I2C can not read and write. So In VCC=3.3 V application, if initial battery voltage is ≥ V_{CC}, it may be necessary to reduce battery voltage (i.e.,through wave soldering the battery) in order to avoid inadvertent switchover/deselection for V_{CC} – 10% operation. It is recommended that the battery voltage is lower than 3.1V at this time.
4. Switchover and deselect point.

AC testing input/output waveform



Parameter	RS4C411Q	Unit
Input rise and fall times	≤ 50	ns

Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$	V
Input and output timing ref. voltages	$0.3V_{CC}$ to $0.7V_{CC}$	V

I2C AC Characteristics

(TA = -40°C to +125°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			µs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			µs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			µs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			µs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			µs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time*3/4	Fast mode	0		0.9	µs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1CB		300	ns
		Standard mode	20 + 0.1CB		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1CB		300	ns
		Standard mode	20 + 0.1CB		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			µs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7				10	pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay*8			100		ms

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. After this period, the first clock pulse is generated
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL
4. The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,MAX} + t_{SU:DAT} = 1000 + 250 = 1250$ns before the SCL line is released.
6. C_B—total capacitance of one bus line in pF
7. Guaranteed by design. Not production tested
8. The parameter t_{OSF} is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC\,MAX}$ and $2.5V \leq V_{BAT} \leq 3.5V$

Application Information

Operation

The RS4C411Q clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: seconds register
- 2nd byte: minutes register
- 3rd byte: century/hours register
- 4th byte: day register
- 5th byte: date register
- 6th byte: month register
- 7th byte: years register
- 8th byte: control register
- 9th - 64th bytes: RAM

The RS4C411Q clock continually monitors VCC for an out of tolerance condition. When VCC falls below VSO, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. Upon power-up, the device switches from battery to VCC at VSO and recognizes inputs.

2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.
The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain high.

Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.
By definition, a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

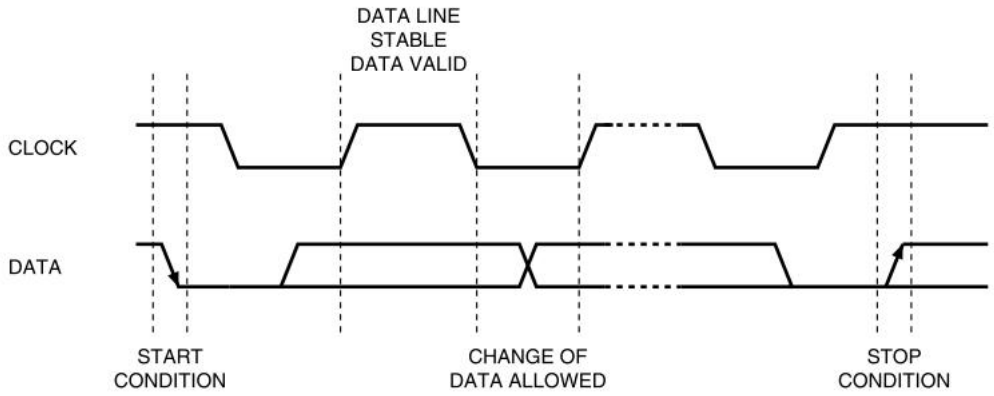
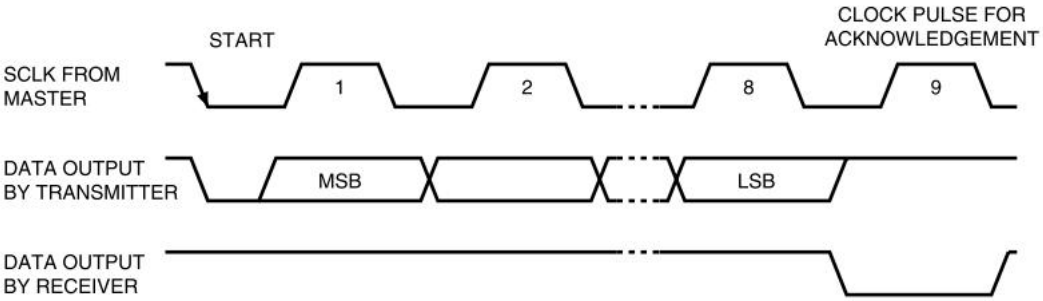
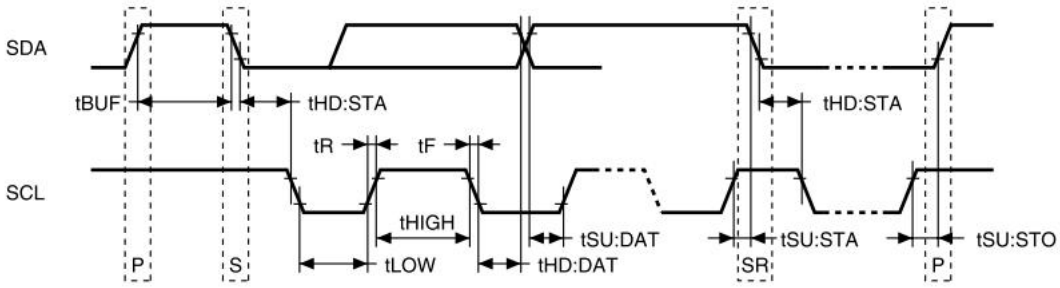


Figure: Serial bus data transfer



sequence

Figure: Acknowledgement



sequence

Figure: Bus timing requirements sequence

Read mode

In this mode, the master reads the RS4C411Q slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The RS4C411Q slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

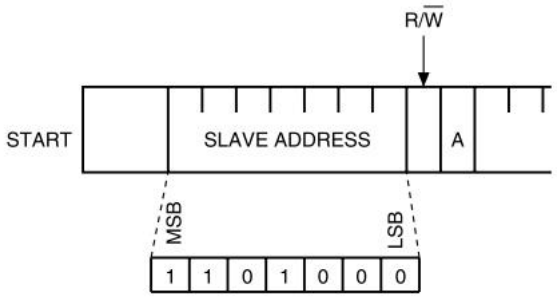


Figure: Slave address location

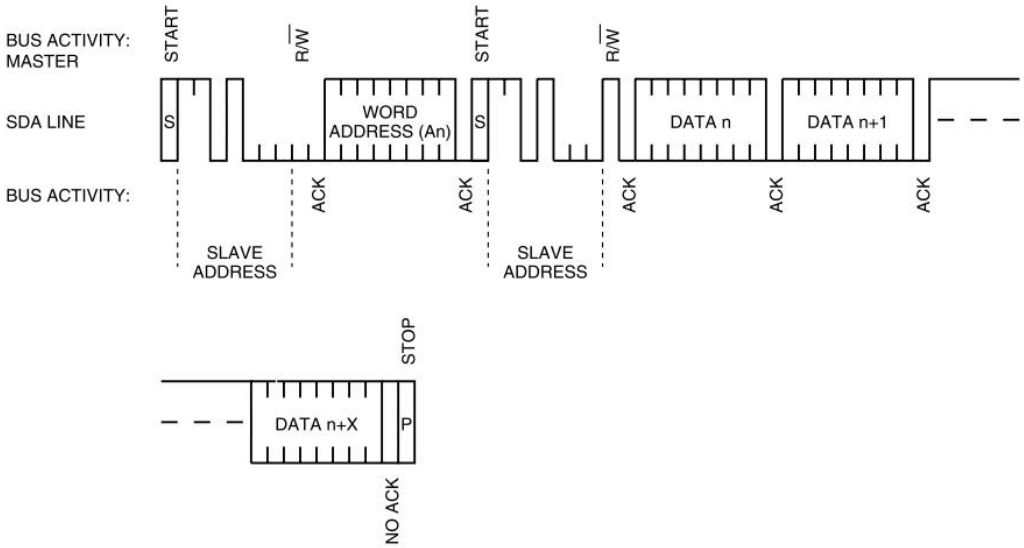


Figure: Read Mode Sequence

Write mode

In this mode the master transmitter transmits to the RS4C411Q slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The RS4C411Q slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

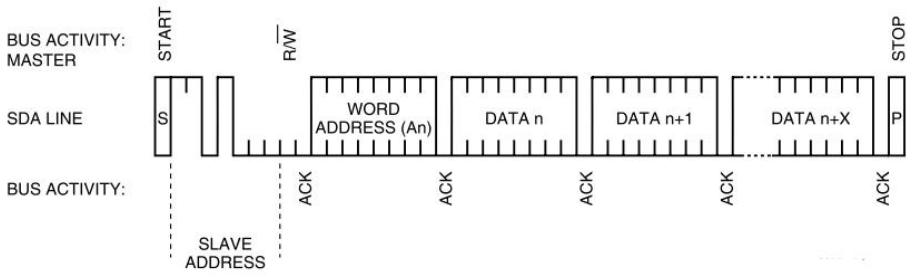


Figure: Write mode sequence

Clock Operation

The eight byte clock register (see Table 3) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, minutes, and hours are contained within the first three registers. Bits D6 and D7 of clock register 2 (hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle. Bits D0 through D2 of register 3 contain the day (day of week). Registers 4, 5 and 6 contain the date (day of month), month and years. The final register is the control register (this is described in the clock calibration section). Bit D7 of register 0 contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

Note: In order to guarantee oscillator startup after the initial power-up, set the ST bit to a '1,' then reset this bit to a '0.' This sequence enables a “kick start” circuit which aids the oscillator startup during worst case conditions of voltage and temperature.
The seven clock registers may be read one byte at a time, or in a sequential block. The control register (address location 7) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250 ms to allow the read to be completed before the update occurs. This will prevent a transition of data during the read.

Note: This 250 ms delay affects only the clock register update and does not alter the actual clock time.

Address	Data*1								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 seconds			Seconds				Seconds	00-59
1	X	10 minutes			Minutes				Minutes	00-59
2	CEB*2	CB	10 hours		Hours				Century/hours	0-1/00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 dates		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

Note
1. Keys:
   ST = STOP bit. Setting this bit to a '1' will cause the oscillator to stop
   X = Don’t care
   CEB = Century enable bit
   CB = Century bit

   When CEB is set to '1', CB will toggle from '0' to'1' or from '1' to '0' every 100 years (dependent upon the initial value set). When CEB is set to '0', CB will not toggle.

   OUT = Output level. Reg 0x07 D7D6=0x00, output Low level. Reg 0x07 D7D6=0x10, output High level.
   FT = FREQUENCY TEST bit. Setting this bit to a '1', output frequency 512hz.

	Data		
address	D7（OUT）	D6（FT）	output
7	0	0	Low level
	0	1	512Hz
	1	0	High level
	1	1	512Hz

S = SIGN bit，'1' indicates positive calibration, '0' indicates negative calibration.
Calibration: represent the degree of time calibration(0~31)，that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

Clock Calibration

The RS4C411Q is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each RS4C411Q improves to better than ±2 ppm at 25°C.

The oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The RS4C411Q design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit calibration byte found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits (D4-D0) in the control register (addr 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64-minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month. Two methods are available for ascertaining how much calibration a given RS4C411Q may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the calibration byte. The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the control register, is set to a '1', and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10(XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

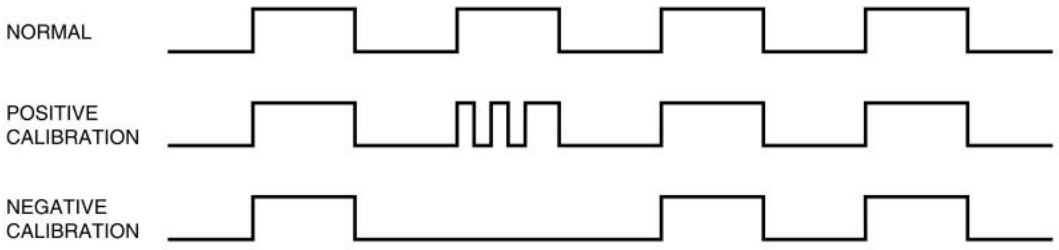


Figure: Clock Calibration

Output driver pin

When the FT bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D6 of location 7 is a zero and D7 of location 7 is a zero and then the FT/OUT pin will be driven low.

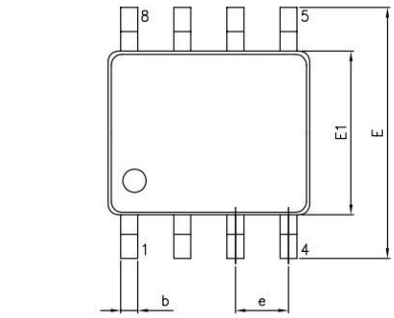
Note:
The FT/OUT pin is open drain which requires an external pull-up resistor.

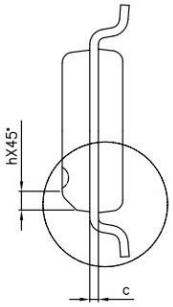
Preferred initial power-on defaults

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a '1'. All other register bits will initially power on in a random state.

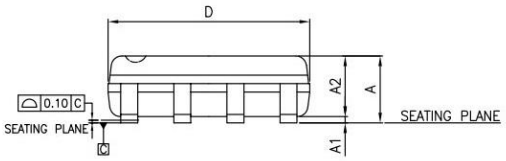
Package Information

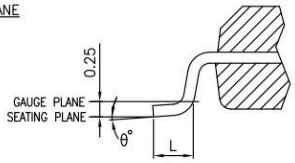
SOP-8 Package

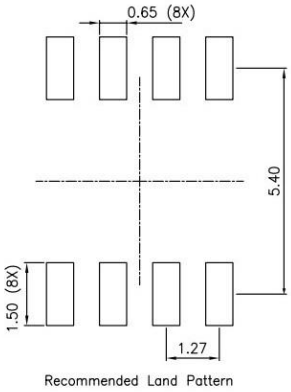




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8







Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	Official release	2023/7/28
V1.1	Update IBAT spec and register description	2023/10/9
V1.2	1. Update register description 2. Increase the VSO description 3. Modify pin description	2023/11/6