RS7LS9306

Bidirectional I2C-bus And SMBus Voltage-Level Translator

Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I²C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I²C-bus and SMBus compatible
- Less than 1.5 ns propagation delay
- Allows voltage level translation between:
  - 1.0 V VREF1 and 1.8 V～5 V VREF2
  - 1.2 V VREF1 and 1.8 V～5 V VREF2
  - 1.5 V VREF1 and 2.5 V～5 V VREF2
  - 1.8 V VREF1 and 3.3 V～5 V VREF2
  - 2.5 V VREF1 and 3.3 V～5 V VREF2
  - 3.3 V VREF1 and 5 V VREF2
- Bidirectional voltage translation with no direction pin
- Low 3.5 ohm ON-state connection between input and output ports provides less signal distortion
- 5 V tolerant I²C-bus I/O ports to support mixed-mode signal operation
- Lock-up free operation for isolation when EN = LOW
- Flow through pin out for ease of printed-circuit board trace routing
- ESD protection exceeds 4000V HBM
- Extended Temperature: -40°C to +85°C

Block Diagram

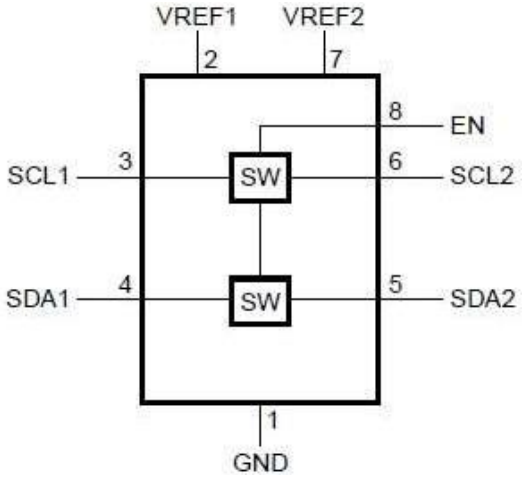


Figure 1: Block Diagram

Description

The RS7LS9306 is a dual bidirectional I²C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.3 V (V_{REF1}) and 1.8 V to 5.5 V(V_{REF2}).

The RS7LS9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high- impedance state exists between ports.

The RS7LS9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The RS7LS9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

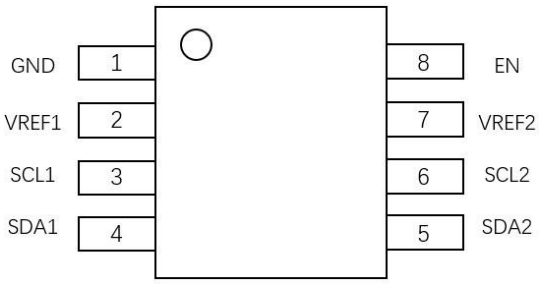
Ordering Information

Part Number	Package	Description
RS7LS9306ZEE	DFN-8	8-pin, 2.0x3.0 mm
RS7LS9306TE	SOT23-8	8-Pin, SOT23

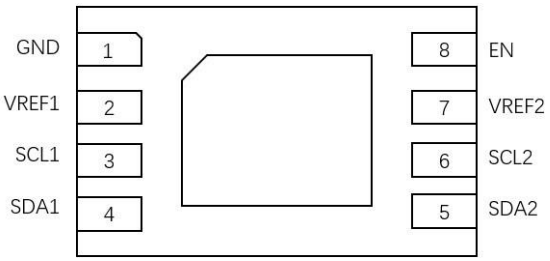
Notes:
1. E = Pb-free and Green

Pin Configuration

SOT23-8（Top view）



DFN-8 (Top view)



Pin Name	Pin NO. SOT23	Pin NO. DFN-8	Description
GND	1	1	Ground
V_{REF1}	2	2	Reference voltage 1
SCL1	3	3	Serial Clock 1
SDA1	4	4	Serial Data 1
SDA2	5	5	Serial Data 2
SCL2	6	6	Serial Clock 2
V_{REF2}	7	7	Reference voltage 2
EN	8	8	Output enable (active High)

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	−65	-	+150	°C
V_{CCA}	DC Supply Voltage port B	-0.3	-	6.0	V
V_{CCB}	DC Supply Voltage port A	-0.3	-	6.0	V
V_{IOB}	Vi(A) referenced DC Input / Output Voltage	-0.3	-	6.0	V
V_{IOB}	Vi(B) referenced DC Input / Output Voltage	-0.3	-	6.0	V
V_{EN}	Enable Control Pin DC Input Voltage	-0.3	-	6.0	V
I_{CH}	Channel Current			128	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
$V_{I/O}$	Voltage on an input/output pin	0	-	5.5	V
V_{REF1}	Reference voltage1	0	-	5.5	V
V_{REF2}	Reference bias voltage 2	0	-	5.5	V
$V_{I(EN)}$	Input voltage on pin EN	0	-	5.5	V
$I_{(pass)}$	Pass switch current	-	-	64	ns/V
T_A	Ambient temperature	-40	-	125	°C

DC Electrical Characteristics

T_A = -40 °C to +125 °C; unless otherwise specified

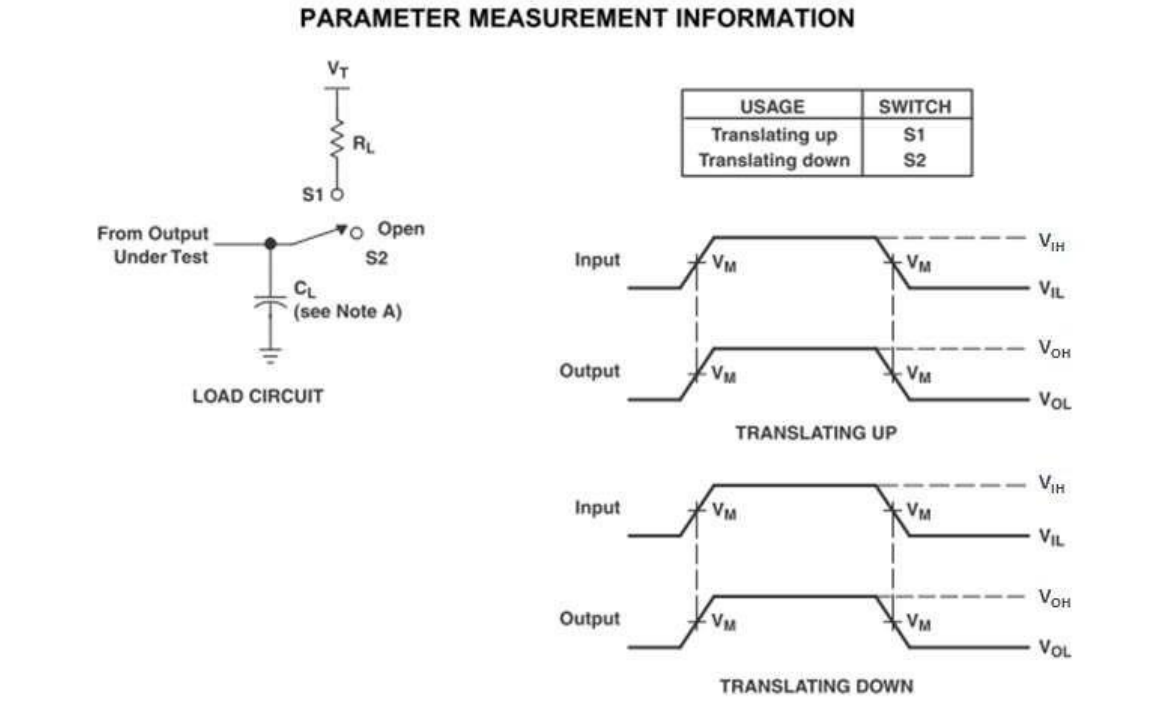
Parameter	Description	Test Conditions (1)		MIN	TYP (2)	MAX	Unit
Input and output SDAB and SCLB							
V_{IK}	input clamping voltage	I_I = -18mA; $V_{I(EN)}$ = 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; $V_{I(EN)}$ = 0 V		-	-	5	µA
$C_{i(EN)}$	input capacitance on pin EN	V_I = 3 V or 0 V		-	11	-	pF
$C_{io(off)}$	Off-state input/output capacitance (SCLn, SDAn)	V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		-	4	-	pF
$C_{io(on)}$	on-state input/output capacitance(SCLn, SDAn)	V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		-	10.5	-	pF
Ron	ON-state resistance(2) (SCLn, SDAn)	V_I = 0V; I_O =64mA	$V_{I(EN)}$ = 4.5 V	-	3.5	5.5	Ω
			$V_{I(EN)}$ = 3 V	-	4.7	7	Ω
			$V_{I(EN)}$ = 2.3 V	-	6.3	9.5	Ω
			$V_{I(EN)}$ = 1.5 V	-	60	140	Ω
		V_I = 2.4V; I_O=15mA	$V_{I(EN)}$ = 4.5 V	1	6	15	Ω
			$V_{I(EN)}$ = 3 V	20	60	140	Ω
		V_I = 1.7V; I_O = 15mA	$V_{I(EN)}$ = 2.3 V	20	60	140	Ω

Notes:
1. All typical values are at T_A = 25 °C.
2. Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

AC characteristics

T_A = -40 °C to +125 °C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
Dynamic characteristics (translating down)									
$V_{I(EN)}$ = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.2	0	1	0	0.5	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.3	0	1	0	0.6	ns
Dynamic characteristics (translating up)									
$V_{I(EN)}$ = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_T = 3.3 V; V_M = 1.15 V;									
t_{PLH}	LOW-to-HIGH propagation delay	ffrom (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.4	0	1.1	0	0.7	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_T = 2.5 V; V_M = 0.75 V;									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.3	0	1.3	0	0.8	ns



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure.2 Load Circuit for Outputs

Functional Description

The RS7LS9306 is a dual bidirectional I^2C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2 V to 3.3 V (VREF1) and 1.8 V to 5.5 V(VREF2).

The RS7LS9306 allows bidirectional voltage translations between 1.2 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high- impedance state exists between ports.

The RS7LS9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The RS7LS9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The RS7LS9306 can also be used to run two buses, one at 400kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The RS7LS9306 has a standard open-collector configuration of the I^2C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I^2C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Application Information

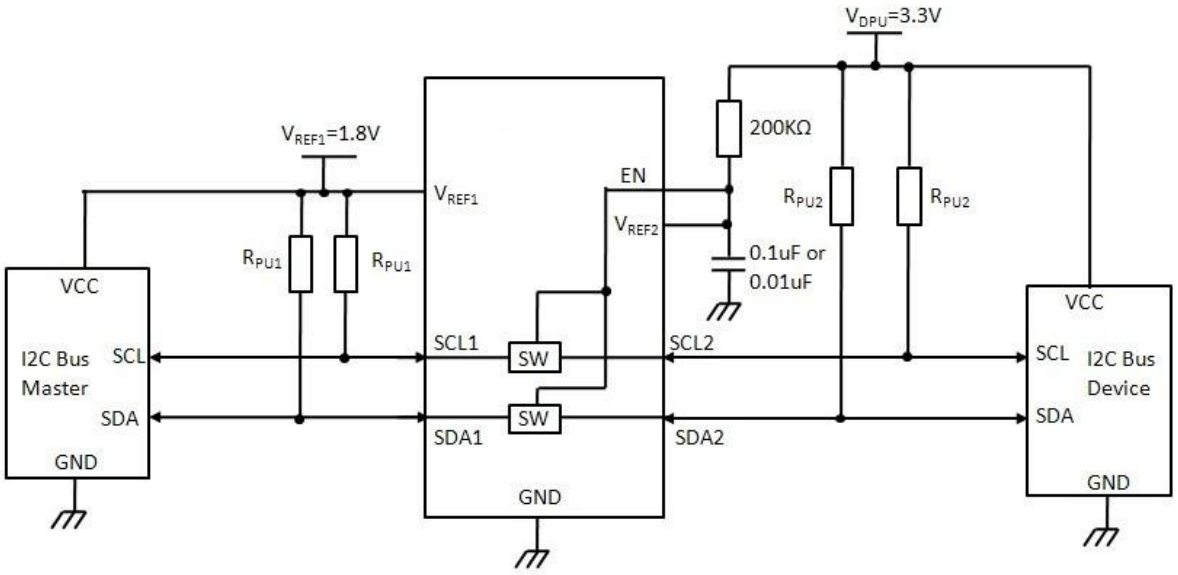


Figure.3 Typical Open Drain Application Circuit (Switch Always Enabled)

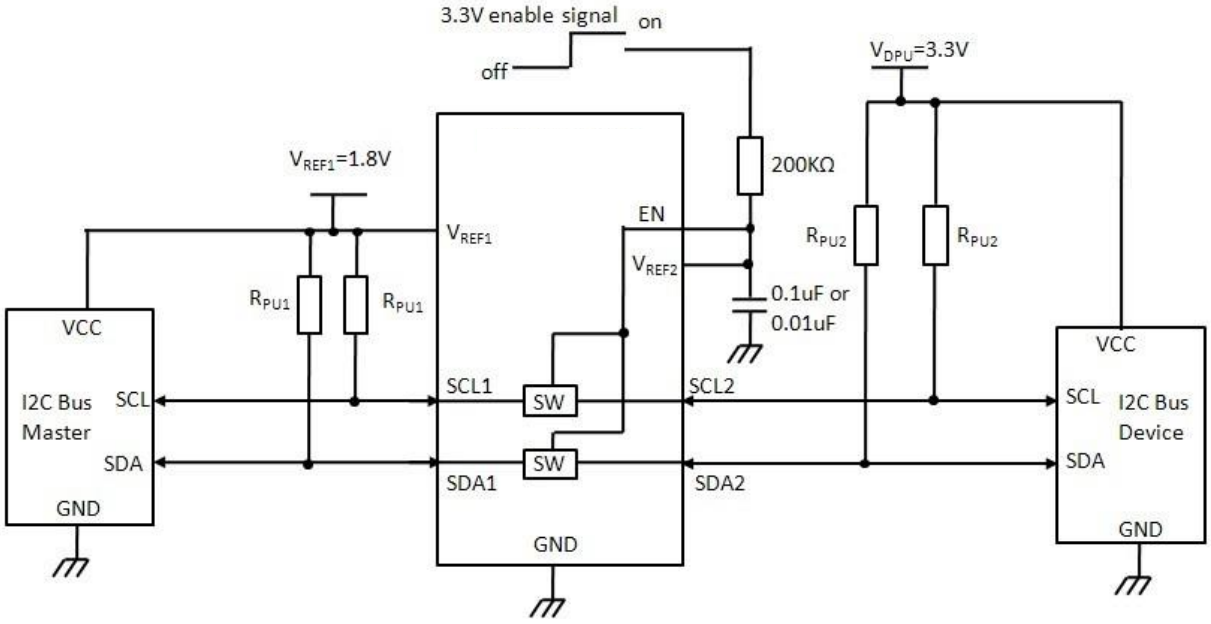


Figure.4 Typical Open Drain Application Circuit (Switch Enabled Control)

Open Drain Application

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to high-side VDPU through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended.

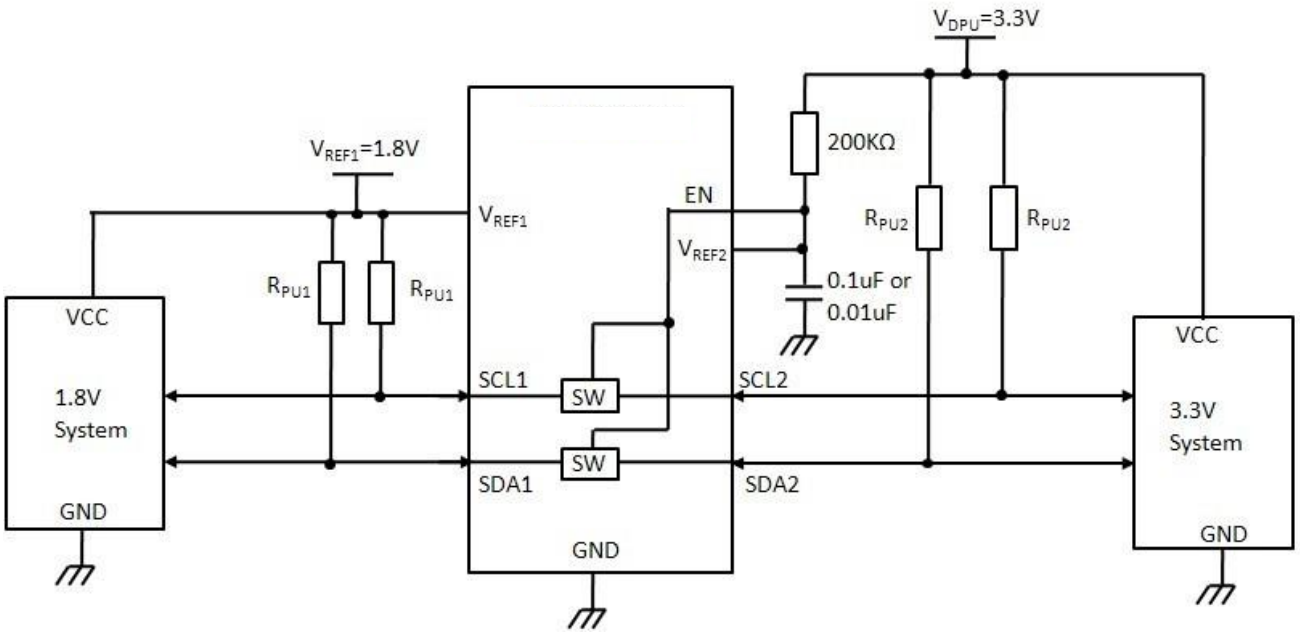


Figure.5 Typical push-pull Application Circuit (Switch Enabled Control)

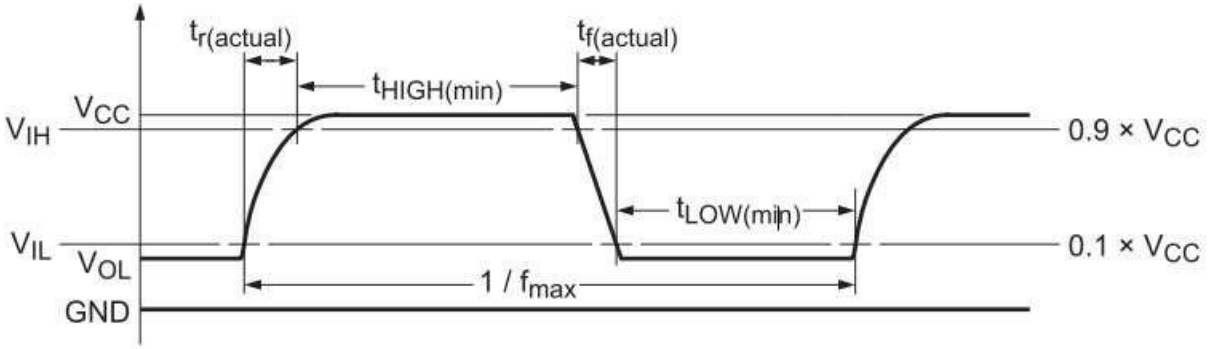
Push Pull Application

If used in push-pull system, the pull-up resistors on REF side are also needed. The data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction.

MAX Frequency Application

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(\max) = \frac{1}{\mathrm{tLOW(min)} + \mathrm{tHIGH(min)} + \mathrm{tr(actual)} + \mathrm{tf(actual)}}$$



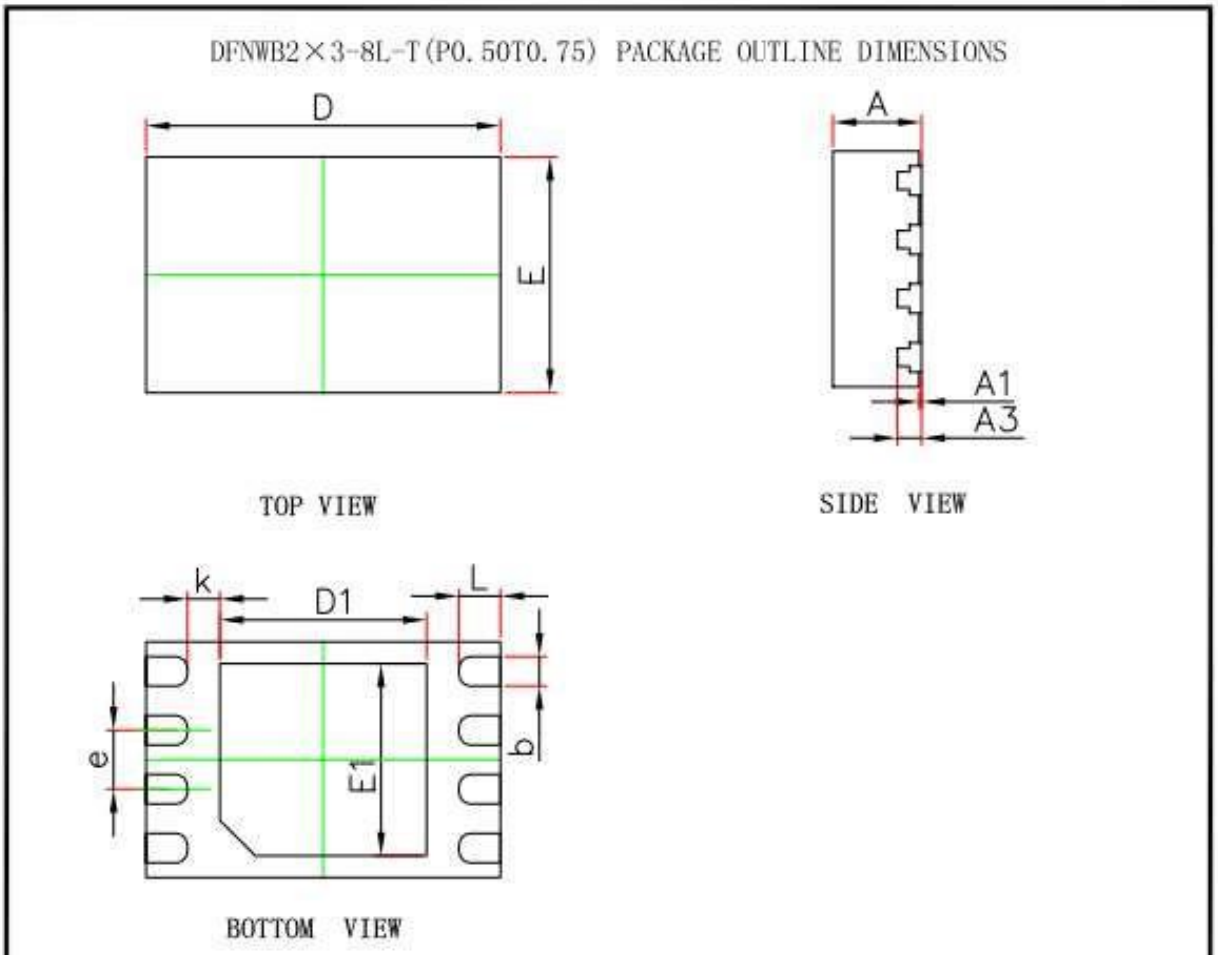
The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (CL) and the pull-up resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus.
Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.
The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.
There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the RS7LS9306 close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

Package Information

DFN 2x3-8L

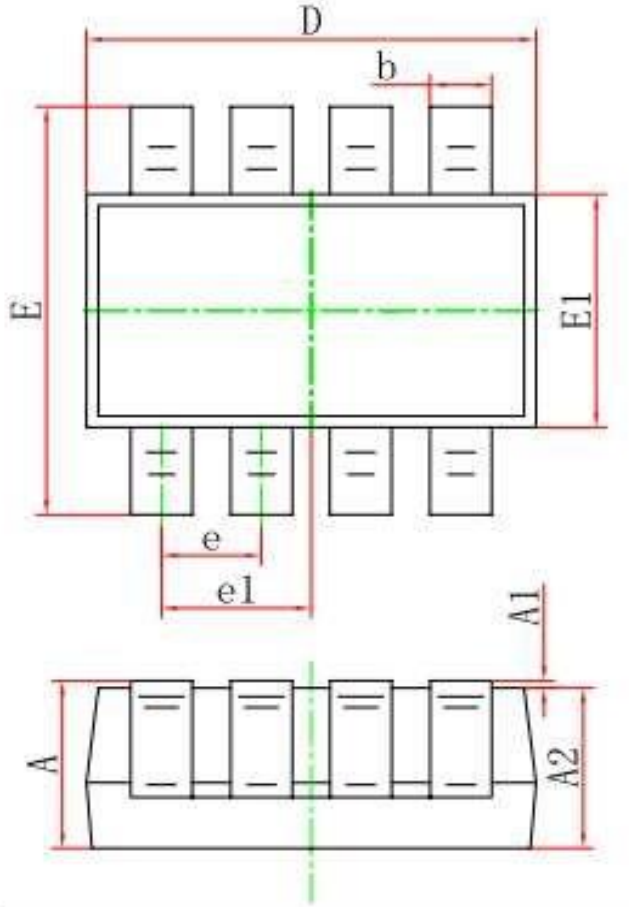


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.950	3.050	0.116	0.120
E	1.950	2.050	0.077	0.081
D1	1.650	1.850	0.065	0.073
E1	1.530	1.730	0.060	0.068
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
k	0.275REF		0.011REF	
L	0.300	0.400	0.012	0.016

Mar. 2016, REV. A

SOT23-8L

SOT-23-8L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.650BSC.		0.026BSC.	
e1	0.975BSC.		0.038BSC.	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Nov. 2018,Rev.A

Revision History

Revision	Description	Date
0.3	Initial release	2023/4/23
1.0	Modify the package description from 12-pin to 8-pin (Page 1)	2023/9/26