Preliminary Datasheet
RS2CG284Q
PCIE Clock Generator

Features

- 3.3V Supply Voltage
- Crystal/CMOS Input: 25 MHz
- Four Differential Low-Power HCSL Outputs with On-Chip Termination
- Default ZOUT = 85Ω
- Two reference CMOS Outputs
- Programmable Slew Rate and Output Amplitude for Each Output
- Selectable 0%, -0.25%, or -0.5% Spread on Differential Outputs
- Differential Output-To-Output Skew <60ps
- Very-Low Jitter Outputs à Differential phase Jitter
  < 0.3ps RMS, SSC off
  < 1.5ps RMS, SSC on
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device
- Available in 32-TQPN package
- -40° to +125°C temperature operation
- AEC-Q 100 qualified, Automotive Grade 1suppor; PPAP capable, and manufactured in IATF 16949 certified facilities

Description

The RS2CG284Q is an 4-output differential Low-Power HCSL Outputs and 2-CMOS outputs, very-low-power PCIe Gen1/ Gen2/Gen3/Gen4/Gen5 clock generator.

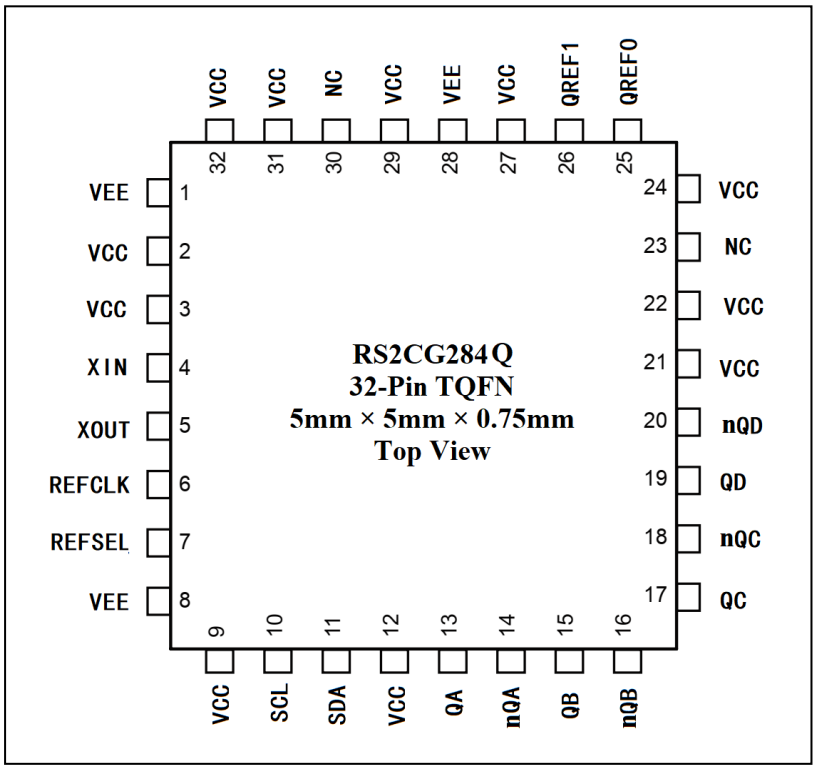
It uses a 25MHz crystal or CMOS reference as an input to generate the 100MHz low-power differential LP-HCSL outputs with on-chip terminations and 2 channels 25MHz LVCMOS buffered reference outputs are provided to serve as a low-noise reference for other circuitry.

It uses RSM's proprietary PLL design to achieve very-low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4/Gen5 requirements. It also provides various options, such as different slew rate and amplitude through SMBUS, so users can easily configure the device to get the optimized performance for their individual boards. The device also supports selectable spread spectrum options to reduce EMI for various applications.

Order information

Ordering Code	Package	Package Description	
RS2CG284QZHE	ZH	TQFN-32L	5X5mm

Pin Configuration



Functional Block Diagram

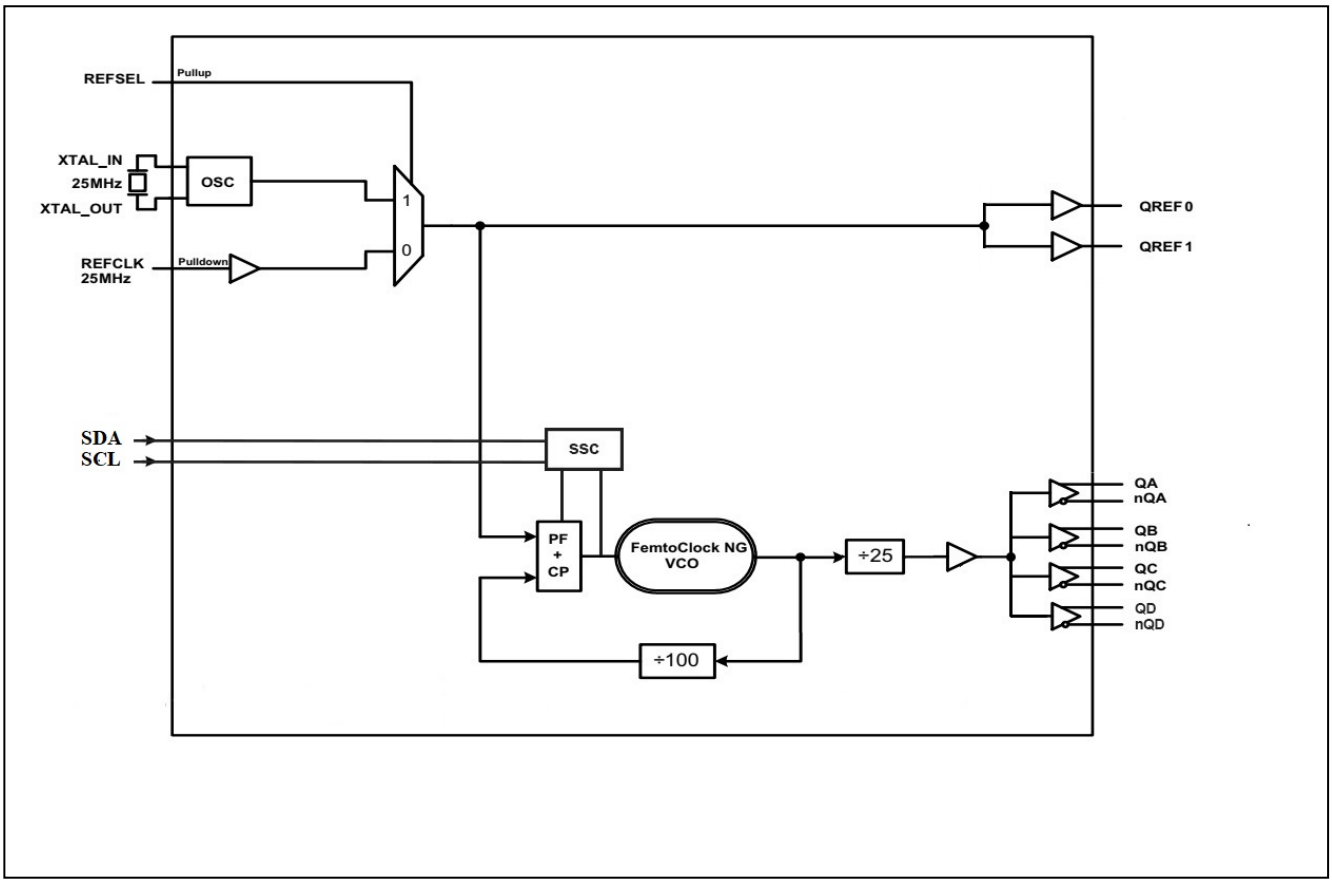


Table 1: Pin Descriptions

Number	Name	Type		Description
1, 8, 28	V_{EE}	Power		Negative supply pins.
2, 3, 9, 12, 21,22,24,27, 29,31,32	V_{CC}	Power		Power supply pins. Pins 2,27 – power supply connection for the 25MHz LVCMOS outputs Pin 3 – power supply connection for the crystal oscillator Pin 9,12,21,22,24 – power supply connection for the LP-HCSL differential outputs Pins 29 – power supply connection for the divider Pin 31,32 – power supply connection for the PLL
25,26	QREF0, QREF1	Output		Single-ended outputs. 3.3V LVCMOS/LVTTL reference levels.
4,5	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
6	REFCLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
7	REFSEL	Input	Pullup	Reference select pin. When HIGH, selects crystal. When LOW, selects REFCLK. LVCMOS/LVTTL interface levels.
10,11	SCL, SDA	I/0		SMBUS communication
23,30	nc			No connect.
13,14	QA, nQA	Output		Differential output pair. LP-HCSL interface levels.
15,16	QB, nQB	Output		Differential output pair. LP-HCSL interface levels.
17,18	QC, nQC	Output		Differential output pair. LP-HCSL interface levels.
19,20	QD, nQD	Output		Differential output pair. LP-HCSL interface levels.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Min	Typ.	Max	Units
C_{IN}	Input Capacitance		Crystal Not Included		2		pF
C_{PD}	Power Dissipation Capacitance (per output)	QREF [0:1]	V_{CC} = 3.6V		6		pF
R_{PULLUP}	Input Pullup Resistor				51		k
$R_{PULLDOWN}$	Input Pulldown Resistor				51		k
R_{OUT}	Output Impedance	QREF [0:1]			33		

Table 3A. REFSEL Function Table

Inputs	**Input Source**
REFSEL	
0	REFCLK
1(default)	XTAL_IN, XTAL_OUT

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, VDDxx .....–0.5V to +4.6V
Input Voltage .....–0.5V to VDD+0.5V, not exceed 4.6V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 4000V
Max Junction Temperature…….....+125ºC

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_A	Ambient air temperature	-40		125	C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
VCC	Power Supply Voltage		3.0	3.3	3.6	V
ICC	Power Supply Current	No Load			200	mA

Table 4B. LVCMOS DC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
V_{IH}	Input High Voltage	REFSEL	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	REFSEL	-0.3		0.8	V

Symbol	Parameter		Test Conditions	Min	Typ.	Max	Units
IIH	Input High Current	REFCLK	VCC = VIN = 3.6V			150	µA
		REFSEL	VCC = VIN = 3.6V			5	µA
IIL	Input Low Current	REFCLK	VCC = 3.6V, VIN = 0V	-5			µA
		REFSEL	VCC = 3.6V, VIN = 0V	-150			µA
VOH	Output High Voltage;		VCC = 3.3V ± 0.3V	2.3			V
VOL	Output Low Voltage;		VCC = 3.3V ± 0.3V			0.8	V

Table 4C. LP-HCSL DC Characteristics, V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
VOH	Output High Voltage;		660		850	mV
VOL	Output Low Voltage;		-150		150	mV
Vomax	Output Maximum Voltage;			820	1150	mV
Vomin	Output Minimum Voltage;		-300	-42		mV
Voc	Output Cross Voltage;		250	380	550	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Min	Typ.	Max	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. LP-HCSL AC Characteristics, V_{CC}= 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 125°C

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
fIN	Input Frequency			25		MHz
fOUT	Output Frequency	LP-HCSL		100		MHz
Tjc-c	Cycle to cycle Jitter			20	60	ps
tsk(o)	Output Skew; NOTE 2, 3	Measured on the Rising Edge			50	ps
tR / tF	Slew rate	+/-150mV window		3		V/ns
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

Table 6B. AC Characteristics for Single Side Band Power Levels (LP-HCSL Outputs),
V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
tjPHASE	Integrated Phase Jitter (RMS)	PCIe Gen 1	20	25	86	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz	0.8	0.9	3.0	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)	1.5	1.6	3.1	ps
		PCIe Gen3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)	0.4	0.5	1	ps
		PCIe Gen3 Separate Reference No Spread (PLL BW of 2-4 or 2-5MHz, CDR=10 MHz)	0.4	0.5	0.7	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)	0.3	0.37	0.5	ps
		PCIe Gen 5(7) (PLL BW of 500k to 1.8MHz. CDR = 20MHz)	0.02	0.05	0.15	ps
tjPH-SRISG2	Integrated Phase Jitter (RMS), -0.25%Spread	PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz)	0.6	0.92	2	ps
tjPH-SRISG3	Integrated Phase Jitter (RMS), -0.25% Sprea	PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz, CDR=10MHz)	0.32	0.4	0.7	ps
tjPH-SRISG2	Integrated Phase Jitter (RMS), -0.5% Spread	PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz)	0.8	1.1	2	ps
tjPH-SRISG3	Integrated Phase Jitter (RMS), -0.5% Spread	PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz, CDR=10MHz)	0.35	0.6	0.7	ps

Table 6C. LVCMOS AC Characteristics, V_{CC} = 3.3V ± 0.3V, T_A = -40°C to 125°C

Symbol	Parameter		Test Conditions	Min	Typ.	Max	Units
f_{IN}	Input Frequency				25		MHz
f_{OUT}	Output Frequency				25		MHz
tjit	RMS Phase Jitter (Random)		25MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 5MHz		0.140		ps
*t*sk(o)	Output Skew;	QREF [0:1]	Measured on the Rising Edge			50	ps
PSNR	Power Supply Noise Reduction	Pin 40, (V_{CC})	From DC to 6.25MHz		-80		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%		1.0	1.5	ps
odc	Output Duty Cycle			45		55	%

Table 6D. AC Characteristics for Single Side Band Power Levels (LVCMOS Outputs),
V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = 25°C

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
N(1k)	Single-side band phase noise, 1kHz from Carrier	25MHz		-137		dBc/Hz
N(10k)	Single-side band phase noise, 10kHz from Carrier			-153		dBc/Hz
N(100k)	Single-side band phase noise, 100kHz from Carrier			-162		dBc/Hz
N(1M)	Single-side band phase noise, 1MHz from Carrier			-163		dBc/Hz
N(5M)	Single-side band phase noise, 5MHz from Carrier			-163		dBc/Hz

SMBus Serial Data Interface

RS2CG284 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below. Read and write block transfers can be stopped after any complete byte transfer

Address Assignment

A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	R/W
1	1	0	1	0	0	0	0/1

How to Write

1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit		8 bit	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	……	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	8 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bit	1 bit	1 bit
……..	Data Byte (N+X-1)	NAck	Stop bit

SMBus Table: Output Enable Control 0

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7			RW			1
Bit 6			RW			1
Bit 5			RW			1
Bit 4			RW			1
Bit 3	OE_OUTA		RW			1
Bit 2	OE_OUTB		RW			1
Bit 1	OE_OUTC		RW			1
Bit 0	OE_OUTD		RW			1

SMBus Table: Output status Control 1

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SLEW RATE OF HCSL	HCSL SLEW RATE CONTROL	RW	Slow setting	Fast setting	0
Bit 6	STOP1	HCSL stop mode control	RW	00=low/low; 01=hiz/hiz; 10=high/low; 11=low/high		0
Bit 5	STOP0		RW			0
Bit 4	HCSL PD	HCSL PD MODE	RW	normal	pd	0
Bit 3						0
Bit 2						0
Bit 1						0
Bit 0	REF HIZ	REF CMOS HIZ MODE	RW	0=normal	1=REF HIZ	0

SMBus Table: Reserved

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 4	Name		Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW	Pin Low	Pin High	0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Vendor/Revision Identification Control

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	Rev A = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	Vendor ID	R	rsm = 0011		0
Bit 2	VID2		R			0
Bit 1	VID1		R			1
Bit 0	VID0		R			1

SMBus Table: Device ID Control

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	DID7		R			0
Bit 6	DID6		R			0
Bit 5	DID5	Device ID	R			0
Bit 4	DID4		R			0
Bit 3	DID3		R			0
Bit 2	DID2		R			1
Bit 1	DID1		R			1
Bit 0	DID0		R			1

SMBus Table: Byte Count Control

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	BC5	Writing to this register configures how many bytes will be read back	RW	Default value is 8		0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

SMBus Table: Reserved

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6			RW			0
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 17	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

SMBus Table: PWRGD Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	PWRGD_PDB_POL	Sets PWRGD_PD# polarity	RW	Power down when low	Power down when high	0
Bit 6	PWRGD	power good	RW	power down	power good	1
Bit 5			RW			0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: Reserved

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

SMBus Table: SSC Control

Byte 20	Name	Control Function	Type	0	1	Default
Bit 7			RW			0
Bit 6	SSC_DIV6	SSC clk divider ratio = N*2+1 Fssc = Fpfd_FB / (N*2+1) /12 B20[1] is RO/RW when B20[7]=0/1	RW	Divide ratio = decimal value x 2 + 1		1
Bit 5	SSC_DIV5		RW			0
Bit 4	SSC_DIV4		RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1			RW			0
Bit 0			RW			0

SMBus Table: SSC and EFUSE Control

Byte 21	Name	Control Function	Type	0	1	Default
Bit 7	SSC_PD	SSC block power down valid if CG and Byte 1 is SSC mode	RW	Normal	Power down	0
Bit 6	SSC_EN_SW1	SSC_EN SW contol	RW	00 = SSC off	10 = Reserved (SS Off)	0
Bit 5	SSC_EN_SW0		RW	01 = -0.3% SS	11 = -0.5% SS	0
Bit 4			RW			0
Bit 3			RW			0
Bit 2			RW			0
Bit 1	Reserved	Write not allowed	RW	00 = ACCESS0 / ACCESS0	10 = OUTPUT1 / ACCESS1	0
Bit 0	Reserved		RW	01 = RE / PEB	11 = OUTPUT0 / ADDR0	0

Plots 25MHz LVCMOS Clock (12k to 5MHz)

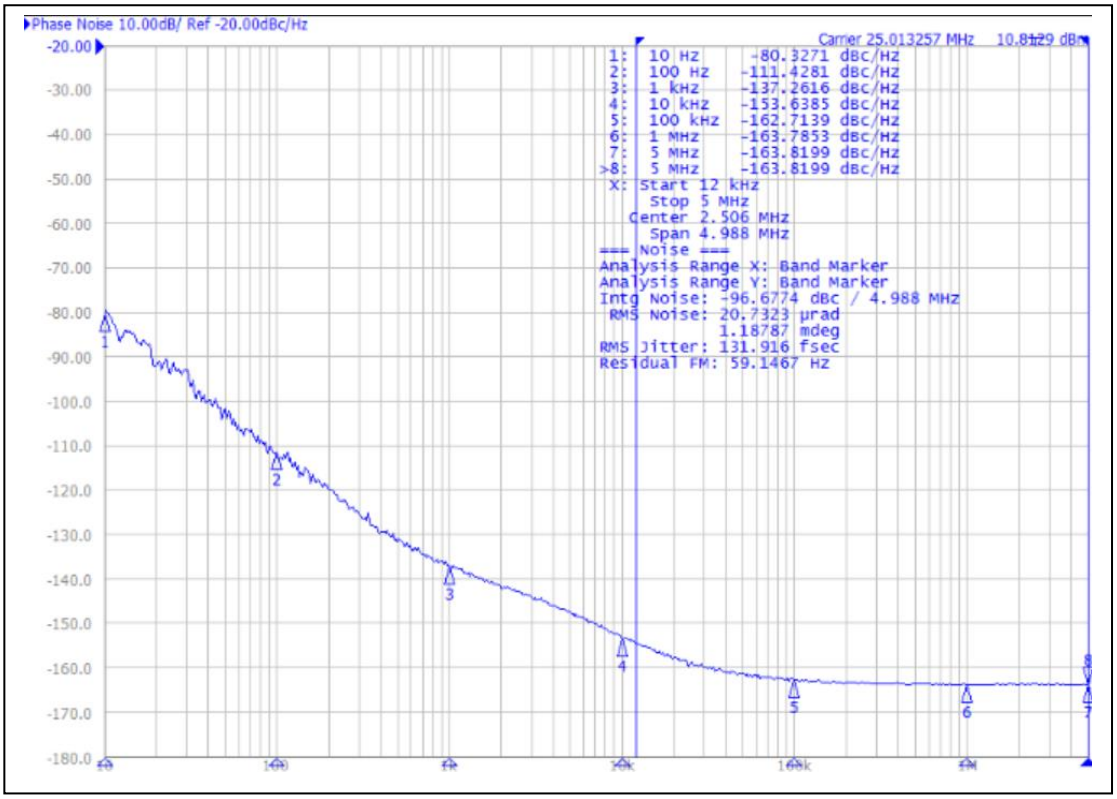


Figure 1. Low-Power HCSL Test Circuit

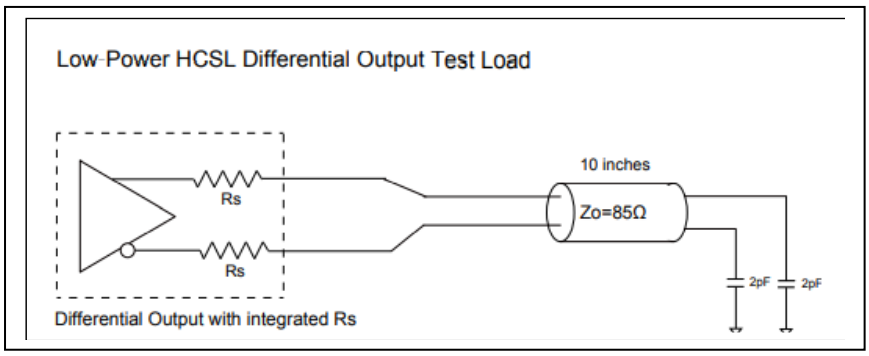


Figure 2. CMOS REF Test Circuit

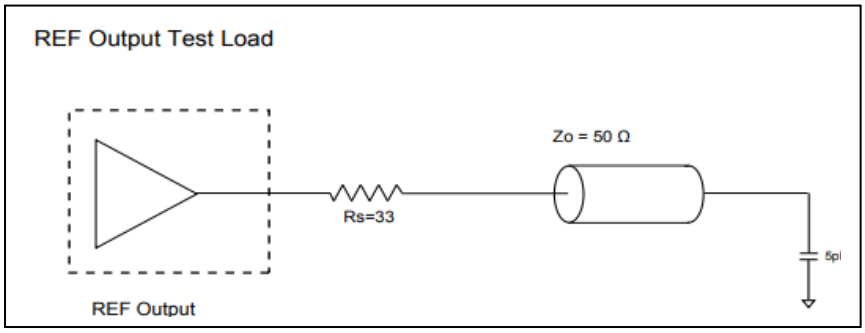
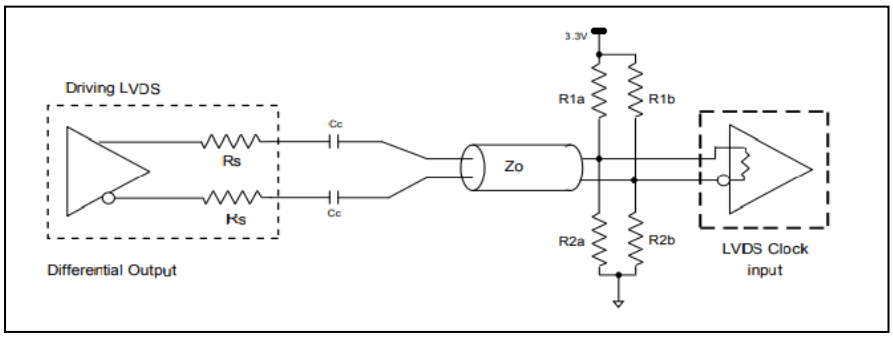


Figure 3. Differential Output Driving LVDS



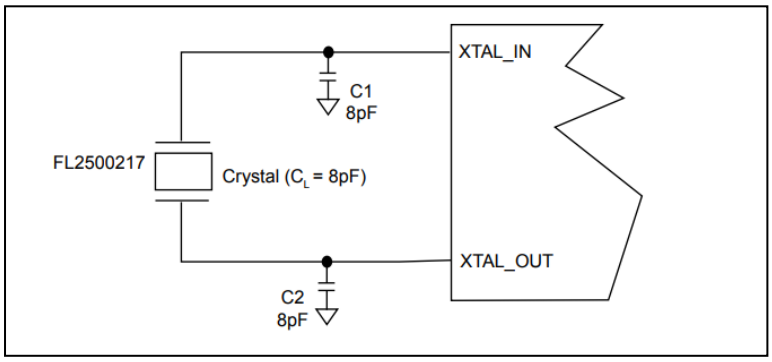
Alternate Differential Output Terminations (Zo = 85Ω)

Component	Receiver with Termination	Receiver without Termination	Unit
R1a, R1b	10,000	130	Ω
R2a, R2b	5600	64	Ω
CC	0.1	0.1	uF
VCM	1.2	1.2	V

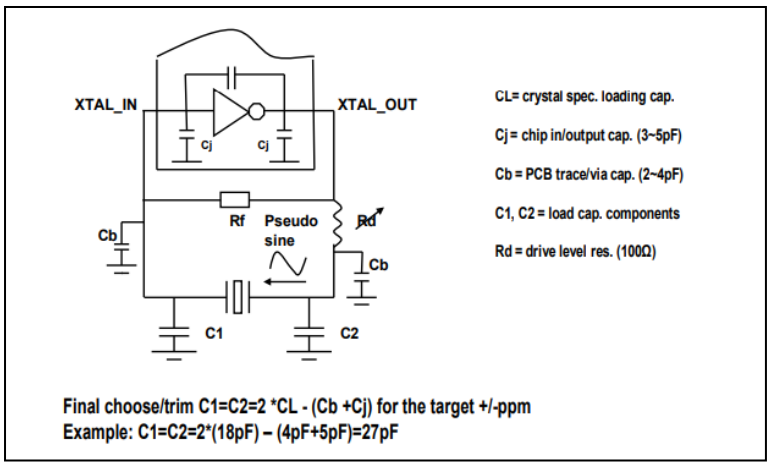
Crystal Circuit Connection

The following diagram shows RS2CG284 crystal circuit connection with a parallel crystal. For the CL=8pF crystal, it is suggested to use C1=8pF and C2=8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

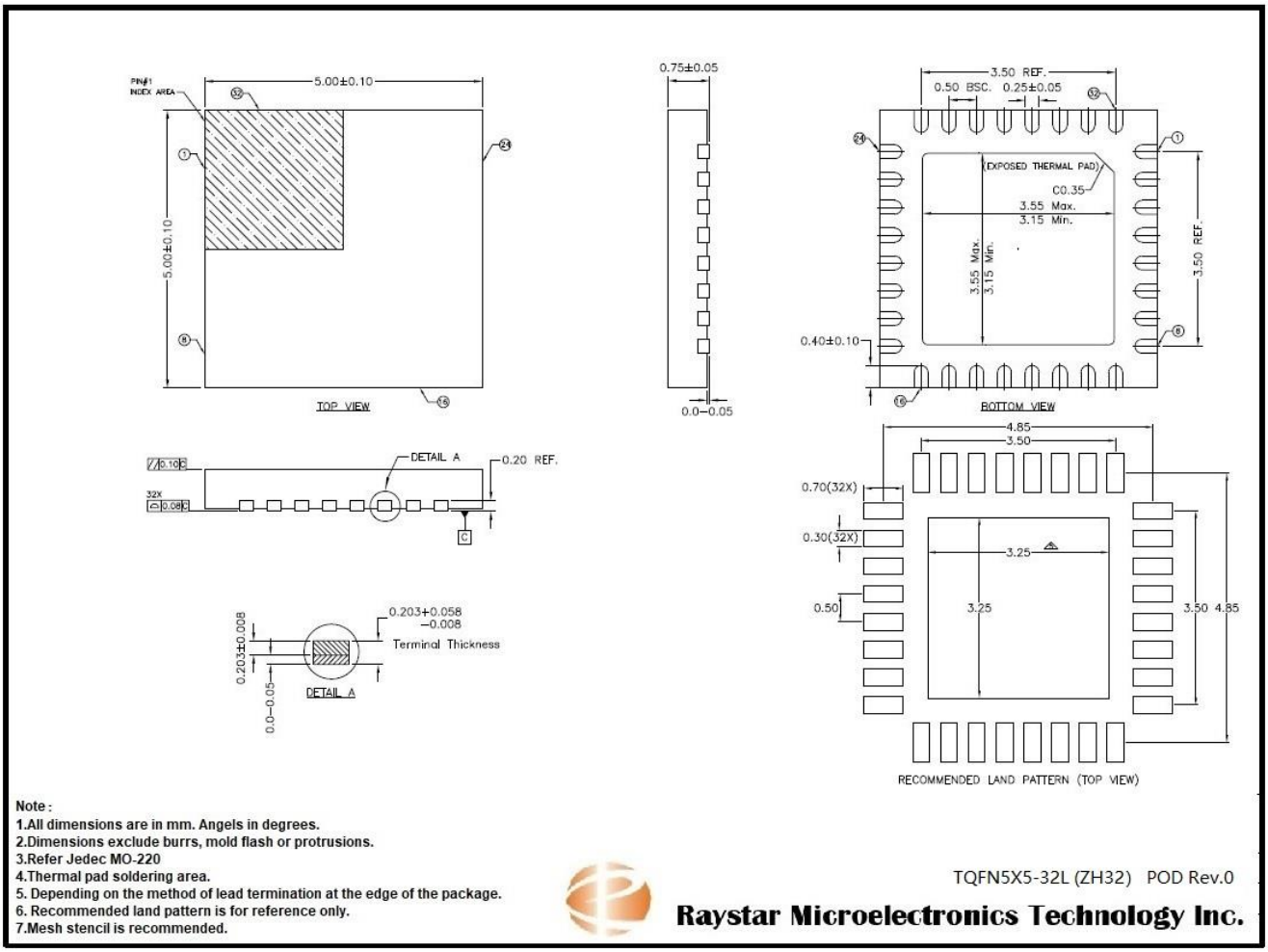
Crystal Oscillator Circuit



Crystal Capacitor Calculation



Packaging Mechanical: 32-TQFN (ZH32)



Revision History

Revision	Description	Date
0	Initiated	2023/9/18