RS2CG5705B

PCIe 3.0 Clock Generator with 4 HCSL Outputs

Features

- PCIe 3.0 compliant
- PCIe 3.0 Phase Jitter -0.45 ps RMS
- LVDS compatible outputs
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 40ps cycle-to-cycle (typ)
- Spread of -0.5%, -1.0%, -1.5%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)
- 20-pin TSSOP (L20)

Application

- Cloud/High-performance Computing
- nVME Storage
- Network
- Accelerators

Block Diagram

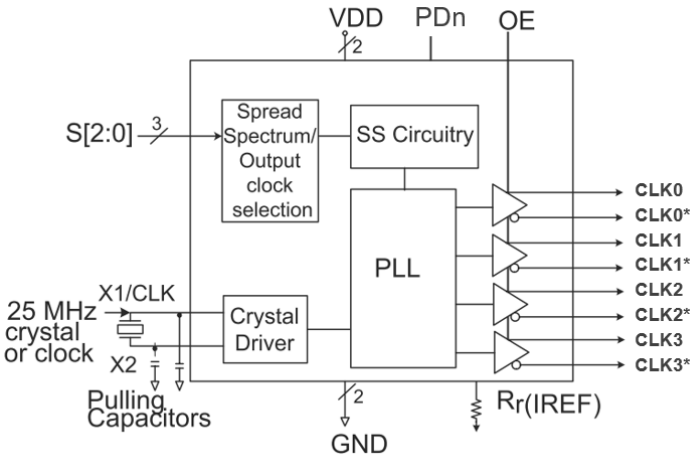


Figure 1 Block Diagram

Description

The RS2CG5705B is a spread spectrum clock generator compliant to PCI Express 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The RS2CG5705B provides four differential (HCSL) or LVDS spread spectrum outputs. The RS2CG5705B is configured to select spread and clock selection. Using Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 100MHz, and 200MHz clock frequencies. It also provides spread selection of -0.5%, -1.0%, -1.5% and no spread.

Ordering Information

Ordering Code	Package	Package Description
RS2CG5705BLE	L	TSSOP 20

Notes

[1] E = Pb-free and Green

Pin Configuration

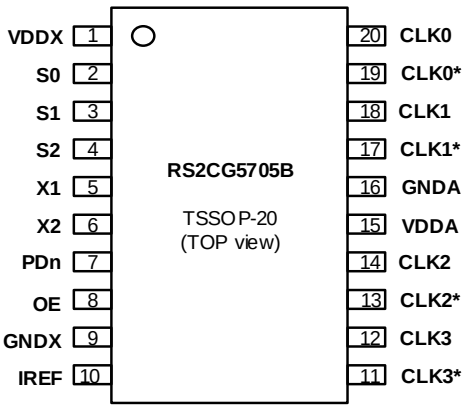


Figure 2 Pin Configuration

Pin No.	Pin Name	I/O Type	Description
1	VDDX	Power	Connect to +3.3V source.
2	S0	Input	Spread Spectrum Select pin #0. Internal pull-up resistor.
3	S1	Input	Spread Spectrum Select pin #1. Internal pull-up resistor.
4	S2	Input	Spread Spectrum Select pin #2. Internal pull-up resistor.
5	X1	Input	Crystal connection.
6	X2	Output	Crystal connection.
7	PDn	Input	Power down. Internal pull-up resistor.
8	OE	Input	Output enable. Tri-states output (High=enable outputs); Low=disable outputs). Internalpull-up resister.
9	GNDX	Power	Connect to digital circuit ground.
10	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
11	CLK3*	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 3.
12	CLK3	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 3.
13	CLK2*	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 2.
14	CLK2	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 2.
15	VDDA	Power	Connect to a +3.3V analog source.
16	GNDA	Power	Output and Analog circuit ground
17	CLK1*	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 1.
18	CLK1	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 1.
19	CLK0*	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 0.
20	CLK0	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 0.

Table1 Spread Selection Table

S2	S1	S0	Spread %	Spread Type	Output Frequency
0	0	0	-0.5	Down	100
0	0	1	-1.0	Down	100
0	1	0	-1.5	Down	100
0	1	1	No Spread	Not Applicable	100
1	0	0	-0.5	Down	200
1	0	1	-1.0	Down	200
1	1	0	-1.5	Down	200
1	1	1	No Spread	Not Applicable	200

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	−65	-	+150	°C
V_{DD}	DC Supply Voltage port B	-0.5	-	5.5	V
V_{IO}	Input / Output Voltage	-0.5	-	VDD+0.5	V
ESD	ESD HBM protection (input)	2000			V

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	V_{CCA} Positive DC Supply Voltage	3.0	-	3.6	V
V_I	Control Pin Input Voltage	-0.3	-	3.6	V
T_A	Operating Temperature Range	−40	-	+125	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 85°C, 3.0V≤V_{DD}≤3.6V

Symbol	Parameter	Conditions		MIN	TYP	MAX	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IH}	Input High Voltage(1)	OE, S0, S1, S2		0.7VDD		VDD +0.3	V
V_{IL}	Input Low Voltage(1)	OE, S0, S1, S2		GND -0.3		0.3VDD	V
I_{IL}	Input Leakage Current	0 ≤ Vin ≤ VDD	Without input pull-up and pull-downs	-5		5	µA
I_{DD}	Operating Supply Current	R_L = 50Ω, C_L = 2pF			105	130	mA
I_{DDOE}		OE = LOW			40	50	mA
I_{DDPD}	Power down Current	No pad load, PDn=LOW			60	100	µA
C_{IN}	Input Capacitance					7	pF
C_{OUT}	Output Capacitance					6	pF
L_{PIN}	Pin Inductance					5	nH
R_{OUT}	Output Resistance	CLK Outputs		3.0			kΩ

Note:
1. R_L= 50 ohm with C_L =2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

HCSL Output AC Characteristics

(V_{DD} = 3.3V ±10%, TA = -40°C to +85°C)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
FIN	Input Frequency			25		MHz
VOUT	Output Frequency	S2=HIGH			200	MHz
		S2=LOW			100	MHz
VOH	Output High Voltage (1,2)	100 MHz HCSL output @ VDD =3.3V	660	800	900	mV
VOL	Output Low Voltage(1,2)		-150	0	150	mV
VCPA	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
VCN	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
JCC	Jitter, Cycle-to-Cycle(1,3)			40	60	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		2.1	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.38	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.48	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.47	1	ps
MF	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
tOR	Rise Time(1,2)	From 0.175V to 0.525V	150	332	700	ps
tOF	Fall Time(1,2)	From 0.525V to 0.175V	150	344	700	ps
TSKEW	Skew between outputs	At Crossing Point Voltage			50	ps
TDUTY-CYCLE	Duty Cycle(1,3)		45		55	%
TOE	Output Enable Time(5)	All outputs			10	µs
TOT	Output Disable Time(5)	All outputs			10	µs
tSTABLE	From power-up to VDD=3.3V	From Power-up VDD=3.3V		3.0		ms
tSPREAD	Setting period after spread change	Setting period after spread change		3.0		ms

Note:
1. R_L= 50 ohm with C_L =2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between each VDD pin and the ground plane and placed as close to the VDD pin as possible.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors

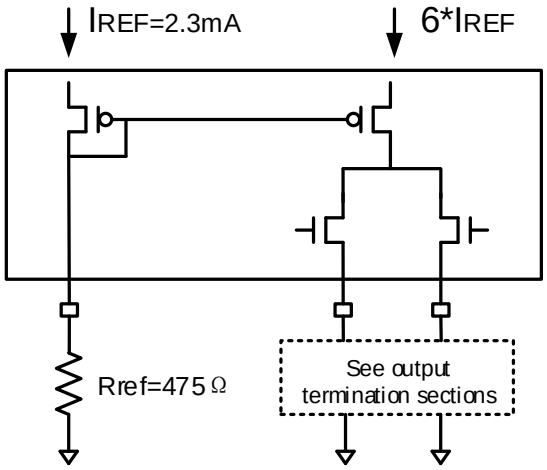
C_L = Crystals' load capacitance in pF Crystal Capacitors (pF) = (C_L - 8) *2

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16-8)*2=16.

Current Source (IREF) Reference Resistor – Rref

If board target trace impedance is 50Ω,

then Rref = 475Ω providing an IREF of 2.32 mA. The output current (IOH) is 6*IREF.

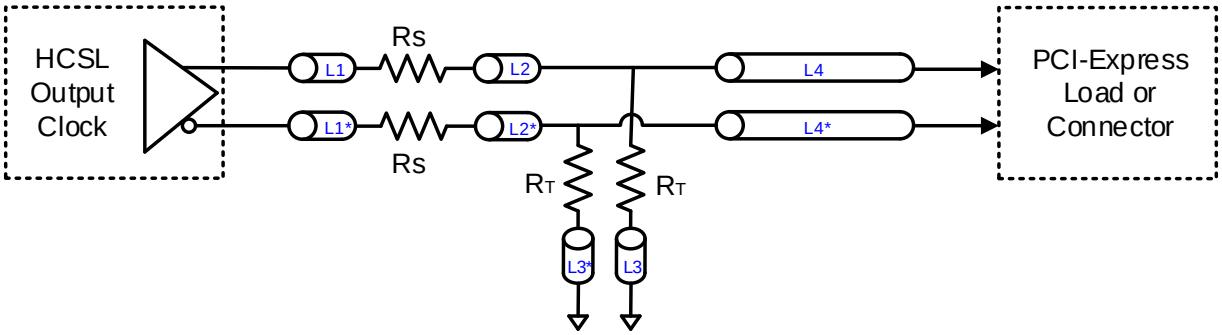


Output Termination

The PCI Express differential clock outputs of the RS2CG5705B are open-source drivers and require an external series resistor and a resistor to ground. These resistor values and their allow- able locations are shown in detail in the PCI Express Layout Guidelines section.

The RS2CG5705B can be configured for LVDS compatible volt- age levels. See the LVDS Compatible Layout Guidelines section.

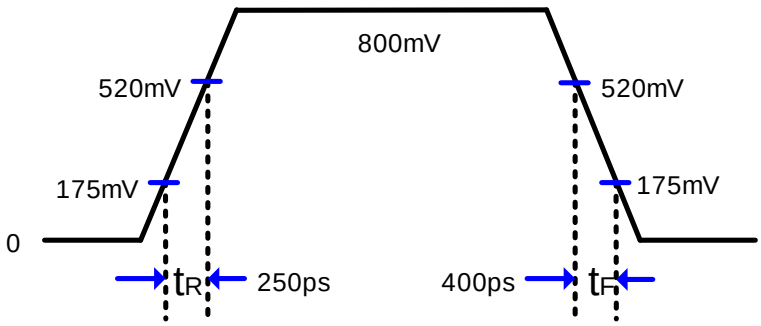
PCIE Device Routing (HCSL)



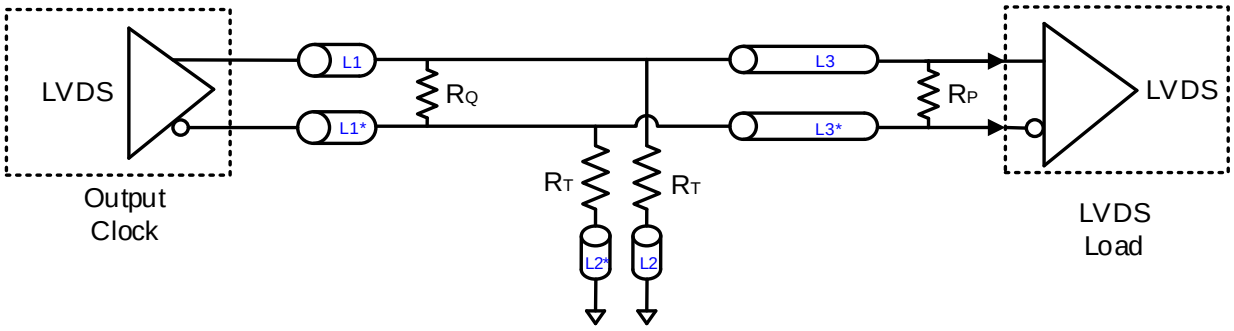
PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω
Differential Routing on a Single PCB	**Dimension or Value**	**Unit**
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	1.8 min to 14.4 max	inch
Differential Routing to a PCI Express connector	**Dimension or Value**	**Unit**
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	0.225 min to 12.6 max	inch

Typical HCSL Waveform



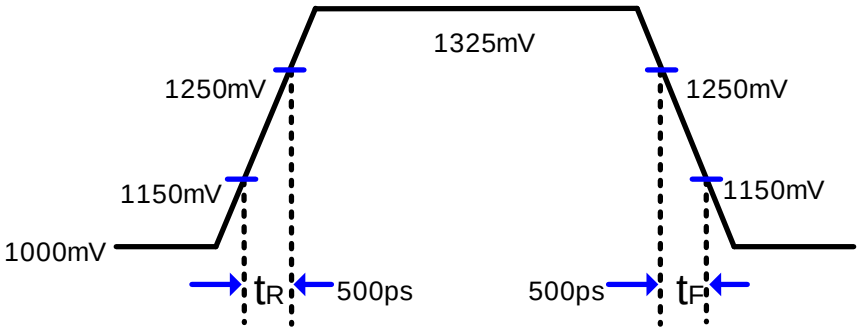
LVDS Device Routing



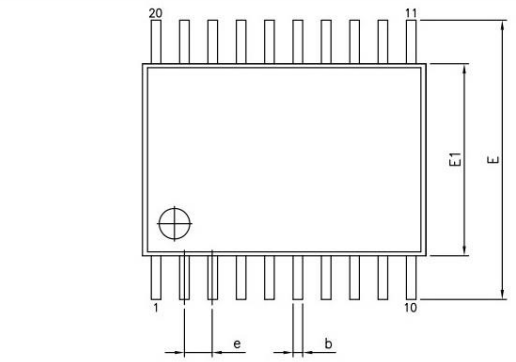
LVDS Device Routing Guidelines

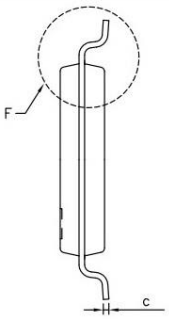
LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_P	100	Ω
R_Q	100	Ω
R_T	150	Ω
L3 length, route as 100Ω differential trace(strip-line)	14 max.	inch
L3 length, route as 100Ω differential trace.(Micro Strip-line)	12 max.	inch

Typical LVDS Waveform

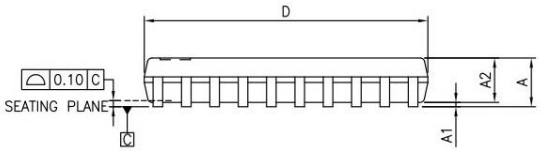


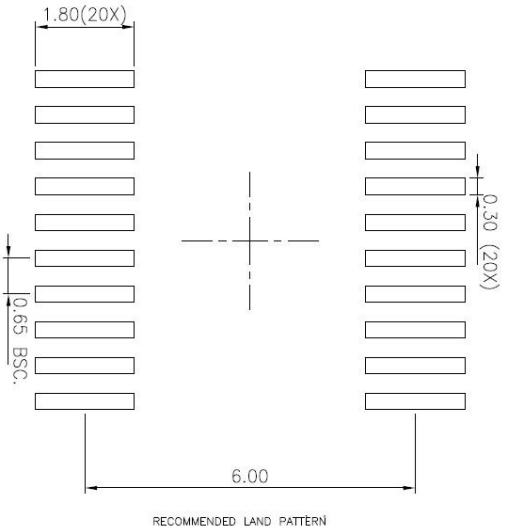
Packaging Information

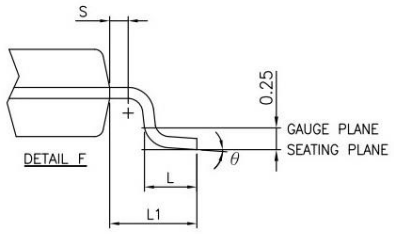




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°







Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

TSSOP20 POD

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	Official release	2023/2/17
V1.1	1. Update DC characteristics 2. Update some figures	2023/6/7
V1.2	Modify Tr/Tf Min value from 175ps to 150ps	2023/7/14