RS2CG5706N
PCIe3.0 Clock Generator with 2 HCSL outputs and 2 CMOS outputs

Features

- PCIe 3.0 compliant
- PCIe 3.0 Phase Jitter -0.45 ps RMS
- LVDS compatible outputs
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 35ps cycle-to-cycle (typ)
- Industrial temperature range
- frequency selection via external pins
- Packaging: (Pb-free and Green)
- 20-pin TSSOP (L20)

Applications

- PCI express
- Ethernet
- Wifi
- Universal timing

Block Diagram

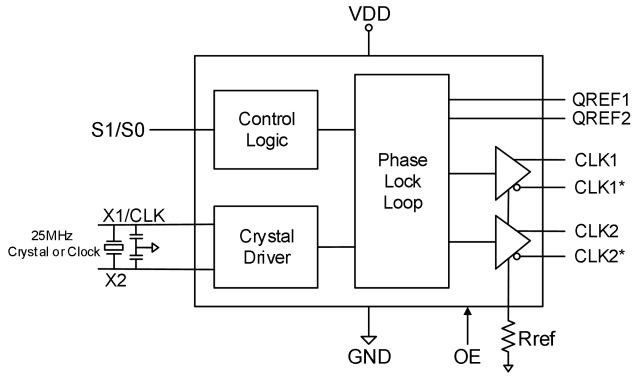


Figure 1: Block Diagram

Description

The RS2CG5706N is a spread spectrum clock generator compliant to PCI Express 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The RS2CG5706N provides two differential (HCSL) or LVDS spread spectrum outputs. The RS2CG5706N is configured clock selection. Using Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 25MHz, 100MHz, 125MHz and 200MHz clock frequencies and two channels CMOS outputs at 25MHz, 100MHz, 125MHz and 200MHz.

Ordering Information:

Ordering Code	Package	Package Description
RS2CG5706NLE	L	TSSOP20

Notes:
[1] E = Pb-free and Green

Pin Configuration (Top view)

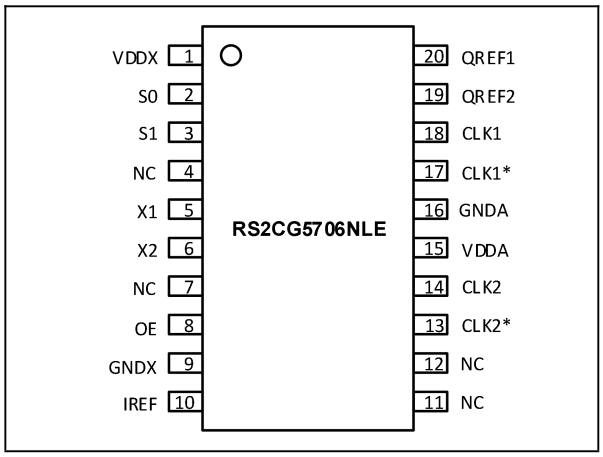


Figure 2. Pin configuration

Table 1. Output Selectable

S1	S0	CLK(MHz)	QREF(MHz)
0	0	25	25
0	1	100	100
1	0	125	125
1	1	200	200

Pin #	Pin Name	I/O Type	Description
1	VDDX	Power	Connect to a +3.3V source.
2	S0	Input	Select pin 0 (Internal pull-up resistor). See Table 1.
3	S1	Input	Select pin 1 (Internal pull-up resistor). See Table 1.
4	NC	NC	Not connect
5	X1	Input	Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
6	X2	Output	Crystal connection. Leave unconnected for clock input.
7	NC	NC	Not connect
8	OE	Input	Output enable. Internal pull-up resistor.
9	GNDX	Power	Crystal ground pin.
10	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
11	NC	NC	Not connect
12	NC	NC	Not connect
13	CLK2*	Output	HCSL compliment clock output
14	CLK2	Output	HCSL clock output
15	VDDA	Power	Connect to a +3.3V source.
16	GNDA	Power	Output and analog circuit ground.
17	CLK1*	Output	HCSL compliment clock output
18	CLK1	Output	HCSL clock output
19	QREF2	Output	Refer2 CMOS output
20	QREF1	Output	Refer1 CMOS output

Absolute Maximum Ratings (Note1)

Symbol	Parameter	Min	TYP	Max	Unit
T_{store}	Storage Temperature	−65	-	+150	°C
V_{DD}	DC Supply Voltage port B	-0.5	-	5.5	V
V_{IO}	Input / Output Voltage	-0.5	-	VDD+0.5	V
ESD	ESD HBM protection (input)	2000			V

Note1: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	Min	TYP	Max	Unit
V_{DD}	V_{CCA} Positive DC Supply Voltage	3.0	-	3.6	V
V_I	Enable Control Pin Voltage	-0.3	-	3.6	V
T_A	Operating Temperature Range	−40	-	+85	°C

DC Electrical Characteristics (Note2)

Unless otherwise specified, T_A = -40°C to +85°C, V_{DD}=3.3V ±10%.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IH}	Input High Voltage(1)	OE, S0, S1		2.0		V_{DD} +0.3	V
V_{IL}	Input Low Voltage(1)	OE, S0, S1		GND -0.3		0.8	V
I_{IL}	Input Leakage Current	0 ≤ Vin ≤ V_{DD}	Without input pull-up and pull-downs	-5		5	μA
I_{DD}	Operating Supply Current	R_L= 50Ω, C_L= 2pF				120	mA
I_{DDOE}		OE = LOW				80	mA
C_{IN}	Input Capacitance					7	pF
C_{OUT}	Output Capacitance					6	pF
L_{PIN}	Pin Inductance					5	nH
R_{OUT}	Output Resistance	CLK Outputs		3.0			kΩ

Note2:

1. RL= 50 ohm with CL =2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

HCSL AC Characteristics (Note3)

Unless otherwise specified, T_A = -40°C to +85°C, V_{DD} =3.3V ±10%.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency			25		MHz
f_{OUT}	Output Frequency		25		200	MHz
V_{OH}	Output High Voltage (1,2)	100 MHz HCSL output @ V_{DD} =3.3V	660	800	900	mV
V_{OL}	Output Low Voltage(1,2)		- 150	0	150	mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			35	60	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.75	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.18	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	1	ps
t_R	Rise Time(1,2)	From 0. 175V to 0.525V	175	332	700	ps
t_F	Fall Time(1,2)	From 0.525V to 0. 175V	175	344	700	ps
T_{SKEW}	Skew between outputs	At Crossing Point Voltage			50	ps
ODC	Output Duty Cycle(1,3)	HCSL output	45		55	%
T_{OE}	Output Enable Time(5)	All outputs			10	µs
T_{OT}	Output Disable Time(5)	All outputs			10	µs
tSTABLE	From power-up to V_{DD}=3.3V	From Power-up V_{DD}=3.3V		3.0		ms
tSPREAD	Setting period after spread change	Setting period after spread change		3.0		ms

Note3:
1. RL= 50 ohm with CL =2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

CMOS AC Characteristics

Unless otherwise specified, T_A = -40°C to +85°C, V_{DD} =3.3V ±10%.

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
f_{IN}	Input Frequency			25		MHz
f_{OUT}	Output Frequency		25		200	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	175		700	ps
ODC	Output Duty Cycle		40		60	%

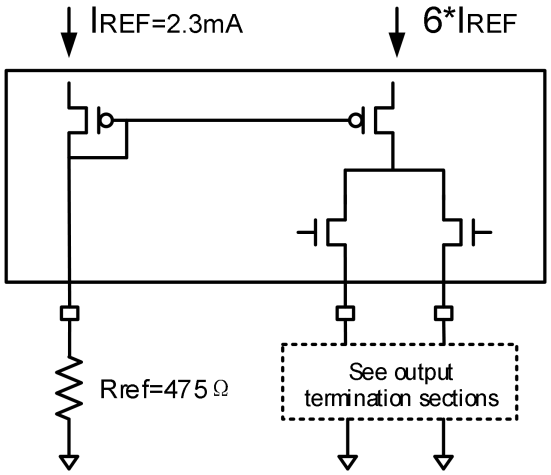
Application Information

Decoupling Capacitors
Decoupling capacitors of 0.01μF should be connected between each VDD pin and the ground plane and placed as close to the VDD pin as possible.

Crystal
Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors
C_L = Crystals' load capacitance in pF Crystal Capacitors (pF) = (C_L - 8) *2
For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16 -8)*2=16.

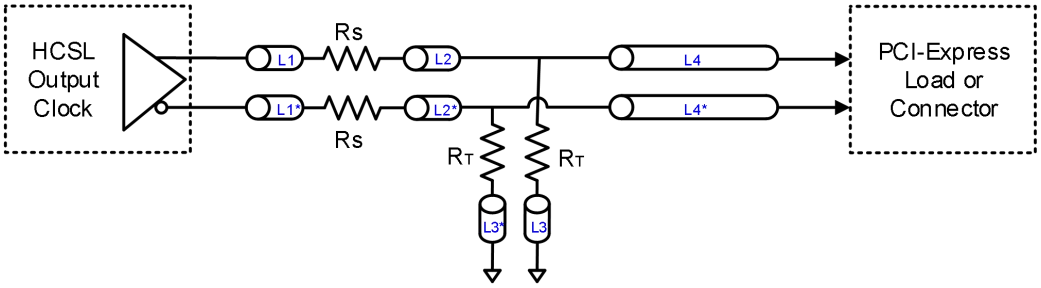
Current Source (IREF) Reference Resistor – R_{ref}
If board target trace impedance is 50Ω,
then R_{ref} = 475Ω providing an IREF of 2.32 mA. The output current (I_{OH}) is 6*IREF.



Output Termination
The PCI Express differential clock outputs of the RS2CG5706N are open-source drivers and require an external series resistor and a resistor to ground. These resistor values and their allow- able locations are shown in detail in the PCI Express Layout Guidelines section.

The RS2CG5706N can be configured for LVDS compatible volt- age levels. See the LVDS Compatible Layout Guidelines section.

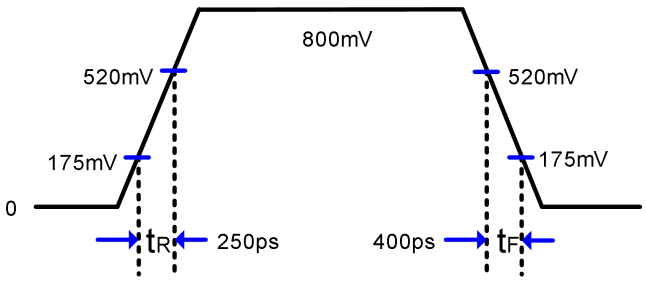
PCIE Device Routing (HCSL)



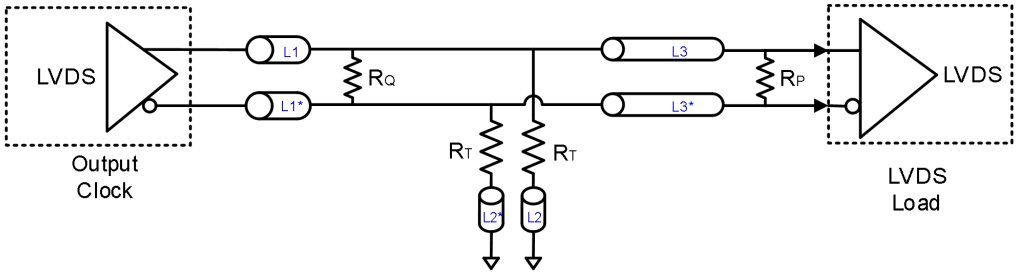
PCI Express Routing Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
RS	33	Ω
RT	49.9	Ω
Differential Routing on a Single PCB	**Dimension or Value**	**Unit**
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	1.8 min to 14.4 max	inch
Differential Routing to a PCI Express connector	**Dimension or Value**	**Unit**
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	0.225 min to 12.6 max	inch

Typical HCSL Waveform



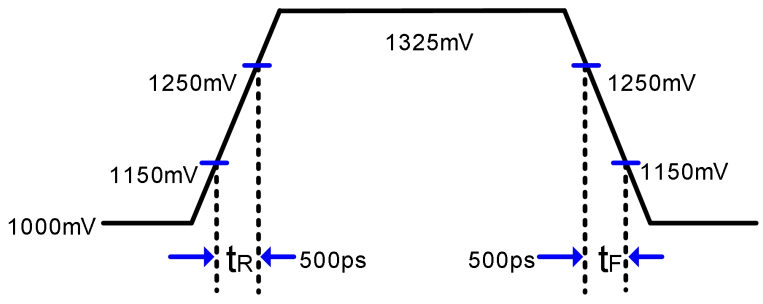
LVDS Device Routing



LVDS Device Routing Guidelines

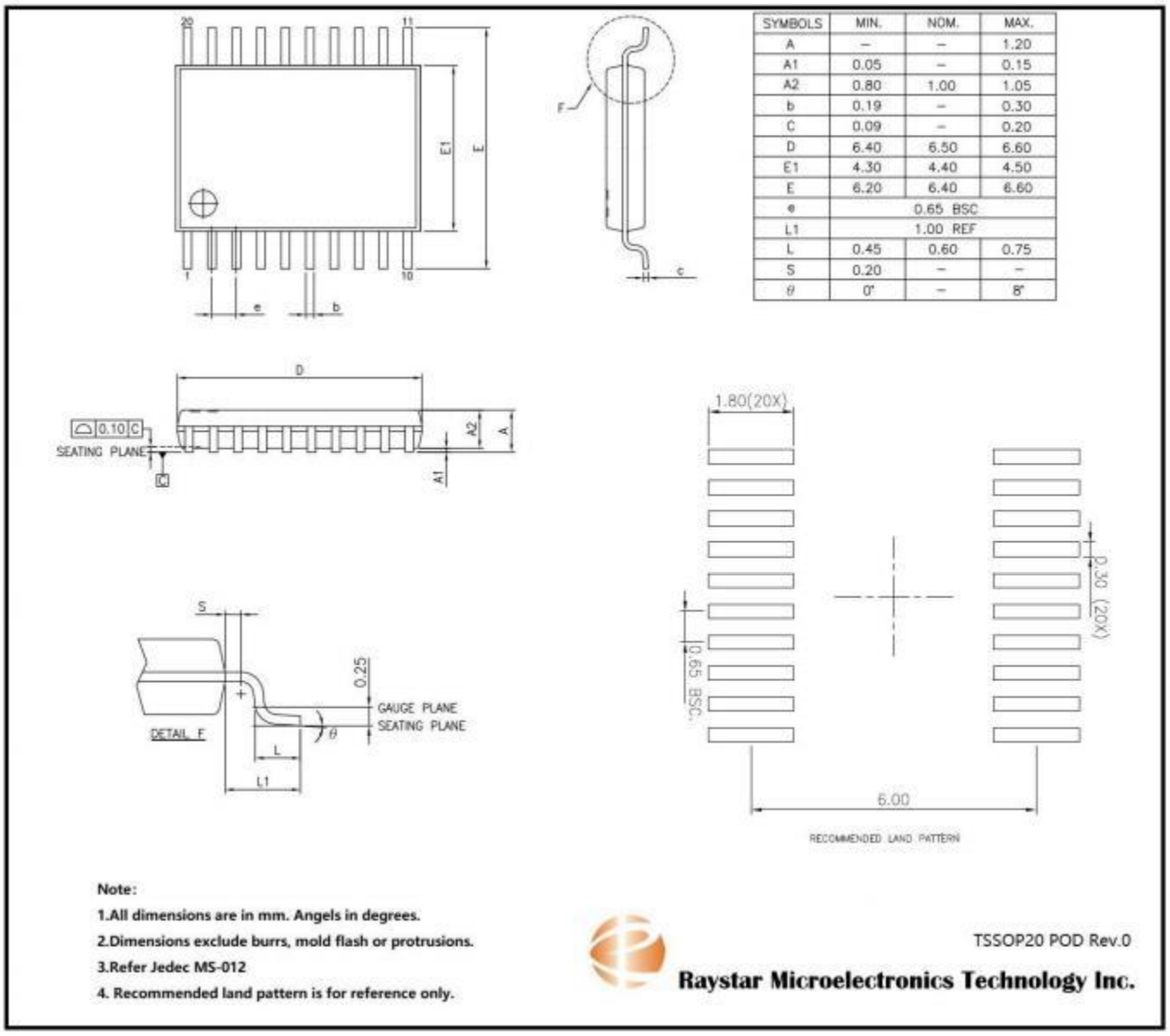
LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
RP	100	Ω
RQ	100	Ω
RT	150	Ω
L3 length, route as 100Ω differential trace(strip-line)	14 max	inch
L3 length, route as 100Ω differential trace.(Micro Strip-line)	12 max	inch

Typical LVDS Waveform



Packaging Mechanical:

TSSOP20 (L20)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

TSSOP20 POD Rev.0

Raystar Microelectronics Technology Inc.

History Log：

Rev #	DCN NO.	REVISION HISTORY	DATE
0.0	230023	Initiate	2023/2/15
1.0	230102	Modify several parameter specs	2023/5/10