Features

- PCIe 3.0 compliant
- PCIe 3.0 Phase Jitter -0.45 ps RMS
- LVDS compatible outputs
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 35ps cycle-to-cycle (typ)
- Spread of -0.5%, -0.75%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)
- 16-pin TQFN

Block Diagram

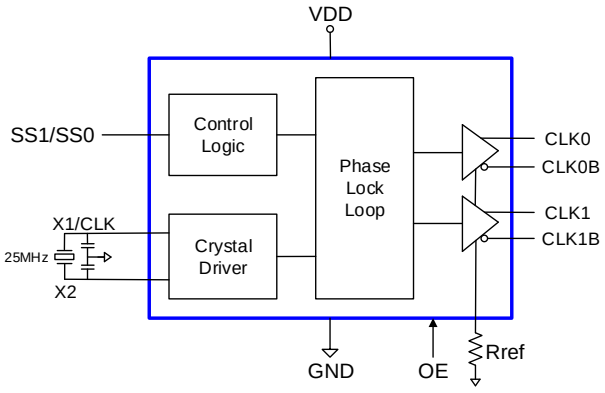


Figure 1: Block Diagram

Description

The RS2CG5702B is a spread spectrum clock generator compliant to PCI Express 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The RS2CG5702B provides two differential (HCSL) or LVDS spread spectrum outputs. The RS2CG5702B is configured to select spread and clock selection. Using Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 100MHz clock frequencies. It also provides spread selection of -0.5%, -0.75%, and no spread.

Ordering Information

Ordering Code	Package	Description
RS2CG5702BZHE	ZH	TQFN-16L 3X3X0.75

Notes:
[1] E = Pb-free and Green

Pin Configuration

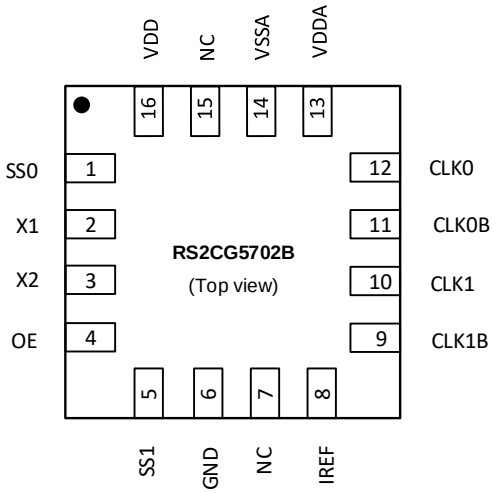


Table 1 Spread Selection

SS1	SS0	Spread
0	0	No Spread
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread

Pin No	Name	Type	Description
1	SS0	Input	Spread Select 0 (Internal pull-up resistor). See Table 1.
2	X1/CLK	Input	Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
3	X2	Output	Crystal connection. Leave unconnected for clock input.
4	OE	Input	Output enable. Internal pull-up resistor.
5	SS1	Input	Spread Select 1 (Internal pull-up resistor). See Table 1.
6	GND	Power	Crystal ground pin.
7	NC		No connect.
8	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
9	CLK1B	Output	HCSL complement clock output
10	CLK1	Output	HCSL clock output
11	CLK0B	Output	HCSL complement clock output
12	CLK0	Output	HCSL clock output
13	VDDA	Power	Connect to +3.3V source.
14	VSSA	Power	Output and analog circuit ground.
15	NC		No connect.
16	VDD	Power	Connect to +3.3V source.

Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	−65	-	+150	°C
V_{DD}	DC Supply Voltage port B	-0.5	-	5.5	V
V_{IO}	Input / Output Voltage	-0.5	-	VDD+0.5	V
ESD	ESD HBM protection (input)	2000			V

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	V_{CCA} Positive DC Supply Voltage	3.0	-	3.6	V
V_I	Enable Control Pin Voltage	-0.3	-	3.6	V
T_A	Operating Temperature Range	−40	-	+85	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 85°C, 3.0V≤V_{DD}≤3.6V

Symbol	Parameter	Conditions		MIN	TYP	MAX	Unit
VDD	Supply Voltage			3.0	3.3	3.6	V
VIH	Input High Voltage(1)	OE, SS0, SS1		0.7*VDD		VDD +0.3	V
VIL	Input Low Voltage(1)	OE, SS0, SS1		GND -0.3		0.3*VDD	V
IIL	Input Leakage Current	0 ≤ Vin ≤ VDD	Without input pull-up and pull-downs	-5		5	µA
IDD	Operating Supply Current	R_L = 50Ω, C_L = 2pF				120	mA
IDDOE		OE = LOW				60	mA
CIN	Input Capacitance					7	pF
COUT	Output Capacitance					6	pF
LPIN	Pin Inductance					5	nH
ROUT	Output Resistance	CLK Outputs		3.0			kΩ

Note:
1. R_L= 50 ohm with C_L =2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is Low

AC Characteristics

(V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
F_{IN}	Input Frequency			25		MHz
VOUT	Output Frequency			100		MHz
VOH	Output High Voltage (1,2)	100 MHz HCSL output @ V_{DD} =3.3V	660	800	900	mV
VOL	Output Low Voltage(1,2)		-150	0	150	mV
VCPA	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
VCN	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
JCC	Jitter, Cycle-to-Cycle(1,3)			35	60	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.75	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.18	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	1	ps
MF	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
tOR	Rise Time(1,2)	From 0.175V to 0.525V	150	332	700	ps
tOF	Fall Time(1,2)	From 0.525V to 0.175V	150	344	700	ps
TSKEW	Skew between outputs	At Crossing Point Voltage			50	ps
TDUTY-CYCLE	Duty Cycle(1,3)		45		55	%
TOE	Output Enable Time(5)	All outputs			10	µs
TOT	Output Disable Time(5)	All outputs			10	µs
tSTABLE	From power-up to V_{DD}=3.3V	From Power-up V_{DD}=3.3V		3.0		ms
tSPREAD	Setting period after spread change	Setting period after spread change		3.0		ms

Note:
1. R_L= 50 ohm with C_L =2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between each VDD pin and the ground plane and placed as close to the VDD pin as possible.

Crystal

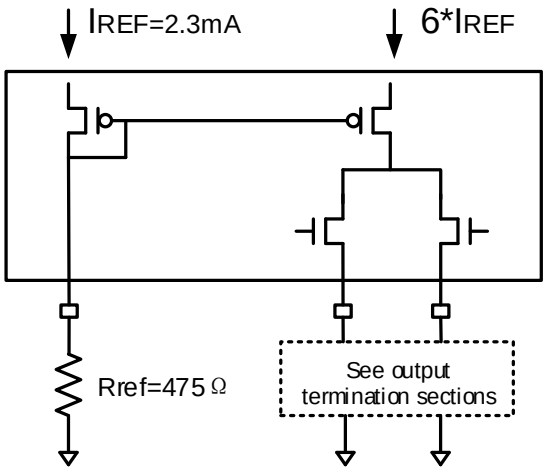
Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors

C_L = Crystals' load capacitance in pF Crystal Capacitors (pF) = (C_L - 8) *2
For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16-8)*2=16.

Current Source (IREF) Reference Resistor – Rref

If board target trace impedance is 50Ω,
then Rref = 475Ω providing an IREF of 2.32 mA. The output current (IOH) is 6*IREF.

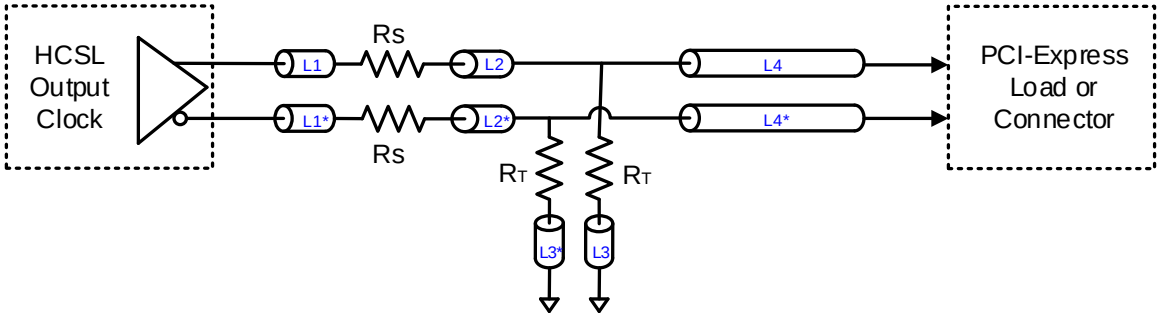


Output Termination

The PCI Express differential clock outputs of the RS2CG5702B are open-source drivers and require an external series resistor and a resistor to ground. These resistor values and their allow- able locations are shown in detail in the PCI Express Layout Guidelines section.

The RS2CG5702B can be configured for LVDS compatible volt- age levels. See the LVDS Compatible Layout Guidelines section.

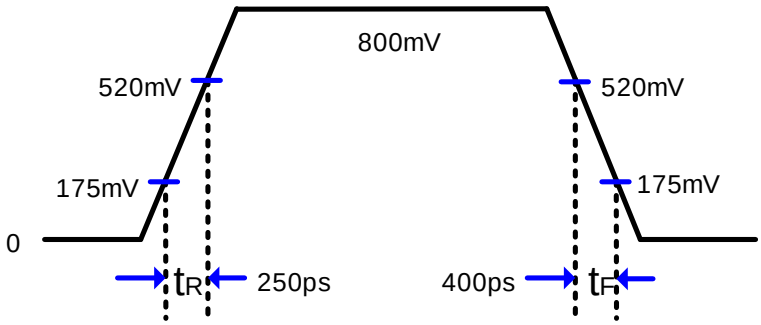
PCIE Device Routing (HCSL)



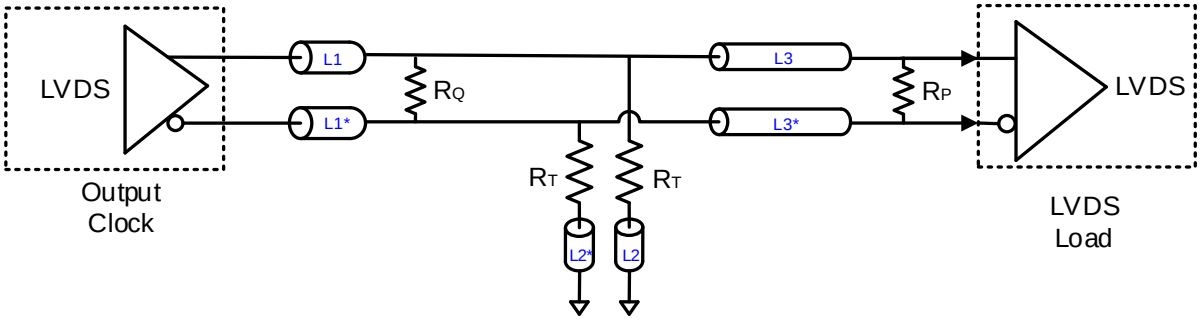
PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω
Differential Routing on a Single PCB	**Dimension or Value**	**Unit**
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	1.8 min to 14.4 max	inch
Differential Routing to a PCI Express connector	**Dimension or Value**	**Unit**
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled strip-line 100Ω differential trace.	0.225 min to 12.6 max	inch

Typical HCSL Waveform



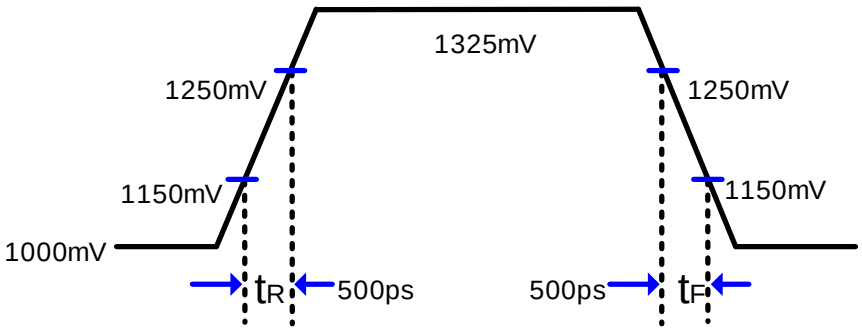
LVDS Device Routing



LVDS Device Routing Guidelines

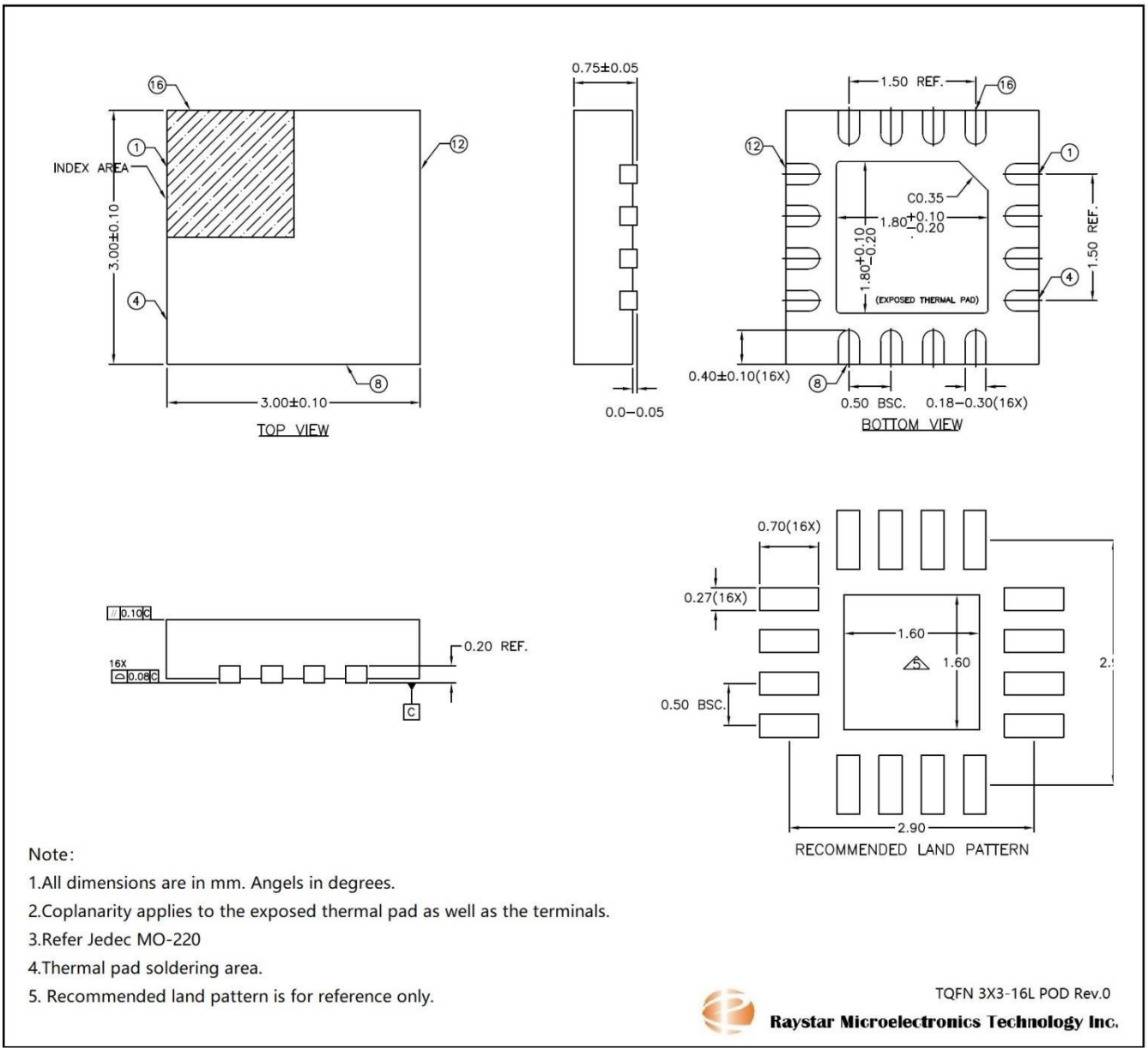
LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
RP	100	Ω
RQ	100	Ω
RT	150	Ω
L3 length, route as 100Ω differential trace(strip-line)	14 max	inch
L3 length, route as 100Ω differential trace.(Micro Strip-line)	12 max	inch

Typical LVDS Waveform



Package Information

TQFN16



Note:

1.All dimensions are in mm. Angels in degrees.

2.Coplanarity applies to the exposed thermal pad as well as the terminals.

3.Refer Jedec MO-220

4.Thermal pad soldering area.

5. Recommended land pattern is for reference only.

TQFN 3X3-16L POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.0	Initial release	2024/09/13