Features

- 3.3V Supply Voltage
- Crystal/CMOS Input: 25 MHz
- Four Differential Low-Power HCSL Outputs with On-Chip Termination
- Default ZOUT = 85Ω
- Two reference CMOS Outputs
- Programmable Slew Rate and Output Amplitude for Each Output
- Selectable 0%, -0.3%, or -0.5% Spread on Differential Outputs
- Differential Output-to-Output Skew <50ps
- Very-Low Jitter Outputs à Differential phase Jitter
  < 0.3ps RMS, SSC off
  < 1.5ps RMS, SSC on
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device
- Available in 32-TQPN package
- -40 to +125°C temperature operation
- AEC-Q 100 qualified, Automotive Grade 1 support; PPAP capable, and manufactured in IATF 16949 certified facilities

Applications

- Cloud/High-performance Computing
- nVME Storage
- In-Vehicle Networking
- Automotive infotainment

Description

The RS2CG506Q is a 4-output differential Low-Power HCSL Outputs and 6-CMOS outputs, very-low-power PCIe Gen1/ Gen2/Gen3/Gen4/Gen5 clock generator.

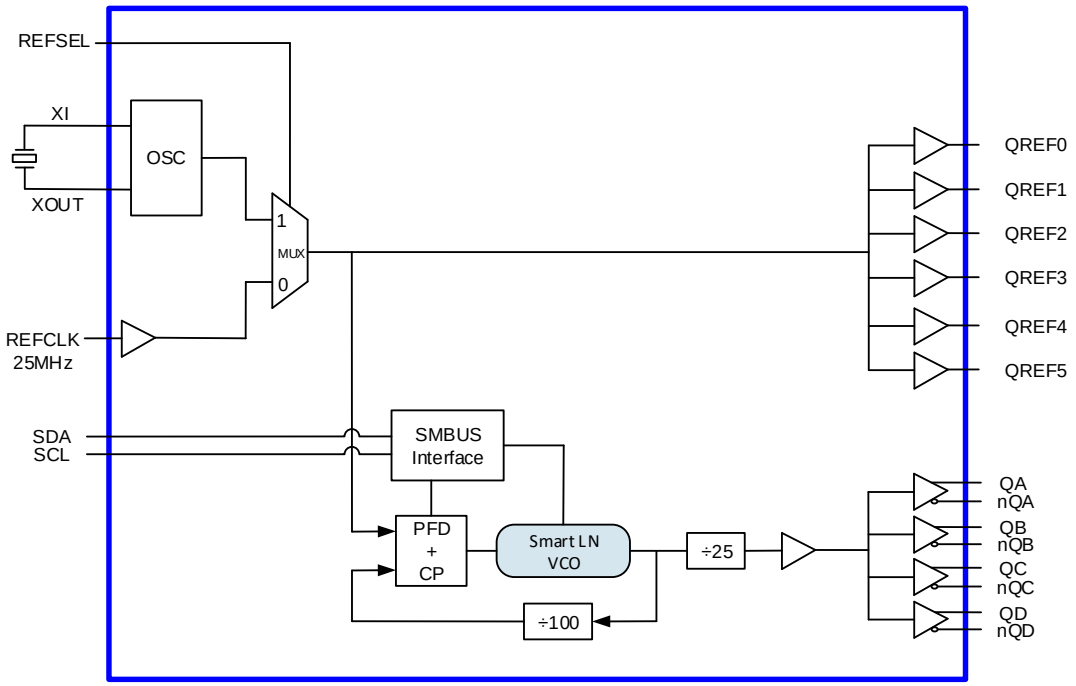
It uses a 25MHz crystal or CMOS reference clock as input to generate the 100MHz low-power differential LP-HCSL outputs with on-chip terminations. The 25MHz LVCMOS buffered reference outputs are provided to serve as a low-noise reference for other circuitry.

It uses RSM's proprietary PLL design to achieve very-low jitter that meets PCIe Gen1/Gen2/Gen3/ Gen4/Gen5 requirements. It also provides various options, such as different slew rate and amplitude through SMBUS. So users can easily configure the device to get the optimized performance for their individual boards. The device also supports selectable spread spectrum options to reduce EMI for various applications.

Order information

Part Number	Package	Description
RS2CG506QZDE	ZD	TQFN-40L_6mmx6mm

Functional Block Diagram



Pin Configuration

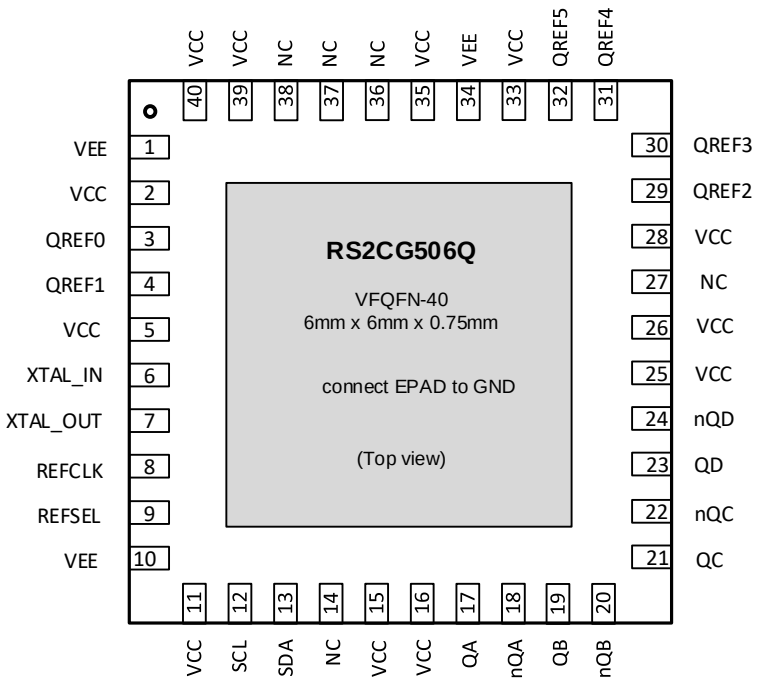


Table 1. Pin Descriptions

Pin Number	Name	Type		Description
1, 10, 34	V_{EE}	Power		Negative supply pins (GND).
2, 5, 11, 15, 16, 25,26, 28, 33,35, 39, 40	V_{CC}	Power		Pins 2, 28, 33 – power supply for the 25MHz LVCMOS outputs Pin 5 – power supply for the crystal oscillator Pins 11, 15, 26, 35 – power supply for the dividers and other core circuitry Pin 16, 25 – power supply for the LP-HCSL outputs Pin 39, 40 – power supply for the PLL
3, 4, 29, 30, 31, 32	QREF0, QREF1, QREF2, QREF3, QREF4, QREF5	Output		Single-ended outputs. 3.3V LVCMOS/LVTTL reference levels.
6, 7	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
8	REFCLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
9	REFSEL	Input	Pullup	Reference select pin. When HIGH, selects crystal. When LOW, selects REFCLK. LVCMOS/LVTTL interface levels.
12.13	SCL, SDA	I/O		SMBUS communication interface
14,27 36, 37,38	NC			No connect.
17, 18	QA, nQA	Output		Differential output pair. LP-HCSL interface levels.
19, 20	QB, nQB	Output		Differential output pair. LP-HCSL interface levels.
21, 22	QC, nQC	Output		Differential output pair. LP-HCSL interface levels.
23,24	QD, nQD	Output		Differential output pair. LP-HCSL interface levels.

Table 2. REFSEL Function

REFSEL	Input Source
0	REFCLK
1(default)	XTAL_IN, XTAL_OUT

Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, VDDxx .....–0.5V to +4.6V
Input Voltage .....–0.5V to VDD+0.5V, not exceed 4.6V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 4000V
Max Junction Temperature…….....+125ºC

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
T_A	Ambient air temperature	-40		125	℃
T_J	Junction temperature			125	℃

NOTE 1: It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.
NOTE 2: All conditions in the table must be met to guarantee device functionality.
NOTE 3: The device is verified to the maximum operating junction temperature through simulation.

DC Electrical Characteristics

Table 3. Power Supply DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No Load			200	mA

Table 4. LVCMOS DC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{IH}	Input High Voltage	REFSEL	2		V_{CC} +0.3	V
		REFCLK	V_{CC} - 0.4			V
V_{IL}	Input Low Voltage	REFSEL	-0.3		0.8	V
		REFCLK			0.4	V

Table 5. LVCMOS DC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C.

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
I_{IH}	Input High Current	REFCLK,	$V_{CC} = V_{IN} = 3.6V$			150	µA
		REFSEL	$V_{CC} = V_{IN} = 3.6V$			5	µA
I_{IL}	Input Low Current	REFCLK,	$V_{CC} = 3.6V, V_{IN} = 0V$	-5			µA
		REFSEL,	$V_{CC} = 3.6V, V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage;		$V_{CC} = 3.3V \pm 0.3V$	2.3			V
V_{OL}	Output Low Voltage;		$V_{CC} = 3.3V \pm 0.3V$			0.8	V

Table 6. LP-HCSL DC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{OH}	Output High Voltage;		660	750	850	mV
V_{OL}	Output Low Voltage;		-150	0	150	mV
V_{omax}	Output Maximum Voltage;			820	1150	mV
V_{omin}	Output Minimum Voltage;		-300	-42		mV
V_{oc}	Output Cross Voltage;		250	380	550	mV

Table 7. Crystal Characteristics

Parameter	Test Conditions	MIN	TYP	MAX	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

Table 8. Pin Characteristics

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
C_{IN}	Input Capacitance		Crystal Not Included		2		pF
C_{PD}	Power Dissipation Capacitance(per output)	QREF[0:5]	$V_{CC} = 3.6V$		6		pF
R_{PU}	Input Pullup Resistor				51		kΩ
R_{PD}	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QREF[0:5]			33		Ω

AC Electrical Characteristics

Table 9. LP-HCSL AC Characteristics, VCC = 3.3V ± 0.3V, VEE = 0V, TA = -40°C to 125°C.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
f_{IN}	Input Frequency			25		MHz
f_{OUT}	Output Frequency	LP-HCSL		100		MHz
T_{jc-c}	Cycle to cycle Jitter			20	60	ps
tsk(o)	Output Skew; NOTE 2, 3	Measured on the Rising Edge			50	ps
t_R / t_F	Slew rate	20% to 80%		3		V/ns
ODC	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

Table 10. AC Characteristics for Single Side Band Power Levels (LP-HCSL Outputs), VCC = 3.3V ± 0.3V, VEE = 0V, TA = 25°C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
tjPHASE	Integrated Phase Jitter (RMS)	PCIe Gen 1	-	30	86	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz	-	0.1	3.0	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)	-	1.3	3.1	ps
		PCIe Gen3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz,CDR = 10MHz)	-	0.42	1	ps
		PCIe Gen3 Separate Reference No Spread (PLL BW of 2-4 or 2-5MHz, CDR=10 MHz)	-	0.21	0.7	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)	-	0.4	0.5	ps
		PCIe Gen 5(7) (PLL BW of 500k to 1.8MHz. CDR = 20MHz)	-	0.05	0.15	ps
tjPH-SRISG2	Integrated Phase Jitter (RMS), -0.3%Spread	PCIe Gen 2, Separate Reference Independent Spread(PLL BW of 16MHz, CDR=5MHz)	-	0.92	2	ps
tjPH-SRISG3	Integrated Phase Jitter (RMS), -0.3% Spread	PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz,CDR=10MHz)	-	0.4	0.7	ps
tjPH-SRISG2	Integrated Phase Jitter (RMS), -0.5% Spread	PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz)	-	1.1	2	ps
tjPH-SRISG3	Integrated Phase Jitter (RMS), -0.5% Spread	PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz,CDR=10MHz)	-	0.6	0.7	ps

Table 11. LVCMOS AC Characteristics, VCC = 3.3V ± 0.3V, TA = -40°C to 125°C

Symbol	Parameter		Test Conditions	MIN	TYP	MAX	Units
f_{IN}	Input Frequency				25		MHz
f_{OUT}	Output Frequency				25		MHz
t_{jit}	RMS Phase Jitter (Random)		25MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 5MHz		0.140		ps
*t*sk(o)	Output Skew;	QREF[0:5]	Measured on the Rising Edge			50	ps
PSNR	Power Supply Noise Reduction	Pin 40, (VCC)	From DC to 6.25MHz		-80		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%		1.0	1.5	ns
odc	Output Duty Cycle			45		55	%

Table 12. AC Characteristics for Single Side Band Power Levels (LVCMOS Outputs), VCC = 3.3V ± 0.3V, VEE = 0V, TA = 25°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	25MHz		-137		dBc/Hz
φ_N(10k)	Single-side band phase noise, 10kHz from Carrier			-153		dBc/Hz
φ(100k)	Single-side band phase noise, 100kHz from Carrier			-162		dBc/Hz
φ_N(1M)	Single-side band phase noise, 1MHz from Carrier			-163		dBc/Hz
φ_N(5M)	Single-side band phase noise, 5MHz from Carrier			-163		dBc/Hz

SMBus Serial Data Interface

RS2CG506 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below. Read and write block transfers can be stopped after any complete byte transfer

Table 13. Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	0	0/1

Table 14. How to Write

1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit		8 bit	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	……	Data Byte (N+X-1)	Ack	Stop bit

Table 15. How to Read

1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	8 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bit	1 bit	1 bit
……..	Data Byte (N+X-1)	NAck	Stop bit

Table 16. Output Enable Control 0

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			1
Bit 6	Reserved		RW			1
Bit 5	Reserved		RW			1
Bit 4	Reserved		RW			1
Bit 3	OE_OUTA		RW	Disable Output	Enable Output	1
Bit 2	OE_OUTB		RW	Disable Output	Enable Output	1
Bit 1	OE_OUTC		RW	Disable Output	Enable Output	1
Bit 0	OE_OUTD		RW	Disable Output	Enable Output	1

Table 17. Output status Control 1

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SLEW RATE OF HCSL	HCSL SLEW RATE CONTROL	RW	Slow setting	Fast setting	0
Bit 6	STOP1	HCSL Stop Mode Control	RW	00= Low / Low 01= HIZ / HIZ 10= High / Low 11= Low / High		0
Bit 5	STOP0					0
Bit 4	HCSL PD	HCSL PD MODE	RW	Normal	PD	0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	REF HIZ	Output REF CMOS HIZ MODE	RW	Normal	HIZ	0

Table 18. Reserved

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 19. Reserved

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 20. Reserved

Byte 4	Name		Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 21. Reserved

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 22. Reserved

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 23. Reserved

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 24. Vendor/Revision Identification Control

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	Rev A = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	Vendor ID	R	RSM = 0011		0
Bit 2	VID2		R			0
Bit 1	VID1		R			1
Bit 0	VID0		R			1

Table 25. Device ID Control

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	DID7		R			0
Bit 6	DID6		R			0
Bit 5	DID5	Device ID	R			0
Bit 4	DID4		R			0
Bit 3	DID3		R			0
Bit 2	DID2		R			1
Bit 1	DID1		R			1
Bit 0	DID0		R			1

Table 26. Byte Count Control

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	BC5	Writing to this register configures how many bytes will be read back	RW	Default value is 8		0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Table 27. Reserved

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 28. Reserved

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 29. Reserved

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 30. Reserved

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 31. Reserved

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 32. Reserved

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 33. Reserved

Byte 17	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 34. Reserved

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	Reserved	Write not allowed	RW			0
Bit 6	Reserved	Write not allowed	RW			1
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 35. Reserved

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	Reserved		RW			0
Bit 5	Reserved		RW			0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

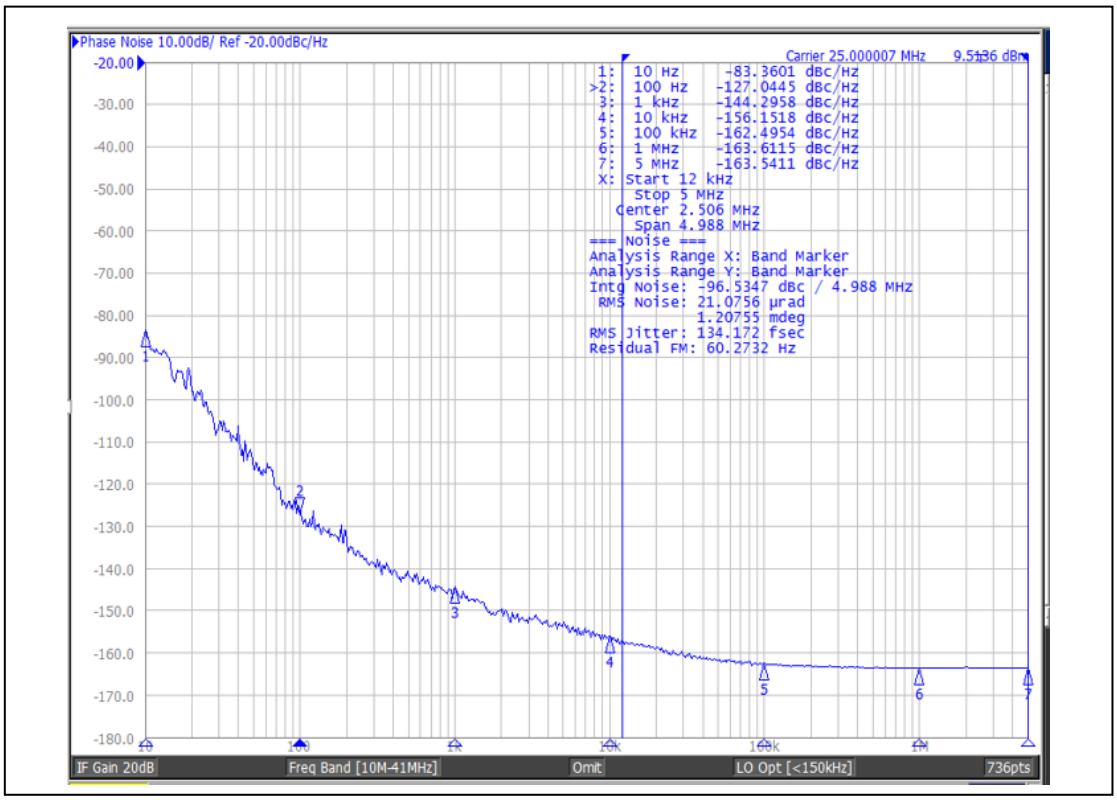
Table 36. SSC Control

Byte 20	Name	Control Function	Type	0	1	Default
Bit 7	Reserved		RW			0
Bit 6	SSC_DIV6	SSC clk divider ratio = N*2+1 Fssc = Fpfd_FB / (N*2+1) /12 B20[1] is RO/RW when B20[7]=0/1	RW	Divide ratio = decimal value x 2 + 1		1
Bit 5	SSC_DIV5		RW			0
Bit 4	SSC_DIV4		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved		RW			0
Bit 0	Reserved		RW			0

Table 37. SSC and EFUSE Control

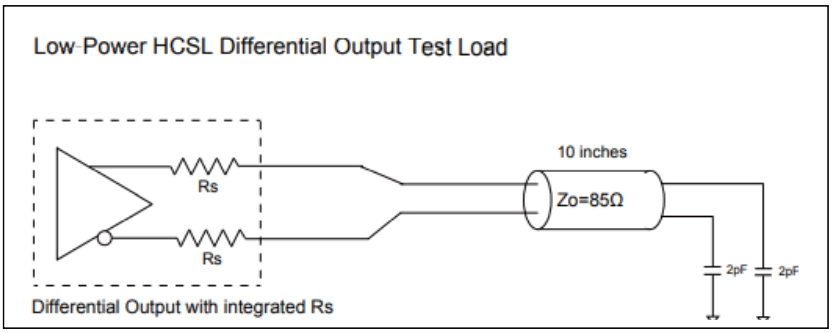
Byte 21	Name	Control Function	Type	0	1	Default
Bit 7	SSC_PD	SSC block power down valid if CG is SSC mode	RW	Normal	Power down	0
Bit 6	SSC_EN_SW1	SSC_EN SW contol	RW	00 = SSC off 01 = -0.3% SS 10 = -0.3% SS 11 = -0.5% SS		0
Bit 5	SSC_EN_SW0					0
Bit 4	Reserved		RW			0
Bit 3	Reserved		RW			0
Bit 2	Reserved		RW			0
Bit 1	Reserved	Write not allowed	RW	00 = ACCESS0 / ACCESS0 01 = RE / PEB 10 = OUTPUT1 / ACCESS1 11 = OUTPUT0 / ADDR0		0
Bit 0	Reserved		RW			0

Plots 25MHz LVCMOS Clock (12k to 5MHz)

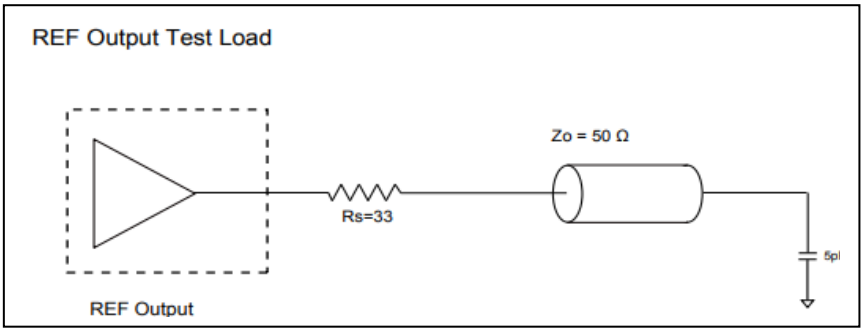


Typical Test Circuit

Low-Power HCSL Test Circuit



CMOS REF Test Circuit



Differential Output Driving LVDS

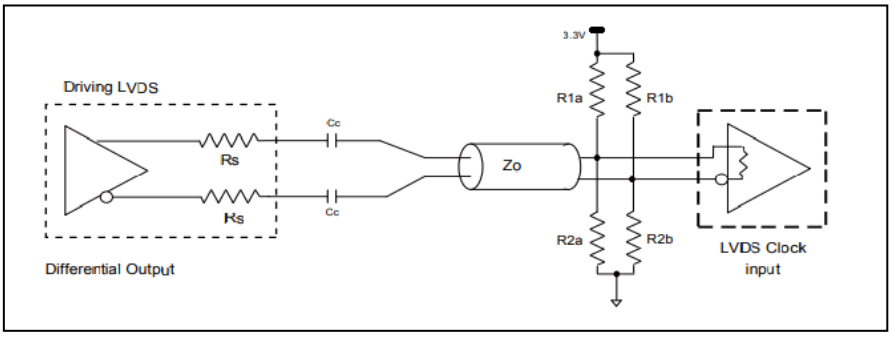


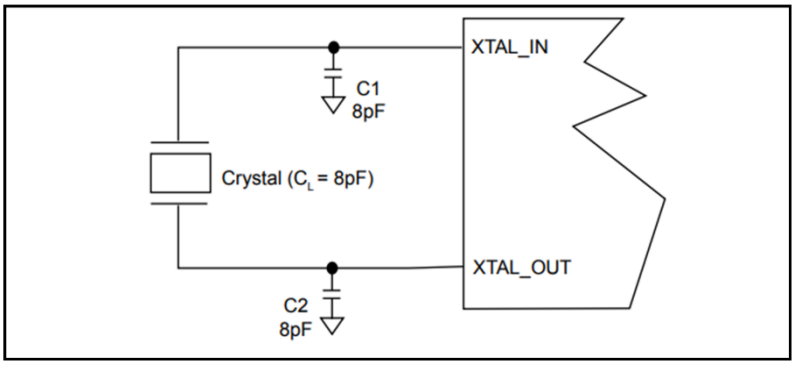
Table 38. Alternate Differential Output Terminations (Zo = 85Ω)

Component	Receiver with Termination	Receiver without Termination	Unit
R1a, R1b	10,000	130	Ω
R2a, R2b	5600	64	Ω
C_C	0.1	0.1	uF
V_{CM}	1.2	1.2	V

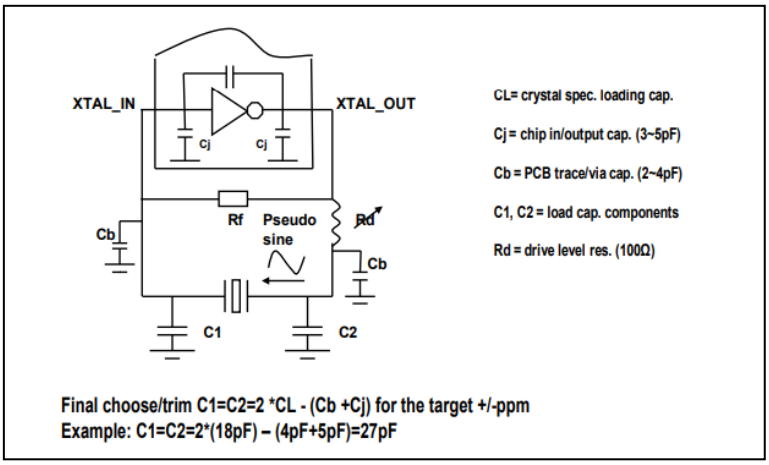
Crystal Circuit Connection

The following diagram shows RS2CG506 crystal circuit connection with a parallel crystal. For the CL=8pF crystal, it is suggested to use C1=8pF and C2=8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit

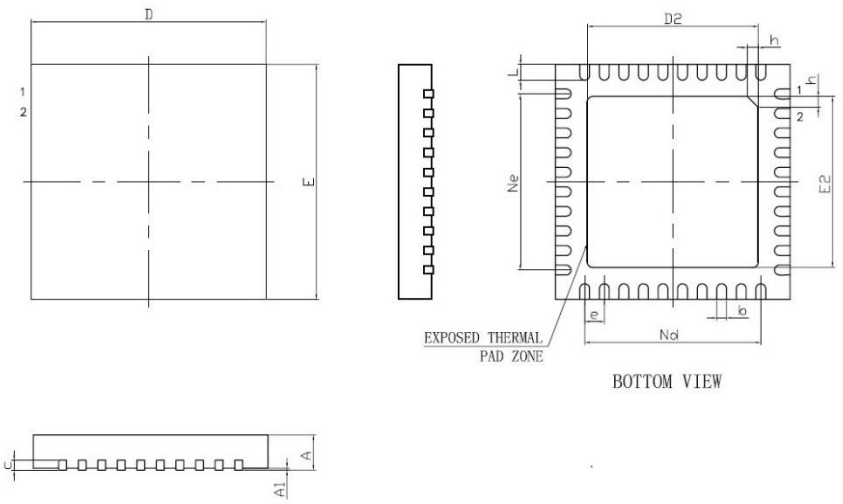


Crystal Capacitor Calculation



Package Information

40-TQFN (ZD40)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	5. 90	6. 00	6. 10
D2	4. 10	4. 20	4. 30
e	0. 50BSC		
Ne	4. 50BSC		
Nd	4. 50BSC		
E	5. 90	6. 00	6. 10
E2	4. 10	4. 20	4. 30
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40
L/F载体尺寸 (MIL)	177*177		

Note:
1.All dimensions are in mm. Angels in degrees.
2.Coplanarity applies to the exposed thermal pad as well as the terminals.
3.Refer Jedec MO-220
4.Thermal pad soldering area.

TQFN6X6X0.75-0.5-40L (ZD40) POD Rev.0

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
1.0	1. Official release.	2023/9/13
1.1	1. Modify the VCC pin description error. 2. Modify the document number from 51 to 54.	2023/12/12
1.2	1.Update Pin Configuration. 2.Update the Plots. 3.Update LVCMOS AC Characteristics. 4.Update the LP_HCSL Test Circuit and Oscillator Circuit. 5.Update the Parameter of Table 4.	2024/7/19