Features

- Operating Frequency: 0MHz~200 MHz
- Low additive jitter: <50fs rms
- low skew: < 50ps
- Fast rise/fall time: 1.0ns typ.
- Propagation delay: 2.5ns typ.
- Industrial temperature (–40°C to 85°C)
- 3.3V/2.5V/1.8V power supply
- Packaging (Pb-free & Green available)

Applications

- 33 MHz PCI-to- 133 MHz PCIX controllers
- 80 MHz for 10/100 Mbps Ethernet
- 125 MHz for Gigabit networking
- 155.520 MHz for Optical OC3/SDH/SONET

Block Diagram

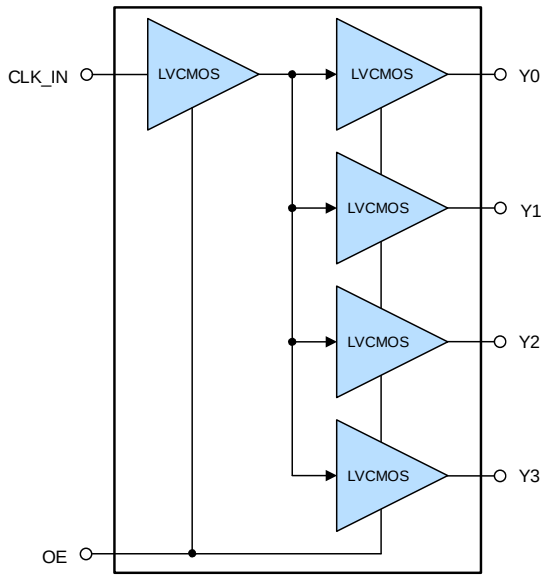


Figure 1 Block Diagram

Description

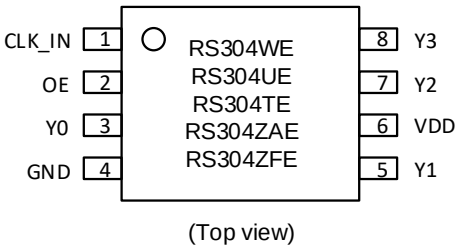
Raystar's RS304 are low-skew, low-noise, high speed clock buffers and are ideal for computing, networking, and communication applications. Application examples include PCI(X) clock buffers in servers and workstations, PCI(X) Storage Area Network (SAN), and RAID controllers. They are used for networking and communications applications requiring 80 MHz for 10/100 Mbps Ethernet and 125 MHz for Gigabit networking clocks. To reduce EMI emission and power consumption, all outputs can be disabled to Low-state by asserting a low signal to the OE (Output Enable) pin. RS304 output impedance is 50 ohms.

Order Information

Part Number	Package	Description
RS304WE	8-Pin SOIC	4.9mmx6mm
RS304UE	8-Pin MSOP	3.2mmx5.15mm
RS304TE	8-Pin TSSOP	3mmx6.4mm
RS304ZAE	8-Pin DFN8	2mmx2mm
RS304ZFE	8-Pin DFN8	1.5mmx1.5mm

Notes
[1] E = Pb-free and Green

Pin Configuration



(Top view)

Table 1 Function table

INPUT		OUTPUT
CLK_IN	OE	Y[0:3]
X	L	L
L	H	L
H	H	H

Pin Description

Pin name	Pin No.	Type	Description
CLK_IN	1	Input	Clock input
OE	2	Input	Active High Output Enable. Y[0:3] outputs will be Low Level when OE is low
Y[0:3]	3,5,7,8	Output	LVCMOS level outputs
GND	4	Ground	Ground
VDD	6	Power	3.3V/2.5V/1.8V Power Supply

Absolute Maximum Ratings

Parameter	Range
Supply Voltage (VDD)	–0.0V to +6.5V
Input Voltage	–0.5V to VDD+0.5V
Industrial Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Input ESD MIL- 883, method 3015, HBM	2KV

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
VDD	I/O Supply, Analog Core Supply	1.71	3.63	V
TA	Industrial Ambient Temperature	–40	+85	° C

DC Electrical Characteristics

(TA = –40~85°C,VCC = 3.3V ±10%,2.5V ±10%,1.8V ±5%)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage	VDD=2.5V/3.3V	0.6*VDD			
I_{IL}	Input Low Current	VIN = 0V			–5	μA
I_{IH}	Input High Current	VIN = VDD			5	
V_{OL}	Output Low Voltage	VDD=2.5V/3.3V, I_{OL} = 12mA			0.25*VDD	V
V_{OH}	Output High Voltage	VDD=2.5V/3.3V, I_{OH} = -12mA	0.7*VDD			
C_O	Output Capacitance			3	7	pF
C_I	Input Capacitance			3	5	
I_{DD}	Supply Current	CL = 15pF/100MHz VDD=3.3V		32		mA
		CL = 15pF/100MHz VDD=2.5V		26		
		CL = 15pF/100MHz VDD=1.8V		20		
Z_O	Nominal Output Impedance	VDD=1.8V		50		Ω
		VDD=2.5V		30		Ω
		VDD=3.3V		25		Ω
L	Pin Inductance				7	nH

AC Characteristics

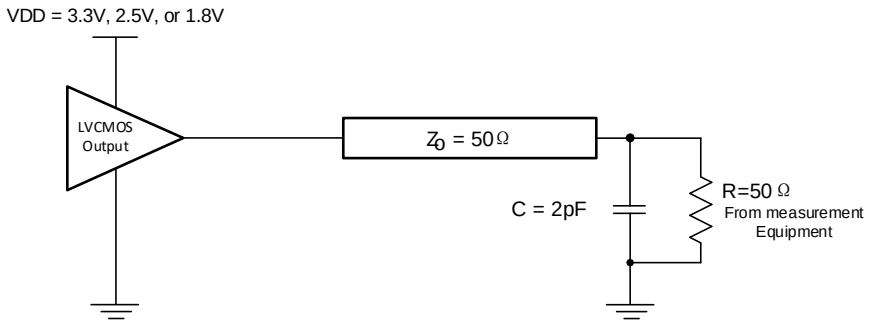
(TA = –40~85°C,VCC = 3.3V ±10%,2.5V ±10%,1.8V ±5%, 15pF/100MHz)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
F_{IN}	Input frequency		0		200	MHz
T_{PLH}	Low-to-high propagation delay	CLK_IN to Y[0-3] rising edges @ 1.5V	1.0	1.7	3.0	ns
		CLK_IN to Y[0-3] rising edges @ 1.25V	1.0	2.0	3.2	
		CLK_IN to Y[0-3] rising edges @ 0.9V	1.0	2.5	3.5	
T_{PHL}	High-to-low propagation delay	CLK_IN to Y[0-3] falling edges @ 1.5V	1.0	1.7	3.0	
		CLK_IN to Y[0-3] falling edges @ 1.25V	1.0	2.0	3.2	
		CLK_IN to Y[0-3] falling edges @ 0.9V	1.0	2.5	3.5	
$T_{SK(O)}$	Output skew	@ VDD/2			100	ps
$T_{SK(P)}$	Pulse skew	@ VDD/2			300	
$T_{SK(T)}$	Package skew(1)	@ VDD/2			500	
T_R,T_F	Rise, Fall time	20%~80% VDD=3.3V		0.7	1.4	ns
		20%~80% VDD=2.5V		1	2	
		20%~80% VDD=1.8V		1.5	3	
T_{EN}	Output Enable Time				5	
T_{DIS}	Output Disable Time				10	
T_{DC}	Output Duty Cycle	tDC = tH/tC Y, tH = High Pulse Width	45		55	%

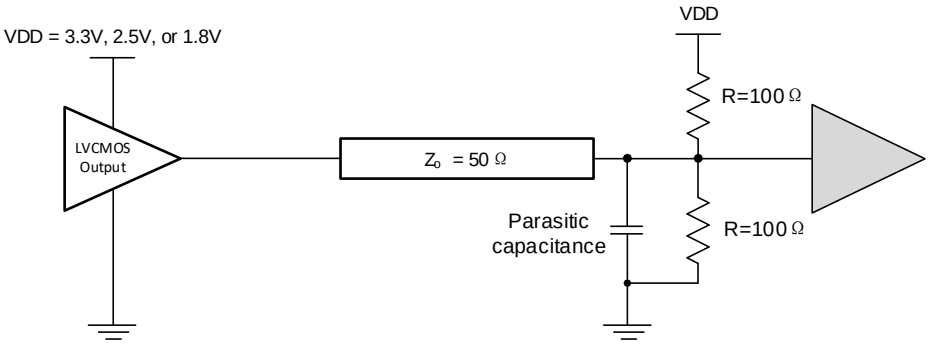
Note:

1. Identical traces, loads, power supply.
2. Maximum Output Skew is 100ps when frequency is below 125MHz with 10pF loading.

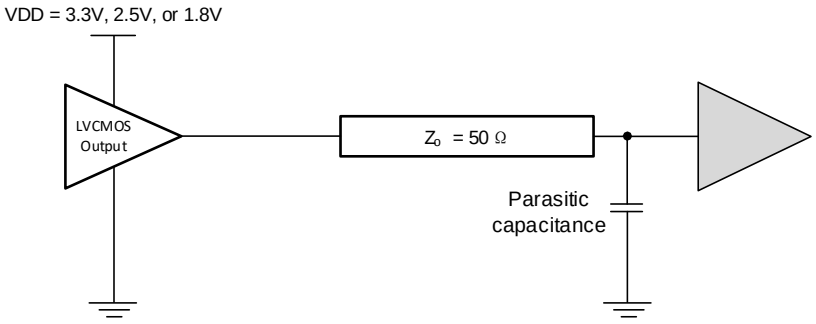
Parameter Measurement Information



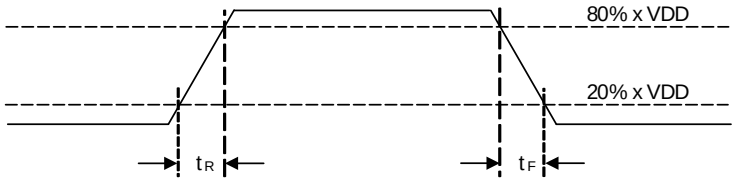
Test Load Circuit



Application Load With 50-Ω Termination



Application Load With Termination

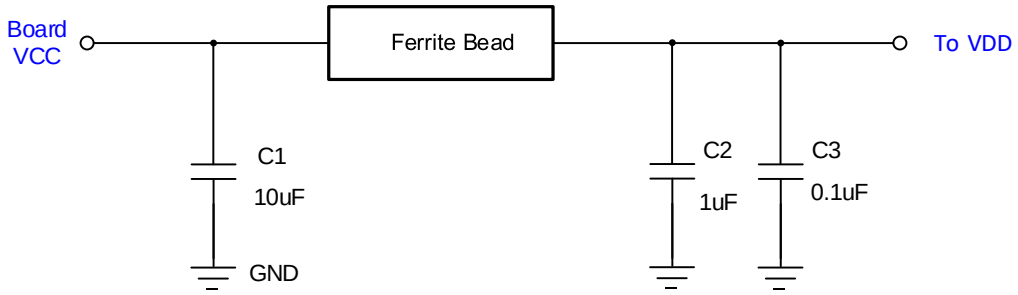


Rise and Fall Time

Power Supply Recommendations

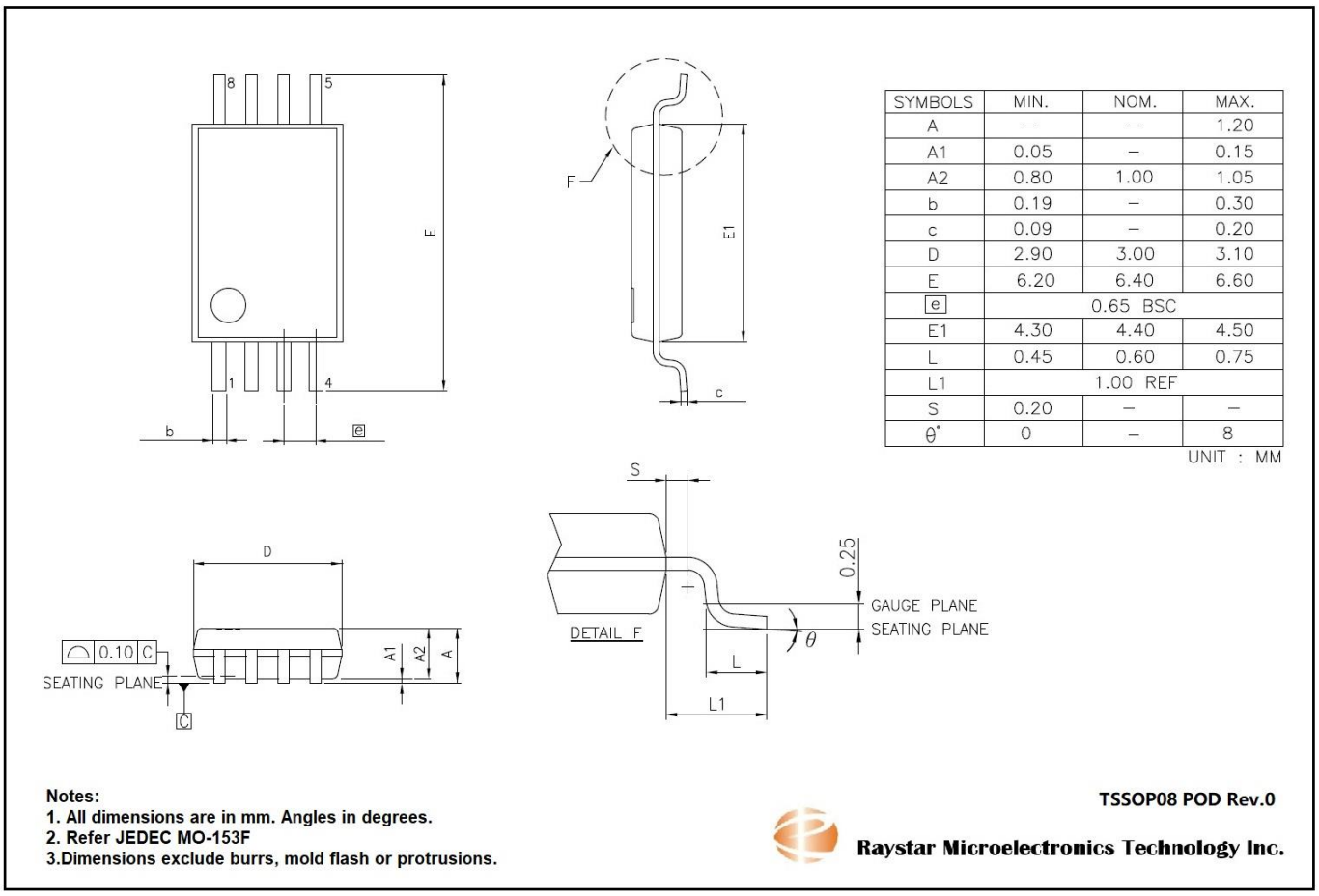
High-performance clock buffers can be sensitive to noise on the power supply, which may dramatically increase the additive jitter of the buffer. Thus, it is essential to manage any excessive noise from the system power supply, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. It's recommends adding as many high- frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. We recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.



Package Information

8-Pin TSSOP (T)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E	6.20	6.40	6.60
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

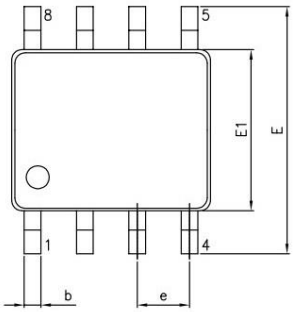
UNIT : MM

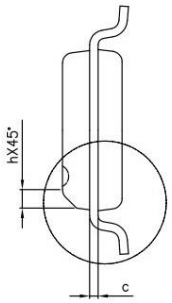
Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-153F
3.Dimensions exclude burrs, mold flash or protrusions.

TSSOP08 POD Rev.0

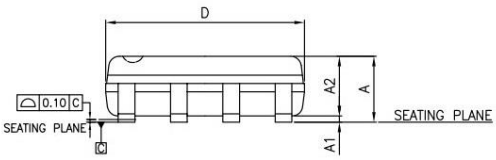
Raystar Microelectronics Technology Inc.

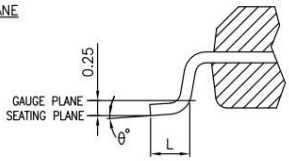
8-Pin SOIC (W)

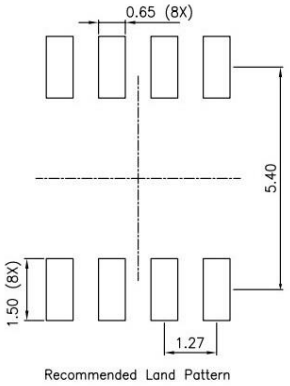




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8







Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

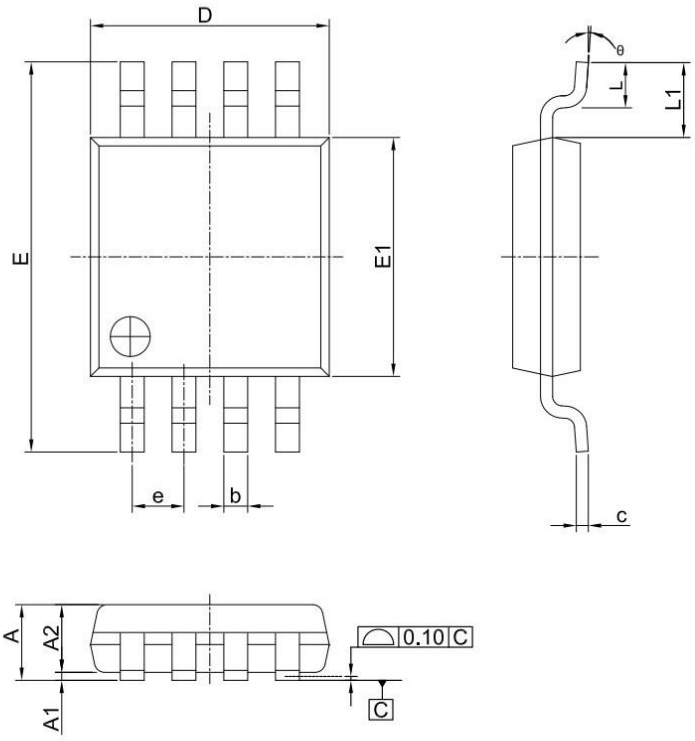
3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

Raystar Microelectronics Technology Inc.

8-Pin MSOP (U)



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Note:

1.All dimensions are in mm. Angels in degrees.

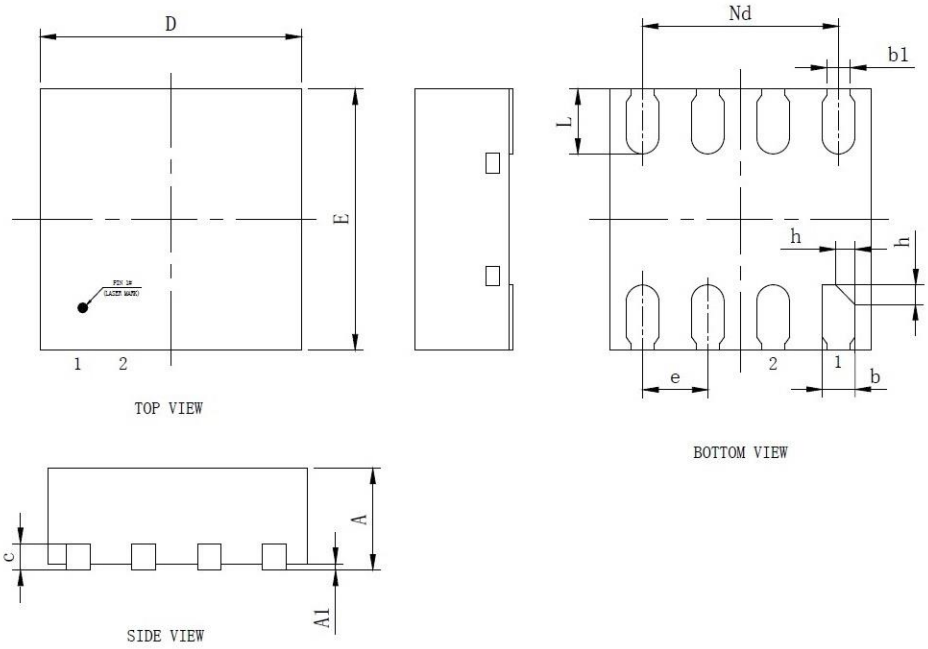
2.Refer Jedec MO-187

3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08 POD Rev.0

Raystar Microelectronics Technology Inc.

8-Pin DFN8 (ZA)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 18	0.25	0. 30
b1	0.18REF		
c	0.203REF		
D	1. 90	2. 00	2. 10
e	0. 50BSC		
Nd	1. 50BSC		
E	1. 90	2. 00	2. 10
L	0. 45	0.50	0. 55
h	0. 10	0. 15	0. 20

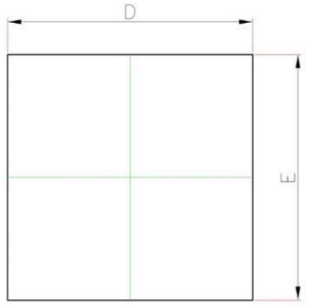
Notes:

1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-229
3.Dimensions exclude burrs, mold flash or protrusions.

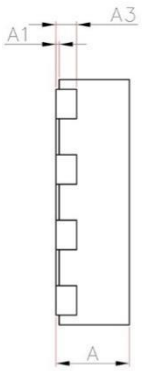
DFN 2X2X0.75-8L(ZA08) POD Rev.0

Raystar Microelectronics Technology Inc.

8-Pin DFN8 (ZF)

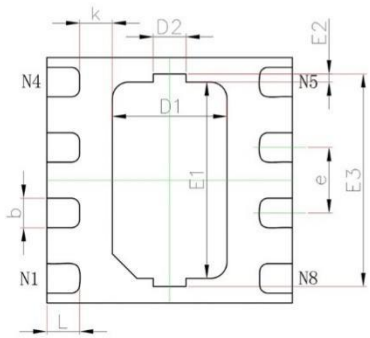


TOP VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.400	0.500	0.016	0.020
A1	0.000	0.050	0.000	0.002
A3	0.127REF.		0.005REF.	
D	1.450	1.550	0.057	0.061
E	1.450	1.550	0.057	0.061
D1	0.600	0.800	0.024	0.031
D2	0.200REF.		0.008REF.	
E1	1.100	1.300	0.043	0.051
E2	0.050REF.		0.002REF.	
E3	1.200	1.400	0.047	0.055
k	0.200REF.		0.008REF.	
b	0.150	0.250	0.006	0.010
e	0.400BSC.		0.016BSC.	
L	0.150	0.250	0.006	0.010



BOTTOM VIEW

Note:
1. All dimensions are in mm. angle in degrees.
2. Refer JEDEC MO-229.
3. demensions exclude burrs, mold flash or protrusions.

DFN 1.5X1.5X0.45 8L(ZF08) POD Rev.A
Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
V1.4	1. Add ordering code RS304ZAE of DFN8 package 2. Applcate formatted document 3. Change TSSOP8,SOP8,MSOP8 package figure	2023/6/16
V1.5	1. Modify VIH（MAX）=0.8V. Delete the typical value. 2. Modify IIL test condition.	2024/4/11
V1.6	1. Add 1.8V and 2.5V Data 2. Modify Test Load information and Order table. 3. ADD Power Supply Recommendations	2025/1/14
V1.7	1. Modify the output Impedance Zo=50Ω. 2. Add DFN8-1.5mmx1.5mm(ZF) package.	2025/2/26
V1.8	1. Update VOH VOL Data	2025/5/26
V1.9	1. Modify $T_{SK(O)}$ =100ps.	2025/7/7
V2.0	1. Modify VIL/VOH/VOL test condition. 2. Update Zo Data and test condition.	2025/12/09