Features

- Low Cost 4 LVCMOS Output Clock Buffer
- 12kHz to 20MHz additive phase jitter: <50fs RMS at 125MHz@3.3V
- Operates DC to160 MHz
- Universal Input: LVCMOS and LVTTL
- Output Skew: < 250ps
- Spread-spectrum tolerant
- -40 to +85°C, 3.3V or 5V Power Supply
- SOP8 Package

Applications

- General-Purpose Applications
- Networking
- Portable Test and Measurement

Description

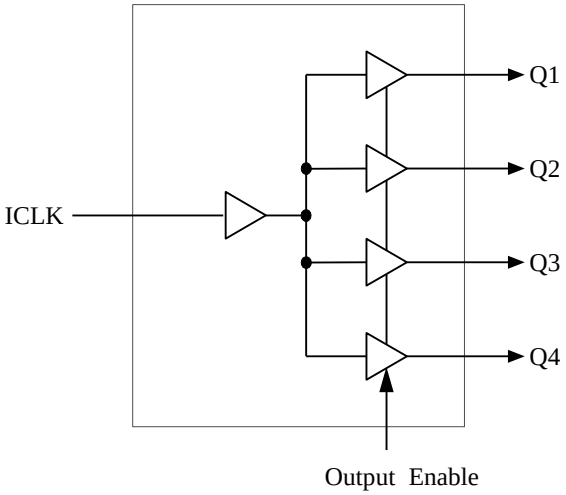
The RS2CB551 device is a high-performance, low-cost, small size, Fan out 1:4 clock buffer.
For more than 10 outputs see the RS2CBXX10 series of clock drivers.
The RS2CB551 operates from 3.3V/5V power supply. The Clock input and output tolerance can reach up to 5V.

Ordering Information

Part Number	Package	Description
RS2CB551WE	SOP8	pitch 1.27mm

Notes:
[1] E = Pb-free and Green

Block Diagram



Pin Configuration

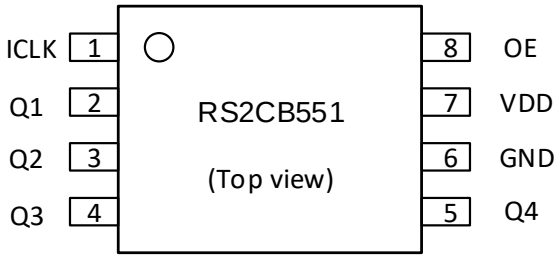


Figure 1 Pin Assignments for SOP8 Package

Pin Description

Table 1. Pin Descriptions

Pin Name	Pin Number	Type	Description
VDD	7	Power	Power Supply for 3.3V or 5.0V.
GND	6	GND	Ground pin.
OE	8	I, SE, PU	Output Enable. Tri-states outputs when low.Internal pull-up resistor. 1 = enable output, 0 = disable output.
ICLK	1	I, SE, PU	Clock input,internal pull-up resistor.
Q1	2	O, SE	LVCMOS Clock Output 1.
Q2	3	O, SE	LVCMOS Clock Output 2.
Q3	4	O, SE	LVCMOS Clock Output 3.
Q4	5	O, SE	LVCMOS Clock Output 4.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01uF should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RS2CB551 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Supply Voltage	VDD				5.5	V
All Inputs and Outputs			-0.5		VDD+0.5	V
Ambient Operating Temperature, Commercial	T_{AC}		0		70	°C
Ambient Operating Temperature, Industrial	T_{AI}		-40		85	°C
Lead Temperature (solder 4 s)	T_L				260	°C
Storage Temperature	T_S		-65		150	°C
Junction Temperature	T_J	Maximum operating junction temperature.			125	°C
Input ESD Protection	ESD	Human Body Model.			2500	V
		Charged-device Model			1000	V

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Core Supply Voltage	V_{DD}		3.0		5	V
Operating Temperature	T_A		-40	25	85	°C

DC Characteristics

VDD=3.3V ±10% , Ambient temperature -40°C ≤ TA ≤ 85°C, unless stated otherwise.

Table 4. DC Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Operating Voltage	VDD		3.0		3.6	V	
Input High Voltage, ICLK	V_{IH}		VDD/2+0.7		3.8	V	1
Input Low Voltage, ICLK	V_{IL}				VDD/2-0.7	V	1
Input High Voltage, OE	V_{IH}		2		VDD	V	
Input Low Voltage, OE	V_{IL}				0.8	V	
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V	
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V	
Operating Supply Current	IDD	No load, 135 MHz		18		mA	
Nominal Output Impedance	Z_O			20		Ω	
Internal Pull-up Resistor	R_{PU}	OE		500		kΩ	
Input Capacitance	C_{IN}	OE pin		5		pF	
Short Circuit Current	I_{OS}			±50		mA	

VDD=5.0V ±10% , Ambient temperature -40°C ≤ TA ≤ 85°C, unless stated otherwise.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Operating Voltage	VDD		4.5		5.5	V	
Input High Voltage, ICLK	V_{IH}		VDD/2+1		5.5	V	1
Input Low Voltage, ICLK	V_{IL}				VDD/2-1	V	1
Input High Voltage, OE	V_{IH}		2.6		VDD	V	
Input Low Voltage, OE	V_{IL}				0.8	V	
Output High Voltage	V_{OH}	I_{OH} = -35 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 35 mA			0.4	V	
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V	
Operating Supply Current	IDD	No load, 135 MHz		35		mA	
Nominal Output Impedance	Z_O			20		Ω	
Internal Pull-up Resistor	R_{PU}	OE		220		kΩ	
Input Capacitance	C_{IN}	OE pin		5		pF	
Short Circuit Current	I_{OS}			±80		mA	

1. Nominal switching threshold is VDD/2.

AC Characteristics

VDD=3.3V ±10%, Ambient temperature -40°C ≤ TA ≤ 85°C, unless stated otherwise.

Table 6. AC Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Input Frequency	F_{IN}				160	MHz	
Input duty cycle	I_{DC}		40%		60%		
Output Frequency	F_{OUT}	15 pF load			160	MHz	4
Output Clock Rise Time	t_R	0.8 to 2.0 V			1.0	ns	
Output Clock Fall Time	t_F	2.0 to 0.8 V			1.0	ns	
Propagation Delay		135 MHz	2	4	8	ns	1
Output to Output Skew		Rising edges at VDD/2			250	ps	2

VDD=5.0V ±10%, Ambient temperature -40°C ≤ TA ≤ 85°C, unless stated otherwise.

Table 7. AC Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Input Frequency	F_{IN}				135	MHz	
Input duty cycle	I_{DC}		40%		60%		
Output Frequency	F_{OUT}	15 pF load			135	MHz	4
Output Clock Rise Time	t_R	0.8 to 2.0 V			1.0	ns	
Output Clock Fall Time	t_F	2.0 to 0.8 V			1.0	ns	
Propagation Delay		135 MHz	1.5	3	6	ns	1
Output to Output Skew		Rising edges at VDD/2			250	ps	2

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle.
4. With external series resistor of 33Ω positioned close to each output pin.

Additive Jitter Characteristics

Table 8. Additive Jitter Characteristics

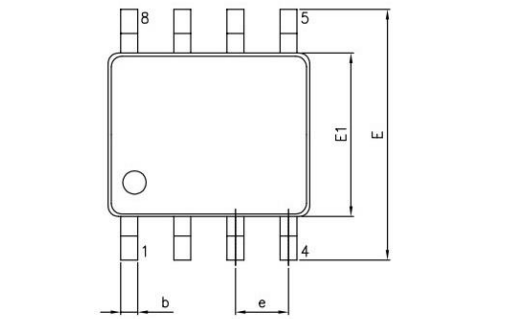
Characterized using RS2CB551 Performance when VDD= 3.3V. Outputs not under test are terminated to 50Ω.

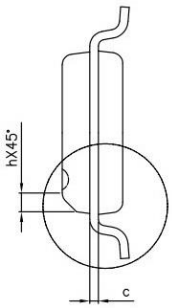
Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	Notes
Additive phase jitter	t_{jitter}	12 kHz to 5 MHz, f_{out} = 50 MHz		50		fs rms	1
		12 kHz to 20 MHz, f_{out} = 125 MHz		30			

1. CMOS input slew rate ≥ 2 V/ns, CL= 5pF. With rail to rail input clock.

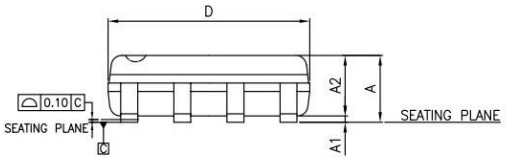
Package Information

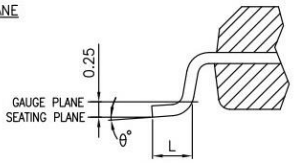
SOP8

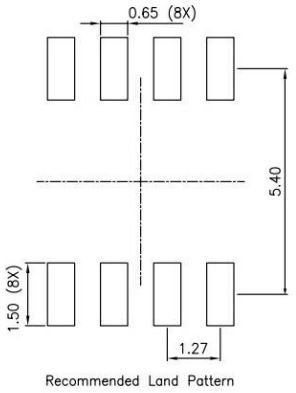




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8







Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary release	2024/06/21
1.0	1. Initial release	2024/09/24