Features

- Provides year, month, day, weekday, hours, minutes, and seconds
- Optional 12/24 hour format.
- Low power consumption: 500nA typical value
- Operating voltage: 1.8~5.3V.
- Operating temperature: -40℃~+85℃.
- Standard IIC bus interface, maximum speed 400KHz
- 12-byte SRAM
- Alarm function
- Countdown timer
- Programmable square-wave output
- Write protection function
- Built-in power supply voltage regulation, internal timing voltage can be as low as 1.5V.

Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment

Description

RS4C2058 is a real-time clock chip with a standard IIC interface, which can be used by the CPU to read and write data from 32 bytes of registers on the chip (including time registers, alarm registers, control registers, and general SRAM registers)

RS4C2058 built-in single timing/alarm interrupt output, alarm interrupt time can be set up to 100 years.

RS4C2058 built-in clock accuracy digital adjustment function, can correct the deviation of the clock in a wide range (-189ppm~+189ppm, resolution of 3.05ppm), and through the external temperature sensor can be set to adapt to the temperature change adjustment value, to achieve high precision timing function in a wide temperature range.

Ordering Information

Part Number	Package	Description
RS4C2058WE	SOP8	Pitch 1.27mm
RS4C2058UE	MSOP8	Pitch 0.65mm

Note:
E= Green Package

Typical Application Circuit

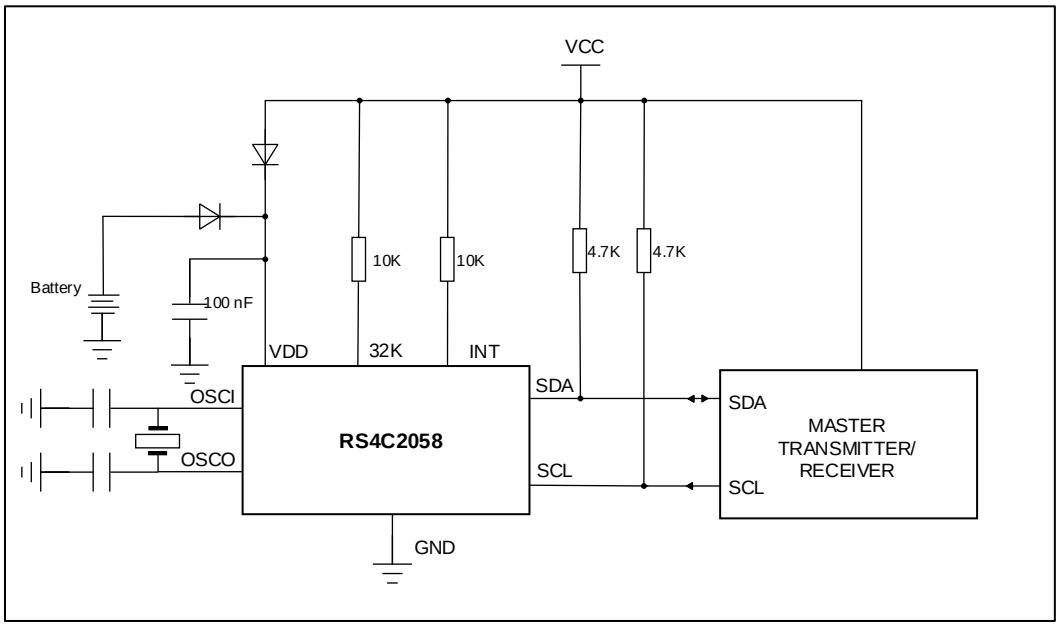


Figure1 Typical application circuit

Pin Configuration

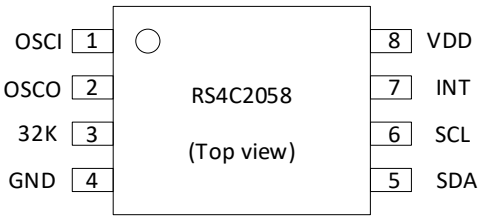


Figure2 Pin configuration

Pin Description

Pin Number	Pin Name	Description
1	OSCI	oscillator input
2	OSCO	oscillator output
3	32K	32KHZ frequency output pin (open-drain)
4	GND	Ground supply voltage
5	SDA	serial data line
6	SCL	serial clock input
7	INT	Interrupt/square-wave output (open-drain)
8	VDD	Power Supply

Note

[1]: Recommends tying VDD of the device and VDD of all the external pull-up resistors to the same Power Supply.

Registers Table

Addr. (hex)	Function (time range BCD format)	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Time and date registers									
00	Seconds	0	SECONDS (0 to 59)						
01	Minutes	0	MINUTES (0 to 59)						
02	Hours	12/24	0	AMPM	HOURS (1 to 12) in 12-hour mode				
				HOURS (0 to 23) in 24-hour mode					
03	Weekdays	0	0	0	0	0	WEEKDAYS (0 to 6)		
04	Days	0	0	Days(1-31)					
05	Months	0	0	0	MONTHS (1 to 12)				
06	Years	YEARS (0 to 99)							
Alarm register									
07	Second_alarm	0	SECOND _ALARM (0 to 59)						
08	Minute_alarm	0	MINUTE _ALARM (0 to 59						
09	Hour_alarm	0	0	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
				HOUR_ALARM (0 to 23) in 24-hour mode					
0A	Weekday_alarm	0	AW6	AW5	AW4	AW3	AW2	AW1	AW0
0B	Day_alarm	0	0	Day_alarm (1-31)					
0C	Month_alarm	0	0	0	Month_alarm (1 to 12)				
0D	Year_alarm	YEARS (0 to 99)							
0E	Alarm enable	0	EAY	EAMO	EAD	EAW	EAH	EAMN	EAS
Control registers									
0F	CTR1	WRTC3	0	INTAF	INTDF	0	WRTC2	0	RTCF
10	CTR2	WRTC1	IM	INTS1	INTS0	-	INTDE	INTAE	INTFE
11	CTR3	ARST	0	TDS1	TDS0	FS3	FS2	FS1	FS0
12	Offset	0	F6	F5	F4	F3	F2	F1	F0
13	Timer	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
14-1F	RAM	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Time and date registers

Seconds register(0x00)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 seconds			Seconds			

Minutes register(0x01)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			Minutes			

Hours register(0x02)

D7	D6	D5	D4	D3	D2	D1	D0
D7=1;24h mode D7=0;12h mode	0	D5=0;AM D5=1;PM	HOUR_ALARM (1 to 12) in 12-hour mode				
		HOUR_ALARM (0 to 23) in 24-hour mode					

Note:
In the 24-hour mode, the highest bit of the hour is set to 1. When you read the time, discard the highest bit or set it to 0. Otherwise, the hour time is incorrect.

Weekdays register(0x03)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Weekdays		

Days register(0x04)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		Days			

Months register(0x05)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	10Months	Months			

Years register(0x06)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Note:
During power-on reset, the real-time clock data register is not cleared or set inside the chip.

Alarm register

Second_alarm register(0x07)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 seconds			Seconds			

Minute_alarm register(0x08)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			Minutes			

Hour_alarm register(0x09)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	D5=0;AM D5=1;PM	HOUR_ALARM (1 to 12) in 12-hour mode				
		HOUR_ALARM (0 to 23) in 24-hour mode					

Weekday_alarm register(0x0A)

D7	D6	D5	D4	D3	D2	D1	D0
0	AW6 Saturday	AW5 Friday	AW4 Thursday	AW3 Wednesday	AW2 Tuesday	AW1 Monday	AW0 Sunday

Note:
For example,AW6 and AW1=1, other bits are 0, corresponding to Saturday, Monday will alarm

Day_alarm register(0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		Days			

Month_alarm register(0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	10Months	Months			

Year_alarm register(0x0D)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Alarm enable register(0x0E)

D7	D6	D5	D4	D3	D2	D1	D0
0	If EAY=1 Year enable	If EAMO=1 Month enable	If EAD=1 Day enable	If EAW=1 Week enable	If EAH=1 Hour enable	If EAMN=1 Min Enable	If EAS=1 Sec enable

Control register

CTR1 register(0x0F)

Bit	Symbol	Description
7	WRTC3	**Write protection**[*1]
6	0	/
5	INTAF	**alarm flag** 0 = read: alarm flag inactive 0 = write: alarm flag is cleared 1= read: alarm flag active 1= write: alarm flag remains unchanged
4	INTDF	**timer flag** 0=no timer interrupt generated 1=flag set when timer interrupt generated
3	0	/
2	WRTC2	**Write protection**[*1]
1	0	/
0	RTCF	Power on after all power supplies fail. This bit is 1.After power-on, as long as the register is successfully written, this bit will be cleared to 0

CTR2 register(0x10)

Bit	Symbol	Description
7	WRTC1	**Write protection**[*1]
6	IM	**Alarm interrupt mode** 0:Single alarm,INT pin output low level until alarm flag is cleared to 0 1:Periodic alarm,INT pin output a periodic pulse of 250ms width until the interrupt enable bit is cleared to 0
5	INTS1	**INT pin interrupt output selection** INTS1=0,INTS0=0;Output high resistance INTS1=0,INTS0=1;Alarm interrupt output INTS1=1,INTS0=0;Frequency output INTS1=1,INTS0=1;Timer interrupt output
4	INTS0	
3	-	Non-function
2	INTDE	**Timer enable** 0=timer disable 1=timer enable
1	INTAE	**Alarm enable** 0=alarm disable 1=alarm enable
0	INTFE	**Frequency enable** 0=Frequency disable 1=Frequency enable

Note：

When WRTC1=WRTC2=WRTC3=1, the register allows writing values.It need to set WRTC1=1 before WRTC2=WRTC3=1

When WRTC1=WRTC2=WRTC3=0, the register cannot write values.It need to set WRTC2=WRTC3=0 before WRTC1=0.

Write disable does not affect read operations

CTR3 register(0x11)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>ARST</td><td>Reset enable
1=read CTR1 register,INTAF and INTDF clear to 0</td></tr>
<tr><td>6</td><td>0</td><td>/</td></tr>
<tr><td>5</td><td>TDS1</td><td rowspan="2">Timer frequency source selection
<table>
<tr><th>TDS1</th><th>TDS0</th><th>Timer source(Hz)</th></tr>
<tr><td>0</td><td>0</td><td>4096</td></tr>
<tr><td>0</td><td>1</td><td>64</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1/60</td></tr>
</table></td></tr>
<tr><td>4</td><td>TDS0</td></tr>
<tr><td>3</td><td>FS3</td><td rowspan="4">Frequency selection
<table>
<tr><th>FS3</th><th>FS2</th><th>FS1</th><th>FS0</th><th>频率（Hz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>32768</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>4096</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1024</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>64</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>32</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1/4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1/8</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1/16</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1s</td></tr>
</table></td></tr>
<tr><td>2</td><td>FS2</td></tr>
<tr><td>1</td><td>FS1</td></tr>
<tr><td>0</td><td>FS0</td></tr>
</table>

Offset register(0x12)

D7	D6	D5	D4	D3	D2	D1	D0
0	F6	F5	F4	F3	F2	F1	F0

Using the digital time precision adjustment circuit, the number of 32768Hz pulses contained in the current 1 second can be changed every 20 seconds to adjust the time accuracy.
When F6 = 0, the number of pulses in the register producing one second is increased to 32768+((F5,F4,F3,F2,F1,F0)-1) x 2;
When F6 is 0, the number of pulses in the register producing one second is reduced to32768-((/F5,/F4,/F3,/F2,/F1,/F0)+1) x 2;(/F5 is the complement of F5)
When (F6,F5,F4,F3,F2,F1,F0)=(*,0,0,0,0,0,*),Generates 1 second register count pulse unchanged.
Because the minimum value of increasing or decreasing the count pulse every 20s is 2, the minimum precision of adjusting the clock adjustment register is 2/(32768 x 20)=3.015ppm.

Adjustment value calculation method:
(1) When the crystal frequency is greater than 32768Hz,
Adjusted value = (crystal frequency-32768）*10+1；
(2) When the crystal frequency is less than 32768Hz,
Adjusted value = (crystal frequency-32768）*10；
The adjusted value is a value from F6 to F0, expressed in binary complement form.

For example:
(1) crystal frequency =32770Hz
Adjusted value = (32770-32768)*10+1=21;
F6 ~ F0 =(0,0,1,0,1,0,1)
(2) crystal frequency =32762Hz
Adjusted value = (32762-32768)*10=-60
F6 ~ F0=(1,0,0,0,1,0,0)

Time adjustment does not change the INT pin output frequency.
Maximum adjustment range:
1) crystal frequency greater than 32768Hz, adjustment range F6 ~F0 from (0,0,0,0,0,0,0) to (0,1,1,1,1,1,1),Actual adjustable range from -3.05ppm to -189.2ppm.
2) crystal frequency less than 32768Hz, adjustment range F6 ~F0 from (1,1,1,1,1,1,1) to (1,0,0,0,0,1,0),Actual adjustable range from 3.05ppm to 189.2ppm.

Timer register(0x13)

D7	D6	D5	D4	D3	D2	D1	D0
0-255							

RAM register(0x14 -1F)

D7	D6	D5	D4	D3	D2	D1	D0
12Bytes							

The I2C Bus Interface

The RS4C2058 supports the I2C protocol. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The RS4C2058 operates as a slave on the I2C bus. Within the bus specifications, a standard mode (100kHz cycle rate) and a fast mode (400kHz cycle rate) are defined. The RS4C2058 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.
Slave addresses have a fixed length of 7 bits. The slave address is [**0110010**].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

Slave address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	R/W
0	1	1	0	0	1	0	1 = Read 0 = Write

Read mode

In this mode, the master reads the slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the

master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

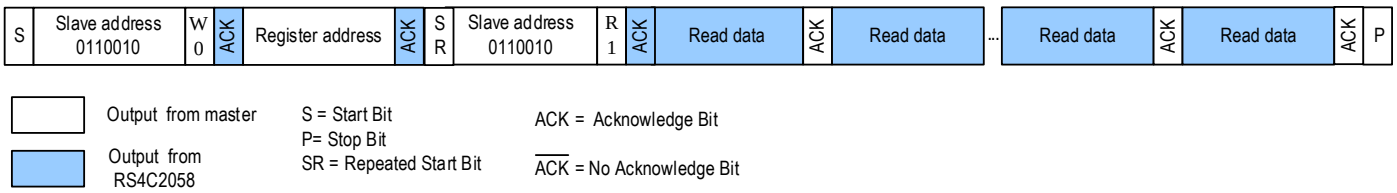


Figure 3 Read Mode Sequence

Write mode

In this mode the master transmitter transmits to the slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

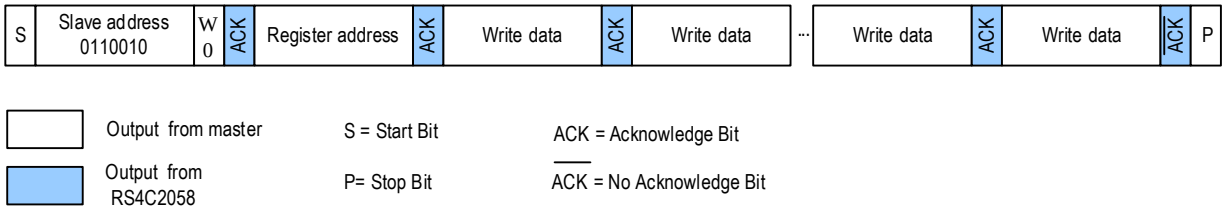


Figure 4 Write Mode Sequence

Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	output voltage		-0.5	+7	V
T_{stg}	storage temperature		-60	+150	°C
T_{amb}	ambient temperature	operating device	-40	+85	°C

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VDD	Main power supply		1.8		5.3	V
IDD1	Supply Current	VDD=5V		0.6	1	uA
		VDD=3V		0.5	1	uA
IDD2	Supply Current with IIC Active	VDD=5V		20	120	uA
ILI	Input leakage current on SCL			100		nA
ILO	I/O leakage current on SDA			100		nA
V_{BATHYS}	VBAT Hysteresis			100		mV
INT VOL	Output low Voltage	VDD=5V,IOH=2mA			0.4V	V

I2C AC Characteristics

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time*3/4	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7			10		pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay*8			100		ms

Note:

1.Limits at -40°C are guaranteed by design and not production tested.

2.After this period, the first clock pulse is generated

3.A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to

bridge the undefined region of the falling edge of SCL

4.The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

5.A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geqslant$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX} + t_{SU:DAT} = 1000 + 250 = 1250$ns before the SCL line is released.

6.C_B—total capacitance of one bus line in pF

7.Guaranteed by design. Not production tested

8.The parameter t_{OSF} is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of $Vcc_{MIN} V \leqslant V_{CC} \leqslant V_{CC\ MAX}$

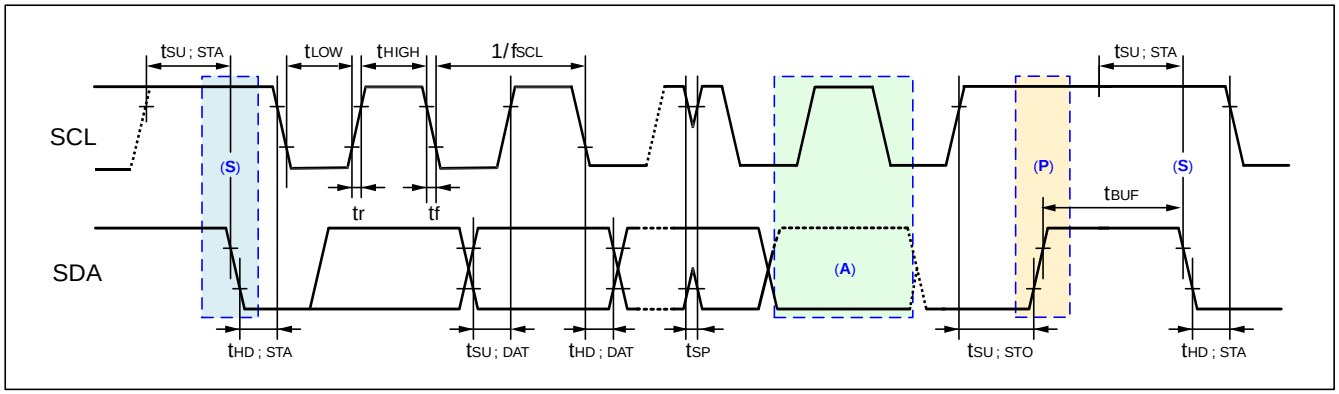
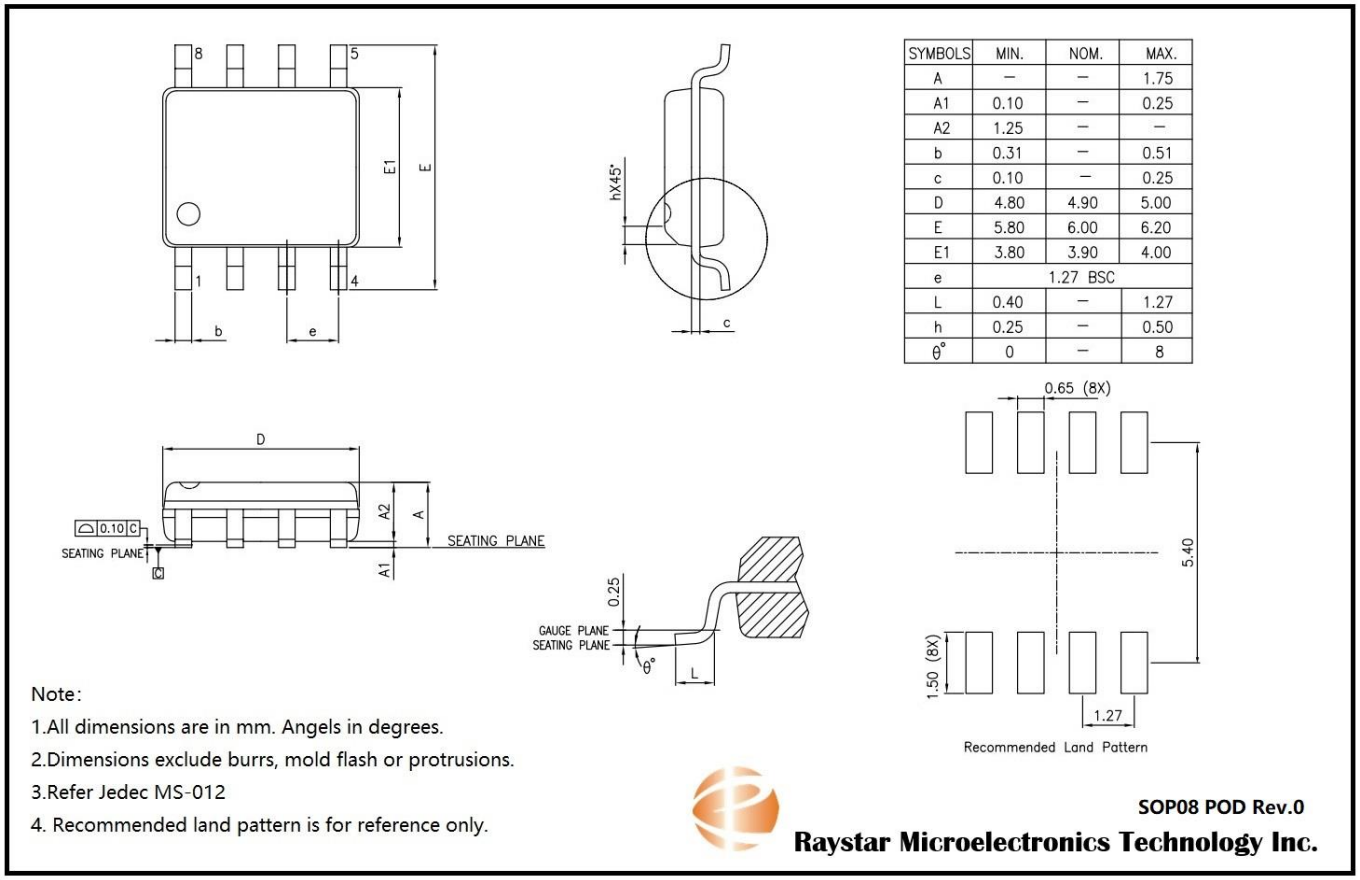


Figure5 I2C-bus timing diagram

Package Information

SOP8

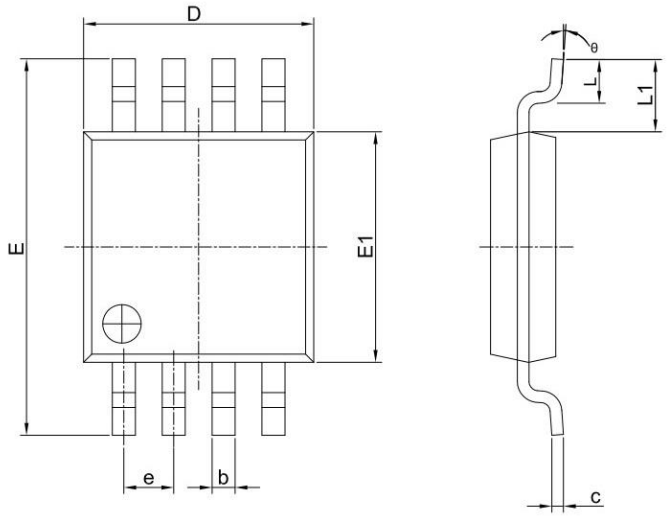


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

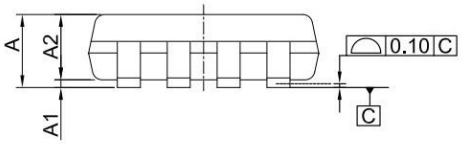
Note:
1.All dimensions are in mm. Angels in degrees.
2.Dimensions exclude burrs, mold flash or protrusions.
3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD Rev.0
Raystar Microelectronics Technology Inc.

MSOP8



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°



Note:
1.All dimensions are in mm. Angels in degrees.
2.Refer Jedec MO-187
3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08

Raystar Microelectronics Technology Inc.

Revision History

Revision	Description	Date
0.9	Preliminary Release	2024/12/10
1.0	Initial Release	2025/01/04